DISCRETE SEMICONDUCTORS

Small-signal and Medium-power MOS Transistors

1997

Data Handbook SC13b

Let's make things better.

Philips Semiconductors

PHILIPS

QUALITY ASSURED

Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

PRODUCT SAFETY

In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility towards the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical', 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

Small-signal and Medium-power MOS Transistors

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PREFACE

Dear Customer,

We are pleased to introduce the new SC13b data handbook for Small-signal and Medium PowerMOS Transistors. Together with the recently published SC13a, PowerMOS Transistors (including TOPFETs and IGBTs), you have a complete overview of Philips Semiconductors' large product offering in small-signal, medium- and high power MOS transistors for switching applications. Our JFETs and dual-gate MOS transistors can be found in data handbook SC07, of which an update is planned for the second half of 1997.

In the new SC13b data handbook, you'll find our extensive range of N-and P-channel MOS transistors intended for switching applications in both wired and wireless telecom terminals, DC-DC convertors, power management and motor control. Our new TRENCHMOS process means that we can offer you cost-effective, very low-ohmic switches in various surface mount packages. We are well positioned to meet your demands for FET products now, and in the future.

To assist you with actual design work, SC13b includes a number of application notes, and a diskette containing the latest SPICE models. We would also like to inform you that we publish a Power Semiconductors Applications Handbook, giving you even more design ideas.

For further information, visit our WWW site, contact your local Philips Semiconductors' sales office or get in touch with our franchised distributors.

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N-CHANNEL D-MOS-FETS

TYPE NUMBER	PACKAGE	RATINGS			CHARACTERISTICS						PAGE
		V_{DS} (V)	I_D (mA)	P_{tot} (mW)	V_{GSth} (V)	R_{DSon} (Ω) typ.	R_{DSon} (Ω) max.	at I_D (mA)	at V_{GS} (V)	t_{on}/t_{off} max. (ns)	
BS107	SOT54 (TO-92) var.	200	150	830	0.8 to 2.4	20	28	20	2.6	10/20	52
BS107A	SOT54 (TO-92) var.	200	250	600	1 to 3	4.5	6.4	250	10	5/15	58
BS108	SOT54 (TO-92) var.	200	250	1000	0.4 to 1.8	5	8	100	2.8	10/30	62
BS170	SOT54 (TO-92) var.	60	500	830	0.8 to 3	2.5	5	200	10	10/10	65
BSH101	SOT23	60	700	500	1 to 2.8	–	0.69	350	10	7/10(1)	76
BSH102	SOT23	30	1000	500	1 to 2.8	–	0.3	500	10	8/13(1)	79
BSH103	SOT23	30	900	500	0.5 to 1.1	–	0.35	450	4.5	6/13(1)	82
BSH105	SOT23	12	1500	500	0.4(2)	–	0.12	800	4.5	–	85
BSH106	SOT363	12	1800	800	0.4(2)	–	0.14	900	4.5	–	88
BSN10	TO-92	50	175	830	0.4 to 1.8	8	15	100	10	5/10	97
BSN10A	TO-92	50	175	830	0.4 to 1.8	8	15	100	10	5/10	97
BSN20	SOT23	50	100	250	0.4 to 1.8	8	15	100	10	5/10	101
BSN20W	SOT323	50	80	200	0.4 to 1.8	8	15	80	10	5/10	105
BSN205	SOT54 (TO-92) var.	200	300	1000	0.8 to 2.8	4	6	400	10	10/20	109
BSN205A	SOT54 (TO-92) var.	200	300	1000	0.8 to 2.8	4	6	400	10	10/20	109
BSN254	SOT54 (TO-92) var.	250	300	1000	0.8 to 2	5	10	20	2.4	10/30	112
BSN254A	SOT54 (TO-92) var.	250	300	1000	0.8 to 2	5	10	20	2.4	10/30	112
BSN274	SOT54 (TO-92) var.	270	250	1000	0.8 to 2	9	14	20	2.4	10/30	117
BSN274A	SOT54 (TO-92) var.	270	250	1000	0.8 to 2	9	14	20	2.4	10/30	117
BSN304	SOT54 (TO-92) var.	300	250	1000	0.8 to 2	7.9	14	20	2.4	10/30	120
BSN304A	SOT54 (TO-92) var.	300	250	1000	0.8 to 2	7.9	14	20	2.4	10/30	120
BSP030	SOT223	30	10000	5000	1 to 2.8	–	0.03	5000	10	60/150	126
BSP89	SOT223	240	350	1500	0.8 to 2	4	6	340	10	10/30	140
BSP100	SOT223	30	3500	5000	1 to 2.8	0.08	0.1	2200	10	40/75	146
BSP106	SOT223	60	425	1500	0.8 to 3	2.5	4	200	10	5/15	152
BSP107	SOT223	200	200	1500	0.8 to 2.4	20	28	20	2.6	10/20	158
BSP108	SOT223	80	500	1500	1.5 to 3.5	2	3	500	10	8/15	164
BSP110	SOT223	80	325	1500	0.8 to 2.8	7	10	150	5	5/10	169
BSP120	SOT223	200	250	1500	0.8 to 2.8	7	12	250	10	6/20	174
BSP121	SOT223	200	350	1500	0.8 to 2.8	4.5	6	400	10	10/20	179
BSP122	SOT223	200	550	1500	0.4 to 2	1.6	2.5	750	10	35/50	185
BSP126	SOT223	250	350	1500	0.8 to 2	5	10	20	2.4	10/30	187
BSP127	SOT223	270	350	1500	0.8 to 2	6.5	8	250	10	10/30	192
BSP128	SOT223	200	350	1500	0.4 to 1.8	5	8	100	2.8	10/30	194
BSP130	SOT223	300	300	1500	0.8 to 2	6.7	8	250	10	10/30	196
BSP152	SOT223	200	550	1500	1.5 to 3.5	–	2.5	750	10	15/30	202

N-CHANNEL D-MOS-FETS

TYPE NUMBER	PACKAGE	RATINGS			CHARACTERISTICS						PAGE
		V_{DS} (V)	I_D (mA)	P_{tot} (mW)	V_{GSth} (V)	R_{DSon} (Ω) typ.	R_{DSon} (Ω) max.	at I_D (mA)	at V_{GS} (V)	t_{on}/t_{off} max. (ns)	
BSS87	SOT89	200	280	1000	0.8 to 2.8	4.5	6	400	10	10/25	272
BSS89	SOT54 (TO-92) var.	240	300	1000	0.8 to 2.8	4.5	6	400	10	5/15(1)	275
BSS123	SOT23	100	150	250	0.8 to 2.8	3	6	120	10	10/20	281
BST70A	SOT54 (TO-92) var.	80	500	1000	1.5 to 3.5	2	4	500	10	10/15	290
BST72A	SOT54 (TO-92) var.	80	300	830	1.5 to 3.5	7	10	150	5	10/10	296
BST74A	SOT54 (TO-92) var.	200	250	1000	0.8 to 2.8	6	12	250	10	10/25	302
BST76A	SOT54 (TO-92) var.	180	300	1000	0.7 to 2.4	7	10	15	3	10/15	308
BST80	SOT89	80	500	1000	1.5 to 3.5	2	3	500	10	10/15	313
BST82	SOT23	80	175	300	1.5 to 3.5	7	10	150	5	10/10	318
BST84	SOT89	200	250	1000	0.8 to 2.8	6	12	250	10	10/25	324
BST86	SOT89	180	300	1000	0.7 to 2.7	7	10	15	3	10/15	330
PHN103	SOT96 (SO8)	30	8500	4000	1 to 2.8	–	0.03	5500	10	35/150	378
PHN110	SOT96 (SO8)	30	4000	2800	1 to 2.8	0.08	0.1	2000	10	16/50	386
PHN205(3)	SOT96 (SO8)	30	6400	3500	1 to 2.8	–	0.05	3200	10	15/32(1)	393
PHN210(3)	SOT96 (SO8)	30	3500	2000	1 to 2.8	0.08	0.1	2200	10	40/140	400
PHN405(4)	SOT338-1	30	4000	1400	1 to 2.8	–	0.05	2000	10	30/50	407
PHN708(5)	SOT340-1	30	3100	1300	1 to 2.8	–	0.08	1500	10	30/45	411
PHN1013	SOT96 (SO8)	30	10000	2500	2.1 to 4	0.011	0.0135	10000	10	165/180	415
PMBF107	SOT23	200	100	250	0.8 to 2.4	20	28	20	2.6	10/20	450
PMBF170	SOT23	60	250	300	0.8 to 3	2.5	5	200	10	10/15	455
2N7000	SOT54 (TO-92) var.	60	280	830	0.8 to 3	3.5	5.3	75	4.5	10/10	40
2N7002	SOT23	60	180	300	0.8 to 3	3.5	5.3	75	4.5	10/15	446

Notes

1. Typical values.
2. Minimum values.
3. Dual FET.
4. 4 - FET array.
5. 7 - FET array.

P-CHANNEL D-MOS-FETS

TYPE NUMBER	PACKAGE	RATINGS			CHARACTERISTICS						PAGE
		V_{DS} (V)	I_D (mA)	P_{tot} (mW)	V_{GSth} (V)	R_{DSon} (Ω) typ.	R_{DSon} (Ω) max.	at I_D (mA)	at V_{GS} (V)	t_{on}/t_{off} max. (ns)	
BS208	SOT54 (TO-92) var.	200	200	830	0.8 to 2.8	10	14	200	10	10/30	68
BS250	SOT54 (TO-92) var.	45	250	830	1 to 3.5	9	14	200	10	4/10	73
BSH205	SOT23	12	1000	500	0.4(2)	–	0.3	500	4.5	–	91
BSH206	SOT363	12	1200	800	0.4(2)	–	0.36	600	4.5	–	94
BSP090	SOT223	30	5700	5000	1 to 2.8	–	0.09	2800	10	25/190	133
BSP92	SOT223	240	180	1500	0.8 to 2	10	20	180	10	10/30	143
BSP204	SOT54 (TO-92) var.	200	250	1000	0.8 to 2.8	10	15	200	10	10/30	208
BSP204A	SOT54 (TO-92) var.	200	250	1000	0.8 to 2.8	10	15	200	10	10/30	208
BSP205	SOT223	60	275	1500	1.5 to 3.5	7.5	10	200	10	6/15	214
BSP206	SOT223	60	350	1500	1.5 to 3.5	4.5	6	200	10	8/25	220
BSP220	SOT223	200	225	1500	0.8 to 2.8	10	12	200	10	20/30	225
BSP225	SOT223	250	225	1500	0.8 to 2.8	10	15	200	10	10/30	231
BSP230	SOT223	300	210	1500	1.7 to 2.55	–	17	170	10	10/30	237
BSP250	SOT223	30	3000	5000	1 to 2.8	0.22	0.25	1000	10	80/140	243
BSP254	SOT54 (TO-92) var.	250	200	1000	0.8 to 2.8	10	15	200	10	10/30	249
BSP254A	SOT54 (TO-92) var.	250	200	1000	0.8 to 2.8	10	15	200	10	10/30	249
BSP255	SOT223	300	325	4000	0.8 to 2	–	17	160	10	4/25(1)	254
BSP304	SOT54 (TO-92) var.	300	170	1000	1.7 to 2.55	–	17	170	10	10/30	261
BSP304A	SOT54 (TO-92) var.	300	170	1000	1.7 to 2.55	–	17	170	10	10/30	261
BSS84	SOT23	50	130	250	0.8 to 2	–	10	130	10	3/7(1)	267
BSS92	SOT54 (TO-92) var.	240	150	1000	0.8 to 2.8	10	20	100	10	5/20(1)	278
BSS192	SOT89	240	150	1000	0.8 to 2.8	10	20	100	10	10/30	285
BST100	SOT54 (TO-92) var.	60	300	1000	1.5 to 3.5	4.5	6	200	10	4/20	336
BST120	SOT89	60	300	1000	1.5 to 3.5	4.5	6	200	10	4/20	341
BST122	SOT89	60	250	1000	1.5 to 3.5	7.5	10	200	10	4/10	346
PHP109	SOT96 (SO8)	30	5000	4000	1 to 2.8	–	0.09	2500	10	35/200	418
PHP125	SOT96 (SO8)	30	2500	2800	1 to 2.8	0.22	0.25	1000	10	16/80	425
PHP212(3)	SOT96 (SO8)	30	4000	3500	1 to 2.8	–	0.12	2000	10	10/45(1)	432
PHP212L(3)	SOT96 (SO8)	30	4000	3500	0.5 to 1.1	–	0.12	2000	4.5	10/45(1)	440
PHP225(3)	SOT96 (SO8)	30	2300	2000	1 to 2.8	0.22	0.25	1000	10	80/140	443

Notes

1. Typical values.
2. Minimum values.
3. Dual FET.

COMPLEMENTARY N- AND P-CHANNEL D-MOS-FETS

TYPE NUMBER	PACKAGE	CHANNEL	RATINGS			CHARACTERISTICS						PAGE
			V_{DS} (V)	I_D (mA)	P_{tot} (mW)	V_{GSth} (V)	R_{DSon} (Ω) typ.	R_{DSon} (Ω) max.	at I_D (mA)	at V_{GS} (V)	t_{on}/t_{off} max. (ns)	
PHC2300	SOT96 (SO8)	N	300	350	2000	0.8 to 2	–	8	175	10	10/30	351
		P	300	250	2000	0.8 to 2	–	17	125	10	10/35	351
PHC20512	SOT96 (SO8)	N	30	6400	3500	1 to 2.8	–	0.05	3200	10	15/32[1]	355
		P	30	4000	3500	1 to 2.8	–	0.12	2000	10	10/45[1]	355
PHC21025	SOT96 (SO8)	N	30	3500	2000	1 to 2.8	0.08	0.1	2200	10	40/140	368
		P	30	2300	2000	1 to 2.8	0.22	0.25	1000	10	80/140	368

Note

1. Typical values.

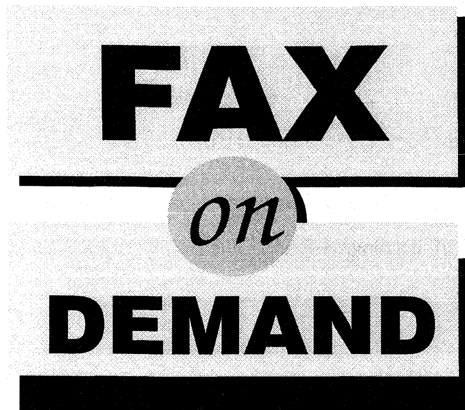
Small-signal and Medium-power MOS transistors

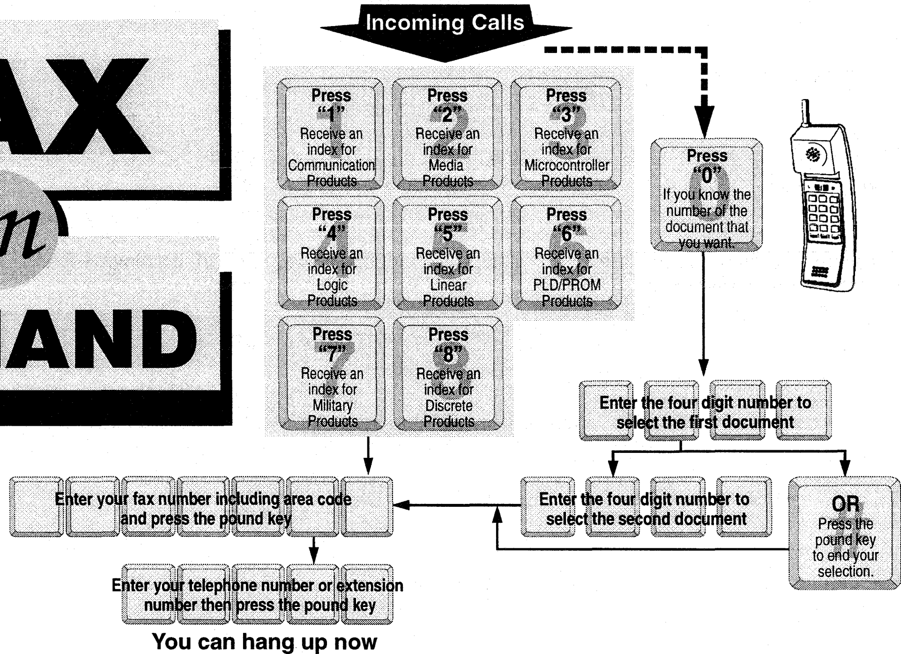
Marking codes

Types in SOT23, SOT89, and SOT323 packages are marked with a code as listed in the following table.

TYPE NUMBER	MARKING CODE
BSN20	M8p
BSN20W	M8t
BSS84	SP
BSS87	KA
BSS123	SA
BSS192	KB
BST80	KM
BST82	02p
BST84	KN
BST86	KO
BST120	LM
BST122	LN
PMBF107	pKz
PMBF170	pKX
2N7002	702

FAX-on-DEMAND System





What is it?

The FAX-on-DEMAND system is a computer facsimile system that allows customers to receive selected documents by fax automatically.

How does it work?

To order a document, you simply enter the document number. This number can be obtained by asking for an index of available documents to be faxed to you the first time you call the system.

Our system has a selection of the latest product data sheets from Philips with varying page counts. As you know, it takes approximately one minute to FAX one page. This isn't bad if the number of pages is less than 10. But if the document is 37 pages long, be ready for a long transmission!

Philips Semiconductors also maintains product information on the World-Wide Web. Our home page can be located at:
http://www.semiconductors.philips.com

Who do I contact if I have a question about FAX-on-DEMAND?

Contact your local Philips sales office.

FAX-on-DEMAND phone numbers:

England (United Kingdom, Ireland)	44-181-730-5020
France	33-1-40-99-60-60
Italy	39-167-295502
North America	1-800-282-2000

Locations soon to be in operation:

Hong Kong
Japan
The Netherlands

Internet World Wide Web Home Page

WHAT IS IT?

Welcome to our place in cyberspace.

The Discretes Group now has its own home page within Philips Semiconductors. Explore our Web pages and take a look at our product offering of advance Discrete Applications and Products.

In addition we offer you the latest information on Products, News, Support, Employment and Offices.

HOW TO REACH US

For access to the Philips Semiconductors Home Page go to the World Wide Web location:

http://www.semiconductors.philips.com/

You can find us in the Product category of Discretes.

GENERAL

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QUALITY

Total Quality Management

Philips Semiconductors is a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system which is described in our Quality manuals. The basis is outlined in the following paragraphs.

QUALITY ASSURANCE

Based on ISO 9000 standards, customer standards such as FDC, QS9000 and IBM MDQ. Our factories are certified to ISO 9000 by external inspectorates.

PARTNERSHIPS WITH CUSTOMERS

PPM co-operations, design-in agreements, ship-to-stock, just-in-time, self-qualification programmes, and application support.

PARTNERSHIPS WITH SUPPLIERS

Ship-to-stock, statistical process control and ISO 9000 audits.

QUALITY IMPROVEMENT PROGRAMME

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

Advanced quality planning

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase in preparation for production under statistical process control.

Product conformance

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- Incoming material management through partnerships with suppliers
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Process steps are under statistical process control
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications SNW-EQ-611 part A
- Periodic inspections to monitor and measure the conformance of products
- Qualification tests (see SNW-EQ-611 part A).

Product reliability

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the product's reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

Customer response

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

Recognition

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organizations.

PRO ELECTRON TYPE NUMBERING SYSTEM

Basic type number

This type designation code applies to discrete semiconductor devices (not integrated circuits), multiples of such devices, semiconductor chips and Darlington transistors.

FIRST LETTER

The first letter gives information about the material for the active part of the device.

- A Germanium or other material with a band gap of 0.6 to 1 eV
- B Silicon or other material with a band gap of 1 to 1.3 eV
- C Gallium arsenide (GaAs) or other material with a band gap of 1.3 eV or more
- R Compound materials, e.g. cadmium sulphide.

SECOND LETTER

The second letter indicates the function for which the device is primarily designed. The same letter can be used for multi-chip devices with similar elements.

In the following list low power types are defined by $R_{th\ j\text{-}mb}$ > 15 K/W and power types by $R_{th\ j\text{-}mb} \leq 15$ K/W.

- A Diode; signal, low power
- B Diode; variable capacitance
- C Transistor; low power, audio frequency
- D Transistor; power, audio frequency
- E Diode; tunnel
- F Transistor; low power, high frequency
- G Multiple of dissimilar devices/miscellaneous devices; e.g. oscillators. Also with special third letter; see under Section “Serial number”.
- H Diode; magnetic sensitive
- L Transistor; power, high frequency
- N Photocoupler
- P Radiation detector; e.g. high sensitivity photo-transistor; with special third letter
- Q Radiation generator; e.g. LED, laser; with special third letter
- R Control or switching device; e.g. thyristor, low power; with special third letter
- S Transistor; low power, switching
- T Control or switching device; e.g. thyristor, power; with special third letter
- U Transistor; power, switching
- W Surface acoustic wave device
- X Diode; multiplier, e.g. varactor, step recovery
- Y Diode; rectifying, booster
- Z Diode; voltage reference or regulator, transient suppressor diode; with special third letter.

SERIAL NUMBER

The number comprises three figures running from 100 to 999 for devices primarily intended for consumer equipment, or one letter (Z, Y, X, etc.) and two figures running from 10 to 99 for devices primarily intended for industrial or professional equipment.[1]

Version letter

A letter may be added to the basic type number to indicate minor electrical or mechanical variants of the basic type.

RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

(1) When the supply of these serial numbers is exhausted, the serial number may be expanded to three figures for industrial types and four figures for consumer types.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

LETTER SYMBOLS

The letter symbols for transistors detailed in this section are based on IEC publication number 148.

Letter symbols for currents, voltages and powers

BASIC LETTERS

I, i current

V, v voltage

P, p power.

Upper-case letter symbols are used to represent all values except instantaneous values that vary with time, these are represented by lower-case letters.

SUBSCRIPTS

A, a	anode terminal
(AV), (av)	average value
B, b	base terminal
(BO)	breakover
(BR)	breakdown
C, c	collector terminal
D, d	drain terminal
E, e	emitter terminal
F, f	forward

G, g	gate terminal
H	holding
I, i	input
K, k	cathode terminal
L	load
M, m	peak value
(min)	minimum
(max)	maximum
O, o	as third subscript: the terminal not mentioned is open-circuit
(OV)	overload
P, p	pulse
R, r	as first subscript: reverse. As second subscript: repetitive. As third subscript: with a specified resistance between the terminal not mentioned and the reference terminal
(RMS), (rms)	root-mean-square value
S, s	as first or second subscript: source terminal (FETs only). As second subscript: non-repetitive (not FETs). As third subscript: short circuit between the terminal not mentioned and the reference terminal
TO	threshold
tot	total
W	working
X, x	specified circuit
Z, z	replaces R to indicate the actual working voltage, current or power of voltage reference and voltage reference diodes.

No additional subscript is used for DC values.

Upper-case subscripts are used for the indication of:

- Continuous (DC) values (without signal), e.g. I_D
- Instantaneous total values, e.g. i_D
- Average total values, e.g. $I_{D(AV)}$
- Peak total values, e.g. I_{DM}
- Root-mean-square total values, e.g. $I_{D(RMS)}$.

Lower-case subscripts are used for the indication of values applying to the varying component alone:

- Instantaneous values, e.g. i_d
- Root-mean-square values, e.g. $I_{d(rms)}$
- Peak values, e.g. I_{dm}
- Average values, e.g. $I_{d(av)}$.

If more than one subscript is used, the subscript for which both styles exist are either all upper-case or all lower-case.

ADDITIONAL RULES FOR SUBSCRIPTS

Transistor currents

If it is necessary to indicate the terminal carrying the current, this should be done by the first subscript (conventional current flow from the external circuit into the terminal is positive).

Examples: I_D, i_D, i_d, I_{dm}.

Transistor voltages

If it is necessary to indicate the points between which a voltage is measured, this should be done by the first two subscripts. The first subscript indicates the terminal at which the voltage is measured and the second the reference terminal or the circuit node. Where there is no possibility of confusion, the second subscript may be omitted.

Examples: V_{GS}, v_{GS}, v_{gs}, V_{gsm}.

Supply voltages or currents

Supply voltages or supply currents are indicated by repeating the appropriate terminal subscript.

Examples: V_{DD}, I_{SS}.

If it is necessary to indicate a reference terminal, this should be done by a third subscript.

Example: V_{DDS}.

Subscripts for devices with more than one terminal of the same kind

If a device has more than one terminal of the same kind, the subscript is formed by the appropriate letter for the terminal, followed by a number. In the case of multiple subscripts, hyphens may be necessary to avoid confusion.

Examples:

I_{G2}	continuous (DC) current flowing into the second gate terminal
V_{G2-S}	continuous (DC) voltage between the second gate and source terminals.

Subscripts for multiple devices

For multiple unit devices, the subscripts are modified by a number preceding the letter subscript. In the case of multiple subscripts, hyphens may be necessary to avoid confusion.

Examples:

I_{2D} continuous (DC) current flowing into the drain terminal of the second unit

V_{1D-2D} continuous (DC) voltage between the drain terminals of the first and second units.

Letter symbols for electrical parameters

DEFINITION

For the purpose of this publication, the term 'electrical parameter' applies to four-pole matrix parameters, elements of electrical equivalent circuits, electrical impedances and admittances, inductances and capacitances.

BASIC LETTERS

The following list comprises the most important basic letters used for electrical parameters of semiconductor devices.

B, b susceptance (imaginary part of an admittance)

C capacitance

G, g conductance (real part of an admittance)

H, h hybrid parameter

L inductance

R, r resistance (real part of an impedance)

X, x reactance (imaginary part of an impedance)

Y, y admittance

Z, z impedance.

Upper-case letters are used for the representation of:

- Electrical parameters of external circuits and of circuits in which the device forms only a part
- All inductances and capacitances.

Lower-case letters are used for the representation of electrical parameters inherent in the device, with the exception of inductances and capacitances.

SUBSCRIPTS

General subscripts

The following list comprises the most important general subscripts used for electrical parameters of semiconductor devices.

F, f forward (forward transfer)

I, i (or 1) input

L, l load

O, o (or 2) output

R, r reverse (reverse transfer)

S, s source.

Examples: Z_s, g_f, g_F.

The upper-case variant of a subscript is used for the designation of static (DC) values.

Examples:

g_{FS} static value of forward transconductance in common-source configuration (DC current gain)

R_{DS} DC value of the drain-source resistance.

The static value is the slope of the line from the origin to the operating point on the appropriate characteristic curve, i.e. the quotient of the appropriate electrical quantities at the operating point.

The lower-case variant of a subscript is used for the designation of small-signal values.

Examples:

g_{fs} small-signal value of the short-circuit forward transconductance in common-source configuration

$Z_i = R_i + jX_i$ small-signal value of the input impedance.

If more than one subscript is used, subscripts for which both styles exist are either all upper-case or all lower-case.

Examples: g_{FS}, g_{fs}.

THERMAL CONSIDERATIONS

Thermal resistance

Circuit performance and long-term reliability are affected by the temperature of the transistor die. Normally, both are improved by keeping the die temperature (junction temperature) low.

Electrical power dissipated in any semiconductor device is a source of heat. This increases the temperature of the die about some reference point, normally an ambient temperature of 25 °C in still air. The size of the increase in temperature depends on the amount of power dissipated in the circuit and the net thermal resistance between the heat source and the reference point.

Devices lose most of their heat by conduction when mounted on a a printed board, a substrate or heatsink. Referring to Fig.1 (for surface mounted devices mounted on a substrate), heat conducts from its source (the junction) via the package leads and soldered connections to the substrate. Some heat radiates from the package into the surrounding air where it is dispersed by convection or

by forced cooling air. Heat that radiates from the substrate is dispersed in the same way.

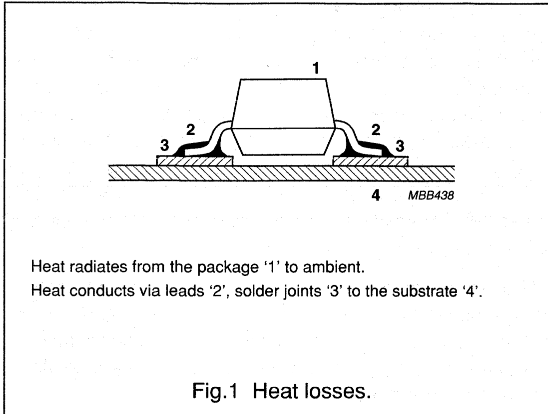


Fig.1 Heat losses.

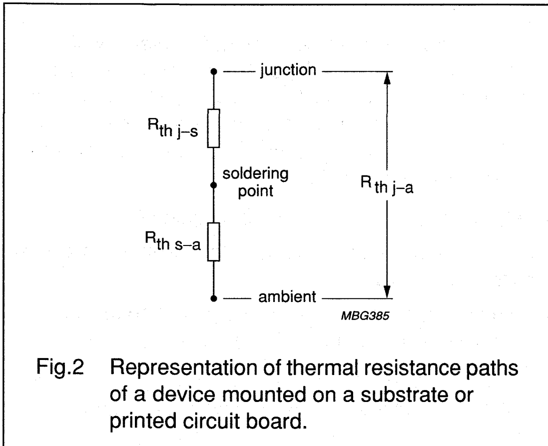


Fig.2 Representation of thermal resistance paths of a device mounted on a substrate or printed circuit board.

The elements of thermal resistance shown in Fig.2 are defined as follows:

$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base
$R_{th\ j\text{-}c}$	thermal resistance from junction to case
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point
$R_{th\ s\text{-}a}$	thermal resistance from soldering point to ambient
$R_{th\ c\text{-}a}$	thermal resistance from case to ambient ($R_{th\ s\text{-}a}$ and $R_{th\ c\text{-}a}$ are the same for most packages)
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient.

The temperature at the junction depends on the ability of the package and its mounting to transfer heat from the junction region to the ambient environment. The basic relationship between junction temperature and power dissipation is:

$$T_{j\ max} = T_{amb} + P_{tot\ max}(R_{th\ j\text{-}s} + R_{th\ s\text{-}a})$$
$$= T_{amb} + P_{tot\ max}(R_{th\ j\text{-}a})$$

where:

$T_{j\ max}$	is the maximum junction temperature
T_{amb}	is the ambient temperature
$P_{tot\ max}$	is the maximum power handling capability of the device, including the effects of external loads when applicable.

In the expression for $T_{j\ max}$, only T_{amb} and $R_{th\ s\text{-}a}$ can be varied by the user. The package mounting technique and the flow of cooling air are factors that affect $R_{th\ s\text{-}a}$. The device power dissipation can be controlled to a limited extent but under recommended usage, the supply voltage and circuit loading dictate a fixed power maximum. The $R_{th\ j\text{-}s}$ value is essentially independent of external mounting method and cooling air; but is sensitive to the materials used in the package construction, the die bonding method and the die area, all of which are fixed.

Values of $T_{j\ max}$ and $R_{th\ j\text{-}s}$, or $R_{th\ j\text{-}c}$ or $R_{th\ j\text{-}a}$ are given in the device data sheets. For applications where the temperature of the case is stabilized by a large or temperature-controlled heatsink, the junction temperature can be calculated from:

$T_j = T_{case} + P_{tot} \times R_{th\ j\text{-}c}$ or, using the soldering point (T_s) definition, from $T_j = T_s + P_{tot} \times R_{th\ j\text{-}s}$.

The thermal resistance from soldering point to ambient, and that from case to ambient depends on the substrate or PCB material used.

Refer to figures 3 and 4 for R_{th} versus mounting substrate area.

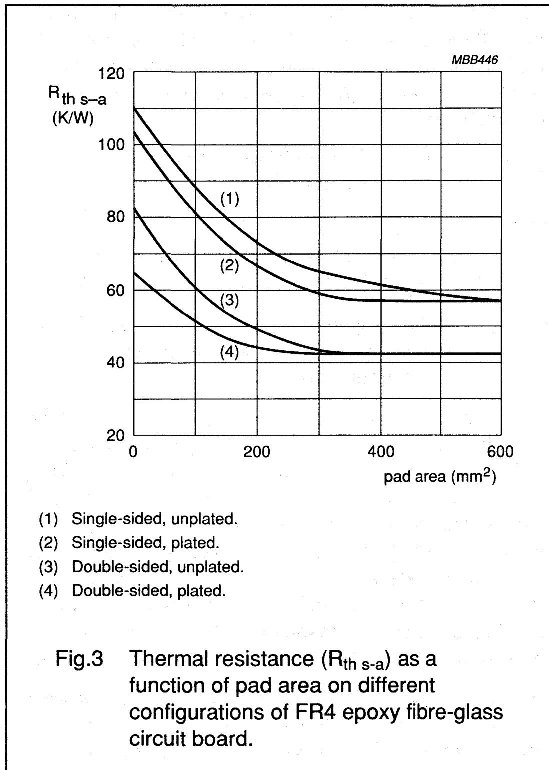


Fig.3 Thermal resistance ($R_{th\ s-a}$) as a function of pad area on different configurations of FR4 epoxy fibre-glass circuit board.

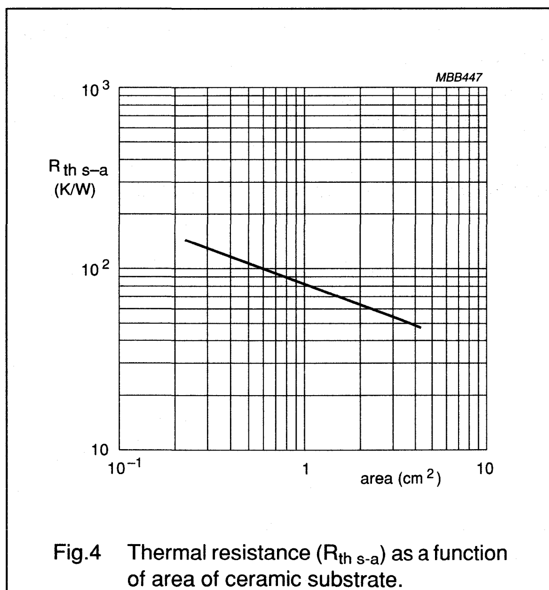


Fig.4 Thermal resistance ($R_{th\ s-a}$) as a function of area of ceramic substrate.

HANDLING MOS DEVICES

Electrostatic charges

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. Our MOS devices **can** be damaged if the following precautions are not taken.

Work station

Figure 5 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material.

The following precautions should be observed:

- Persons at a work bench should be earthed via a wrist strap and a resistor
- All mains-powered electrical equipment should be connected via an earth leakage switch
- Equipment cases should be earthed
- Relative humidity should be maintained between 50 and 65%
- An ionizer should be used to neutralize objects with immobile static charges.

Receipt and storage

MOS devices are packed for dispatch in antistatic conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any MOS devices that are stored temporarily

should be packed in conductive or antistatic packing or carriers.

Assembly

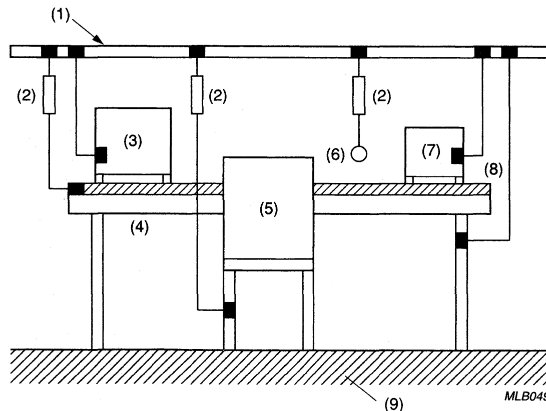
MOS devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the MOS devices are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards containing MOS devices should be handled in the same way as unmounted MOS devices. They should also carry warning labels and be packed in conductive or antistatic packing.



(1) Earthing rail.
(2) Resistor (500 kΩ ± 10%, 0.5 W).
(3) Ionizer.
(4) Work bench.
(5) Chair.
(6) Wrist strap.
(7) Electrical equipment.
(8) Conductive surface/antistatic sheet.
(9) Antistatic floor.

Fig.5 Protected work station.

IDEAS FOR DESIGN

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Printed circuit board heatsink area for surface-mount packages	36

POWER/BATTERY SWITCHING USING VD-MOS FETS

A Power switch can be used to disconnect a load during a period of non use. The load may be anything from a light bulb, an electronic valve, a stepper or brush motor to electronic components in a lap top computer that is not in use all the time. There is a choice between a low-side switch (LSS) located between the load and the power supply return, and a high-side switch (HSS), between the load and the power supply return. With an LSS the control is referenced to ground, whilst with an HSS the control is referenced to V_{DD} (see Fig.1). This makes the control for an HSS more complicated than for an LSS, and the design is more expensive and has a higher risk.

For power switching purposes MOSFETs have some important advantages over bipolar transistors. Firstly they are voltage controlled instead of current controlled, and secondly they have no thermal runaway or secondary breakdown. This is due to the fact that a MOSFET has a negative temperature coefficient of drain current, while a bipolar transistor has a positive temperature coefficient of collector current. Also the on-resistance of the FET can be reduced simply by connecting two or more in parallel.

Although more expensive, an HSS may perform better during fault conditions. The most probable fault that will occur is a short from the output of the switch to ground. Since most environments are connected to ground, damage to the output wire of the switch may be sufficient for an output short to ground to cause the load to remain active. In the case of an HSS the short will be across the load, thus preventing its activation.

It is often required to control power switches from the output of digital logic. The most common logic families use levels of +2.4 V (TTL) or +5 V (CMOS). Figures 2 to 5 illustrate how to switch loads from these logic levels. In Fig.2 the 2.4 volt gate drive will fully turn on a MOSFET with a gate-source threshold voltage (VGS_{th}) of less than 1.5 V. However, when using a FET with VGS_{th} of less than 3 V (see Fig.3), a gate pull-up resistor connected to +5 V is necessary to generate a full 5 volt swing from the TTL output. Using CMOS levels makes life easier. Since these levels equal the V+ and V− values, a MOSFET is simply chosen with a VGS_{th} somewhere between V+ and V−.
If the load is returned to ground, a P-channel FET is recommended (see Fig.4), or N-channel (see Fig.5) otherwise.

If the load is inductive, the use of a series gate resistor is recommended, as the drain-gate capacitance of the FET could couple inductive transients of the load back to the delicate logic circuitry.

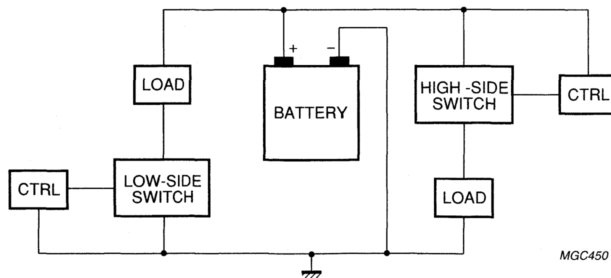


Fig.1 Power/Battery switching using VD-MOS FETs circuit diagram.

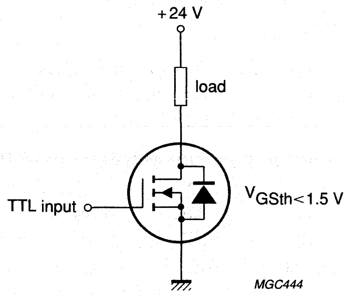


Fig.2 Low threshold N-channel VD-MOS FET switching with TTL levels.

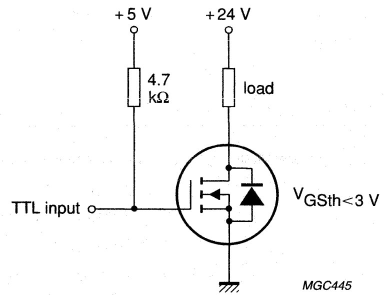


Fig.3 Low threshold N-channel VD-MOS FET switching with TTL levels using a pull-up resistor.

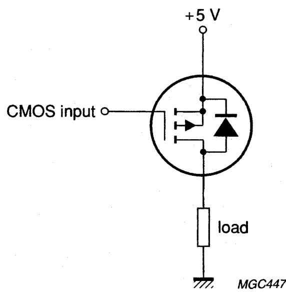


Fig.4 P-channel VD-MOS FET switching with CMOS levels.

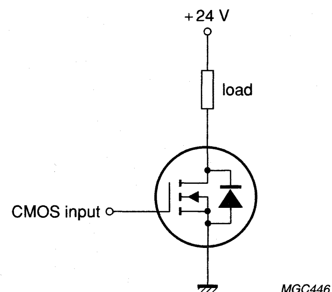


Fig.5 N-channel VD-MOS FET switching with CMOS levels.

DRIVERS FOR BRUSHLESS DC MOTORS

Brushless DC motors normally have a permanent magnet rotor and a wire-wound stator. They are very efficient and provide rapid acceleration, high speed, and smooth, quiet operation. The current to the stator coils is switched electronically as shown in Fig.6 and the switches are arranged in three half-bridge configurations to allow current flow in both directions.

In this example, the complementary P and N channel VD-MOS FETs are shown, but it is also possible to use only N channel switches, depending on the control circuitry. The PHILIPS Integrated Circuit TDA5142T has been chosen as the controller, and three of the PHC21025 MOSFETs (one 100 mΩ N-channel and one 250 mΩ P-channel type in a SO8 package) as motor drivers. These FETs can drive motors that require currents of up to 4 A (when soldering point temperature of drain pins does not exceed 80 °C) with gate drive coming directly from the IC.

A characteristic of inductive loads (such as stator windings) is the flyback energy that occurs when the drive current through a winding is switched off. This energy needs to be absorbed by the intrinsic source-drain diode of the FET. The flyback current is equal to the motor current, which is at a maximum during acceleration and (active) braking. The flyback power is the product of both this current and the forward voltage drop over the diode, and of the duty cycle which in turn depends on the inductance of the windings. This dissipation is a substantial part of the total dissipation.

We can take a practical example and calculate the power dissipation of the intrinsic diodes during flyback, and the FETs when in the 'on' state.

Assume that we have a motor with 6000 rpm (100 rps) and 6 pole-pairs (600 'electrical' rps). The period time for one 'electrical revolution' is 1.667 ms. In each 'electrical revolution' all of the six FETs are switched, giving a switching frequency of 3600 Hz. A FET is therefore switching once every 278 μs, which is also the maximum time that the diode can be conducting. The FETs themselves are conducting at two periods, 278 μs and 556 μs, which is at a duty factor of 33%. The dissipation per half bridge (per SO8) is: $\{0.33 \times (I_{MOTOR})^2 \times R_{DSonP}\} + \{0.33 \times (I_{MOTOR})^2 \times R_{DSonN}\} + flyback_P + flyback_N$.

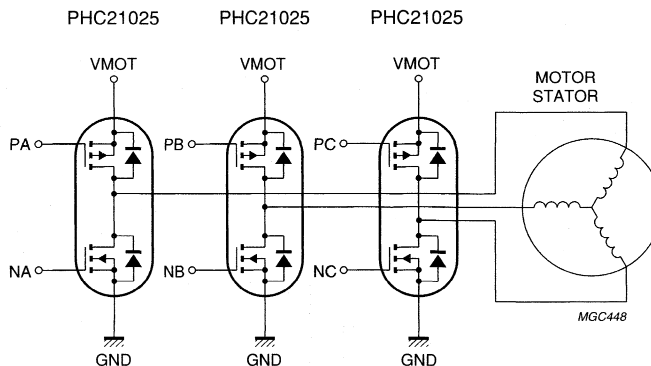


Fig.6 Drivers for brushless DC motors.

To calculate the dissipation during flyback for this example, values of 2 Ω for the ohmic resistance of the windings, and 540 μH for the inductance have been assumed. With a 12 V, 1 A motor, SPICE simulations show that the dissipation in the diode during flyback starts at 1.6 W at time zero, decreasing to 0 W after 60 μs. This is repeated every 1.667 ms and gives an average dissipation of 29 mW. The dissipation in the N-channel FET is 33 mW and in the P-channel FET 83 mW. This gives a total dissipation of 174 mW, of which 58 mW (33%) is in the diodes and cannot be neglected.

During acceleration and (active) braking, the motor current is much higher than during normal operation, and a current limiter may be necessary. The circuit design must be based on this higher current, because acceleration may last for up to a few seconds, long enough to heat up the FETs. During flyback, not only is the current much higher but it also lasts longer. In the simulation example, if the motor current is increased to 3 A, the flyback will last for 120 μs. The diode forward voltage will also be higher at this current level, and for one SO8 package the total dissipation increased to 1.5 W.

USING THE PHN708 AND PHN405 IN HARD DISK DRIVES

Philips Semiconductors has introduced two low-ohmic VD-MOS FET arrays, which are primarily designed for use in hard disk drives. Together with the demand for ever increasing storage capacity and decreasing access times of hard disk drives, also the problems for the design engineers are increasing.

The table below shows what solution we offer for these problems.

For high- and mid-end drives, market developments show a clear trend of moving the power stages from inclusion onto the controller ICs to external discrete field effect transistors.

With the introduction of the two new VD-MOS FET arrays, Philips Semiconductors now offers a cost effective and highly integrated solution to the requirements for external power stages, using up to 35% less printed circuit board area compared with a solution using five or six SO8 packages.

The key feature in the design of these new arrays is that they contain seven (PHN708) or four (PHN405) separate pieces of silicon in one package.

PHN708 – power stage for spindle drive

The PHN708 is an array with seven N-channel FETs, with a maximum on-resistance of 80 mΩ for each FET, and is intended to drive a spindle motor. The maximum drain-source voltage is 30 V, so both 5 and 12 V motors can be used.

The FETs are configured as shown in Fig.7. Six of them form three half-bridges, needed to drive a three-phase brushless DC motor. The seventh is a so called 'isolation transistor', supplying the power to the half-bridges. This transistor can also be used for the break-function. This of course depends on the controller IC that is used. Together with Philips Semiconductors' TDA5149 combined spindle and voice coil motor controller, a complete solution for spindle-motor drives is provided. (See Fig.8.)

The PHN708 comes in a surface-mount SSOP24 package.

Table 1 Hard disk system design considerations

REQUIREMENT	IMPLEMENTATION	PROBLEM	SOLUTION
decreased seek time regarding actuator arm movement	more power in voice coil motor driver stage	controller chip runs too hot	external VD-MOS FET array
decreased seek time regarding rpm	more power in spindle driver stage	controller chip runs too hot	external VD-MOS FET array
faster acceleration and deceleration	more power in spindle driver stage	controller chip runs too hot	external VD-MOS FET array
increased form-factor	more power in spindle driver stage	controller chip runs too hot	external VD-MOS FET array
increased number of platters	more power in spindle driver stage	controller chip runs too hot	external VD-MOS FET array
controlled temperature	less resistance in the circuit	larger MOSFETs required	external VD-MOS FET array
minimal board space	smaller or fewer packages	replacement required for single or dual external FETs	external VD-MOS FET array

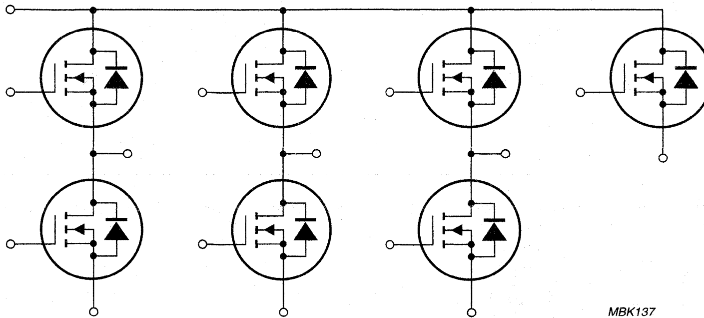


Fig.7 PHN708 FET array.

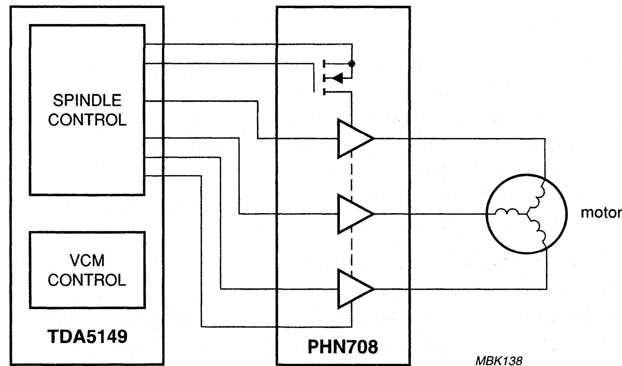


Fig.8 Typical PHN708 spindle motor drive application.

PHN405 – power stage for voice coil motor control

The PHN405 consists of four 50 mΩ max N-channel FETs, two of which have current-sense capability. It is designed for driving voice coil motors. The maximum drain-source voltage is 30 V.

The FETs are configured as shown in Fig.9. The top two FETs have shared drain terminals, while the bottom two FETs have all terminals available to the outside world. To obtain the required accuracy to position the read/write heads of the drive, it is necessary to monitor the current flowing through the motor for each stage. Conventional solutions require series resistors, which are controversial as they need to have a very low resistance value for reasons of power dissipation. Yet they can't be too small because this would produce a too small reference signal for feedback. These contradicting design requirements were solved by using the top two FETs as 'senseFETs', in fact current mirrors, that represent the current through the voice coil motor in a ratio of 1:36.

The PHN405 comes in a surface-mount SSOP16 package.

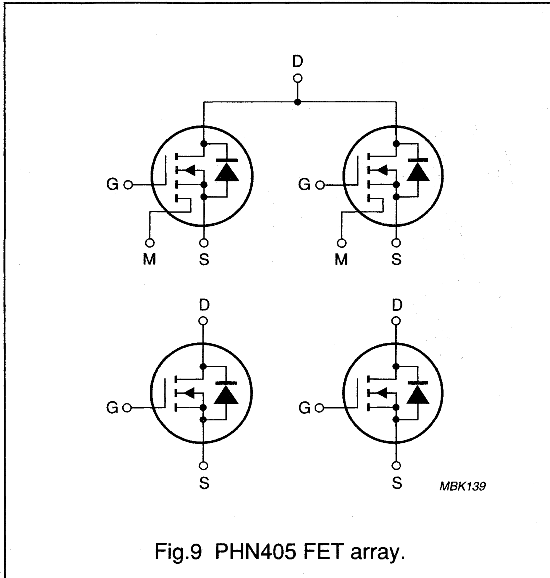


Fig.9 PHN405 FET array.

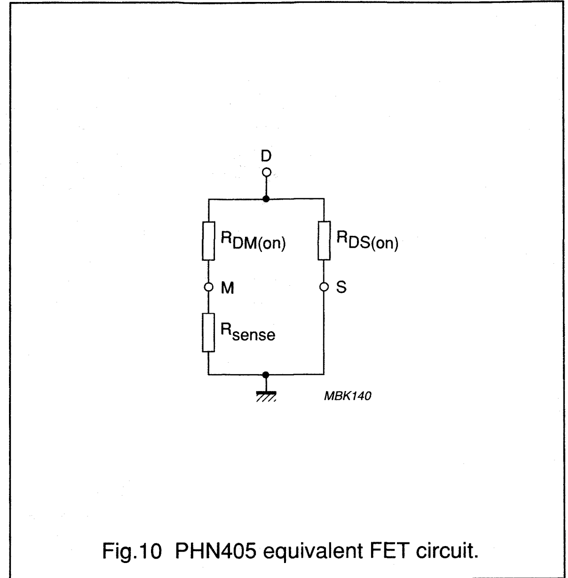


Fig.10 PHN405 equivalent FET circuit.

Current monitoring using senseFETs

Current sensing is often done by means of an external resistor, which is rather expensive due to its required 1-2% accuracy. Also, sensing of the voltage drop would require two extra IC pins and causes performance loss due to the added power dissipation in the resistor. SenseFETs are a better alternative, effectively eliminating all of these problems at the expense of less than 3% more silicon.

A senseFET is a MOSFET that splits the load current into a power and a sense component. In the PHN405, the current ratio is 36 to 1. It is important to know that this ratio is only valid for the condition where the source (S) and monitor (M) terminals are at the same voltage level. If this is not the case, the accuracy of the ratio will decrease, as is explained below.

Think of the FET as a voltage-controlled resistor between drain (D) and source (S) respectively monitor (M) terminals. The equivalent resistance model is shown in Fig.10.

The voltage drop across the sense resistor is:

$$V_{sense} = R_{sense} \times \frac{I_D \times R_{DS(on)}}{R_{DM(on)} + R_{sense}}$$

If $R_{sense} \gg R_{DM(on)}$ then $V_{sense} = I_D \times R_{DS(on)}$.

This is the maximum sense voltage that can be obtained.

Applying these formulas to the PHN405:

$V_{sense\ max} = 5 \times 0.05 = 0.25$ V, and

$$R_{sense\ max} = \frac{V_{sense\ max}}{I_{sense}} = \frac{0.25}{5 \div 36} = 1.8\ \Omega$$

This is the same value as $R_{DM(on)}$.

Due to the addition of R_{sense}, the current ratio will be:

$$n' = \frac{R_{DM(on)} + R_{sense}}{R_{DS(on)}} \text{ instead of } n = \frac{R_{DM(on)}}{R_{DS(on)}}$$

The values of both $R_{DM(on)}$ and $R_{DS(on)}$ are temperature dependent, and because the currents are different, also the temperatures will be different.

The total accuracy of the system depends on the value of R_{sense}. If R_{sense} is kept smaller than $R_{DM(on)}$, then an overall accuracy of 5% is achieved. However, if direct current sensing is used, meaning that no sense resistor is used, while keeping the M and S pins at the same voltage level, an overall accuracy of 2% is achieved. This can easily be implemented with today's controller ICs using an op-amp to detect the voltage difference. The voltage difference is compensated with a voltage or current source.

SIREN DRIVER CIRCUIT FOR CAR ALARMS

Figure 11 shows a siren driver circuit created with VD-MOS FETs. Power is supplied by a 12 V battery, and the driver inputs are complementary pulse waveforms from a microprocessor.

Chosen for our example are two BSN20 VD-MOS FETs in small SOT23 packages and two PHC21025, each comprising two FETs in one SO8 package. In its minimum configuration the circuit requires six components (excluding the speaker) and its maximum configuration is eight components. All components can be surface mounted.

The two push-pull stages X2/X3 and X5/X6 drive the speaker directly. Either X2 and X6 are conducting or X5 and X3, reversing the current through the speaker. Driver stages X1 and X4 convert the 5 V input swing from the microprocessor to the 12 V switching level.

During microprocessor reset and with no alarm, both driver input pins must have the same potential. (0 or 5 V; 0 V is preferred). With the FETs X1 and X4 not conducting, the gates of FETs X2, X3, X5 and X6 will be high, and X2 and X5 will be conducting, resulting in no current through the speaker. When driver inputs are pulsed (complementary), almost the full 12 V is switched over the speaker (a little less due to the on-resistance of the push-pull FETs 100 mΩ N-channel and 250 mΩ P-channel).

When designing this siren driver circuit, take the following into account. The BSN20 (X1 and X4) have an input threshold between 0.4 and 1.8 V. The value of the pull-up resistors R1 + R3 and R2 + R4 must be as small as possible (but not less than 280 Ω) to achieve the highest possible switching speed, and to guarantee a voltage level at the gates of X2 and X5 less than 0.8 V. R3 and R4 are optional, but may be necessary to reduce high through-current in the push-pull stages. When using these resistors however, the gate voltage at X3 and X6 will not fully reduce to 0.8 V, which can influence the on-resistance of these FETs and consequently the dissipation when conducting. When using R3 and R4, the values of R1 and R2 need to be adjusted to maintain the 280 Ω.

Concerning the dissipation in the push-pull stage, the on-resistance of the FETs increases by a factor of 1.7 when operating at 150 °C junction temperature. For the P-channel, which dissipates the most, this means that the on-resistance increases to 425 mΩ. If a 4 Ω speaker is used, the maximum current will be 2.6 A at 12 V. If the pulse is symmetrical and the duty cycle is 50%, the dissipation in the P-channel FET will be 1.45 W. Note that the temperature at the soldering point of the drain pins must not exceed 80 °C.

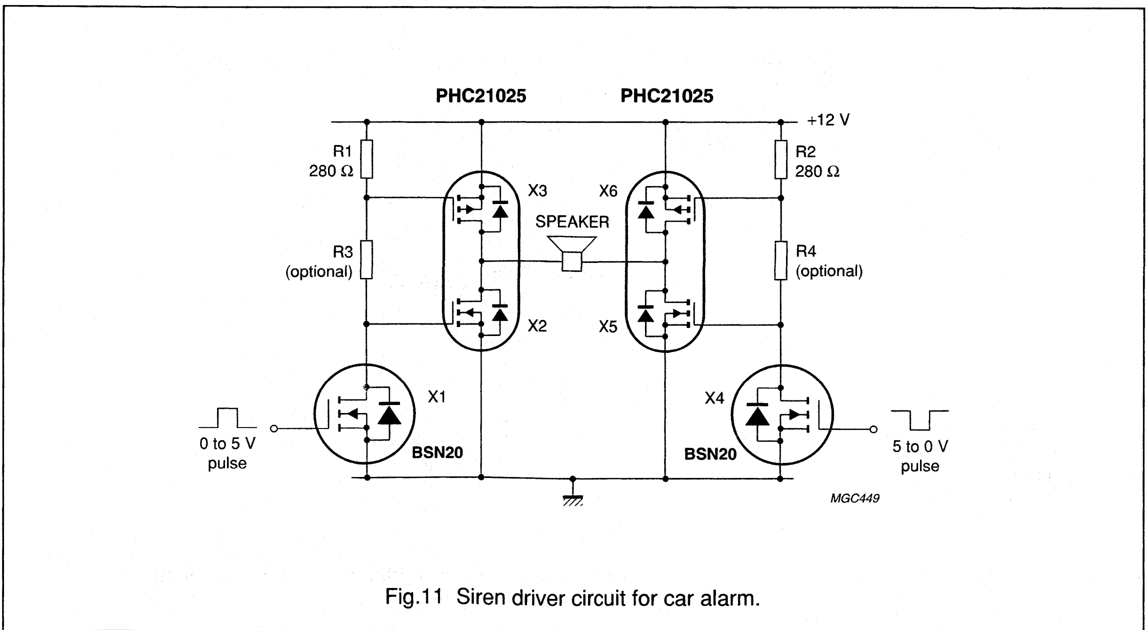


Fig.11 Siren driver circuit for car alarm.

PRINTED CIRCUIT BOARD HEATSINK AREA FOR SURFACE- MOUNT PACKAGES

When using surface mount components, it is not as easy to dissipate heat in clip-on or bolt-on heatsinks than with through-hole components. With surface mount components, the conductive tracks or pads on the printed-circuit board are often the only means to transfer heat away from the component.

The amount of heat sink area required for the BSP100 type in a SOT223 package can be calculated as follows. This type has been selected as an example for a design that uses a 100 mΩ, N-channel VD-MOS-FET with an I_{DS} of 3 A. The maximum operating junction temperature of this device is 150 °C. At this temperature, the on-resistance of the FET increases with a factor of 1.7 and the power dissipation in continuous use (duty factor 100%) is 1.53 W.

If the ambient temperature is 40 °C, then the total thermal resistance (R_{th}) requirement for FET and PCB is: (150 – 40)/1.53 = 72 K/W. The thermal resistance of the FET itself is 10 K/W from junction to the soldering point of the drain tab. Therefore the requirement for R_{th} of the heatsink is 72 – 10 = 62 K/W.

Figure 12 shows typical thermal resistance from soldering point to ambient as a function of area of an epoxy printed-circuit board. The drain tab of the SOT223 is soldered in the centre of one of the sides (as shown in Fig.13). In this example curve (1) shows a single-sided and unplated copper pad area of 20 × 20 mm.

A similar calculation can be applied to the SO8 package. Using the PHN210 as an example, we have two 100 mΩ, N-channel VD-MOS FETs in one SO8 package. Taking I_{DS} = 2 A per FET and duty factor = 50%, the dissipation per FET is 0.34 W and the total for both FETs is 0.68 W. If the ambient temperature is 60 °C, then the total thermal resistance (R_{th}) requirement for FET and PCB is: (150 – 60)/0.68 = 132 K/W. For the SO8 package the R_{th} from junction to the soldering point of the drain tab is 35 K/W, so the requirement for the heat sink thermal resistance is 132 – 35 = 97 K/W. Referring again to curve (1) in Fig.12, it can be seen that 50 mm^2 is required.

This example is true for both FETs dissipating equal power. A suggested PCB design is shown in Fig.14. Here the copper is divided into two 3.5 × 7 mm rectangular portions which gives the required total heatsink area and keeps the drain connections separated.

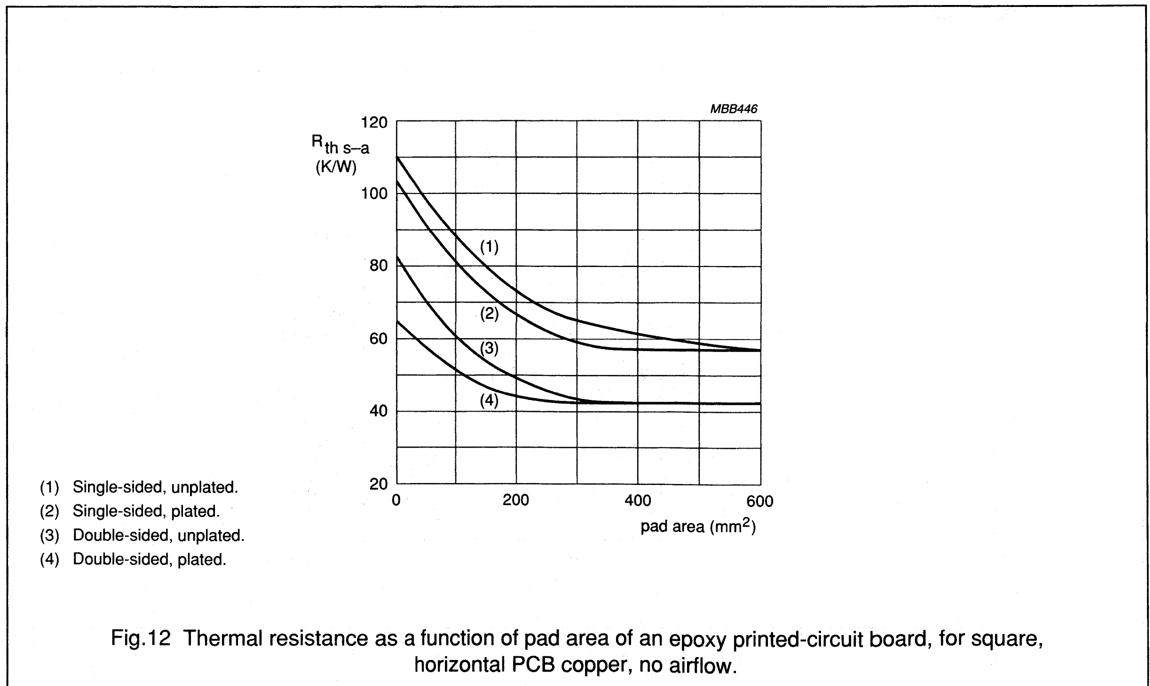


Fig.12 Thermal resistance as a function of pad area of an epoxy printed-circuit board, for square, horizontal PCB copper, no airflow.

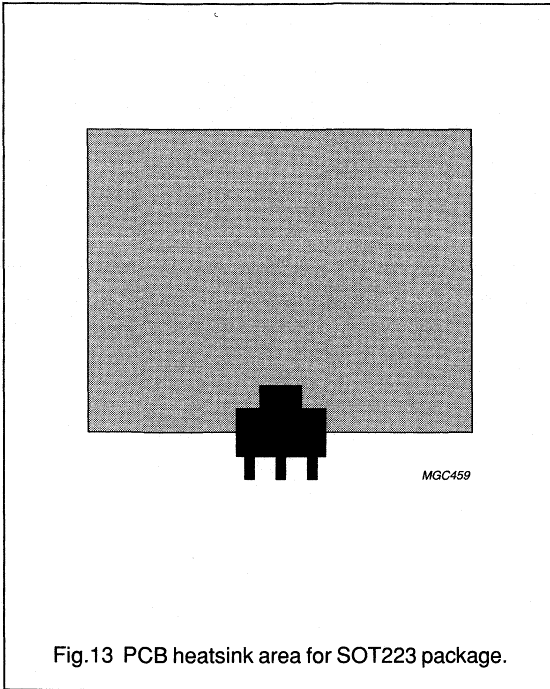


Fig.13 PCB heatsink area for SOT223 package.

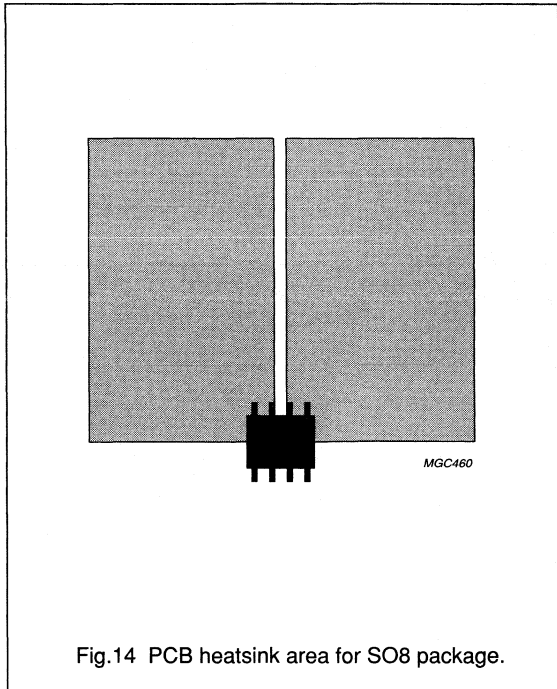


Fig.14 PCB heatsink area for SO8 package.

DEVICE DATA

in alphanumeric sequence

N-channel enhancement mode vertical D-MOS transistor

2N7000

FEATURES

- Low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use in relay, high-speed and line transformer drivers.

PINNING - TO-92 VARIANT

PIN	DESCRIPTION
1	drain
2	gate
3	source

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		60	V
I_D	drain current	DC value	280	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 500 mA V_{GS} = 10 V	5	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	3	V

PIN CONFIGURATION

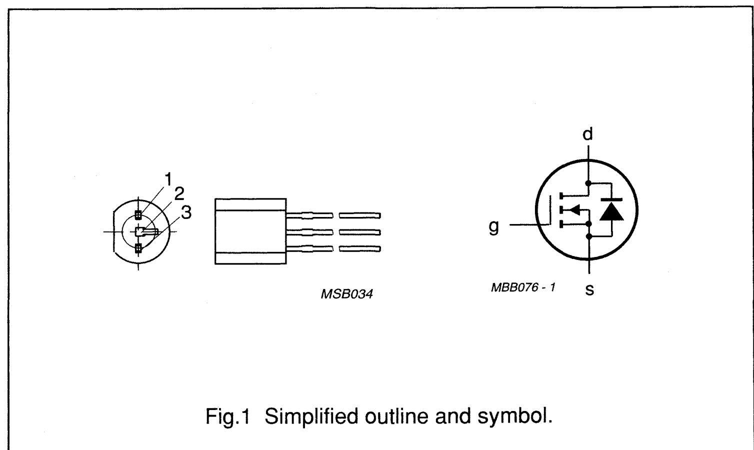


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	60	V
V_{DG}	drain-gate voltage		–	60	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	40	V
I_D	drain current	DC value	–	280	mA
I_{DM}	drain current	peak value	–	1.3	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	–	830	mW
T_{stg}	storage temperature range		–55	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	150	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	60	90	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 48 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 15 V V_{DS} = 0	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA $V_{GS} = V_{DS}$	0.8	–	3	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 500 mA V_{GS} = 10 V	–	3.5	5	Ω
		I_D = 75 mA V_{GS} = 4.5 V	–	–	5.3	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 200 mA V_{DS} = 10 V	100	200	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	25	40	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	22	30	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	6	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	4	10	ns
t_{off}	turn-off time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	4	10	ns

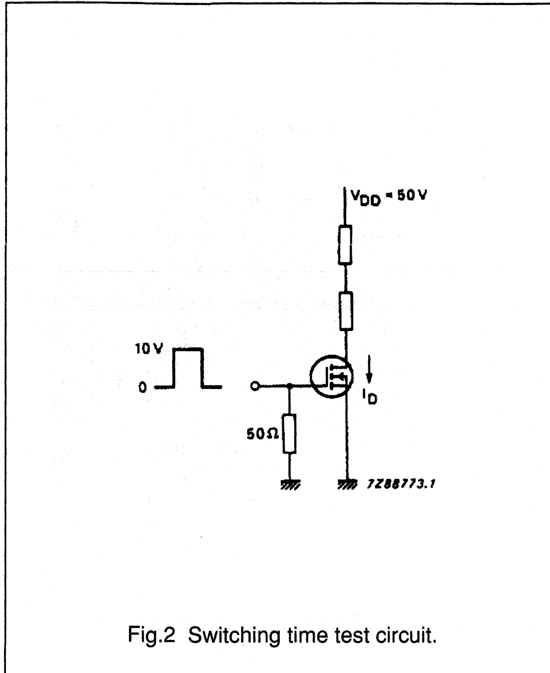


Fig.2 Switching time test circuit.

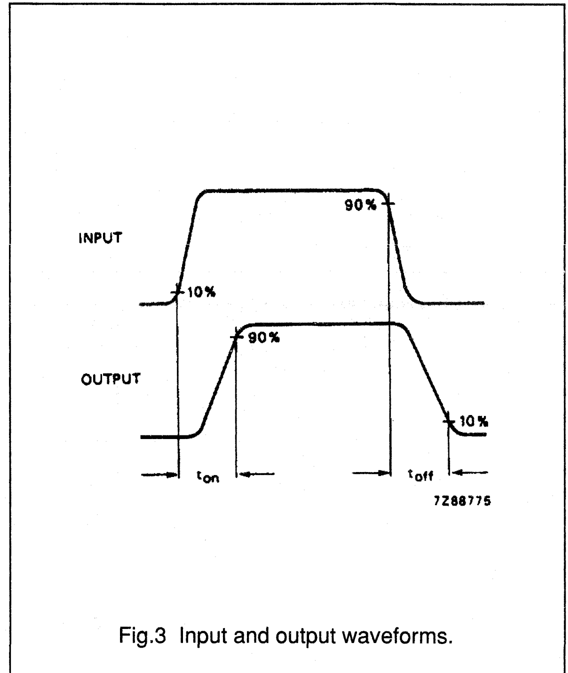


Fig.3 Input and output waveforms.

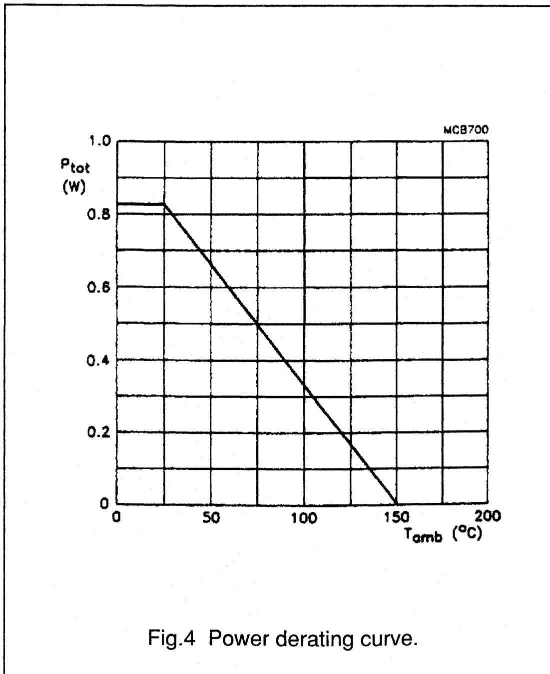


Fig.4 Power derating curve.

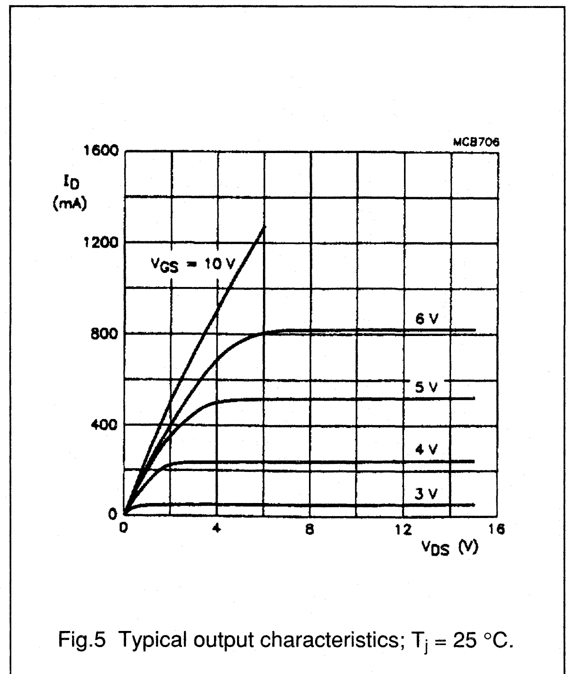


Fig.5 Typical output characteristics; T_j = 25 °C.

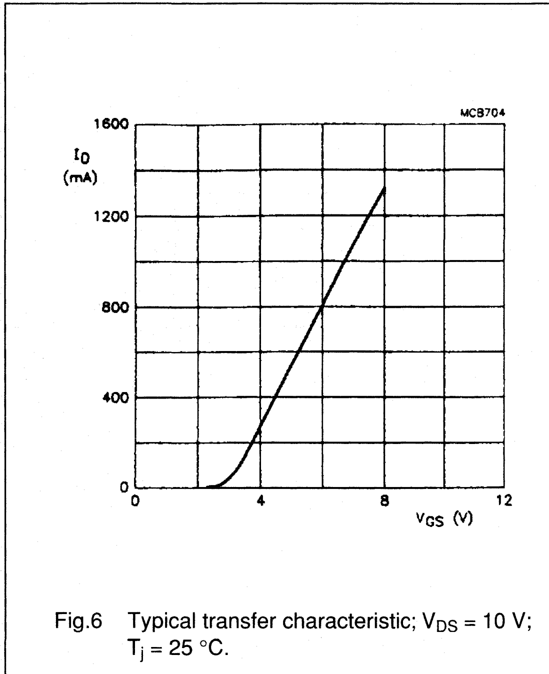


Fig.6 Typical transfer characteristic; V_{DS} = 10 V; T_j = 25 °C.

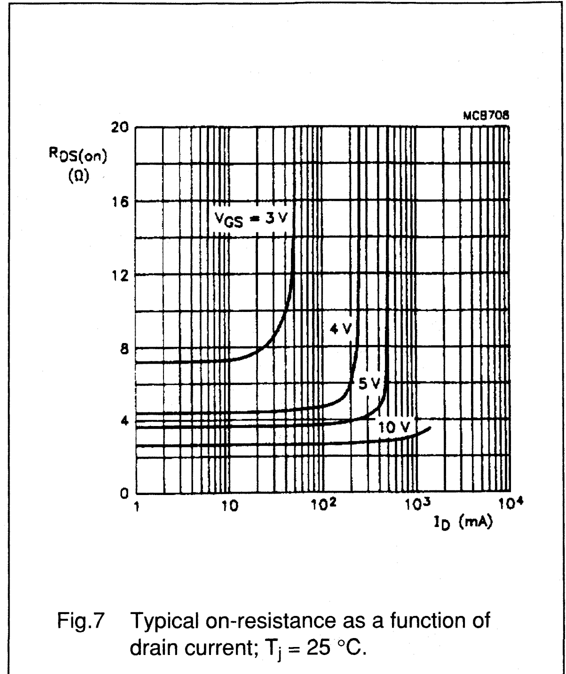


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

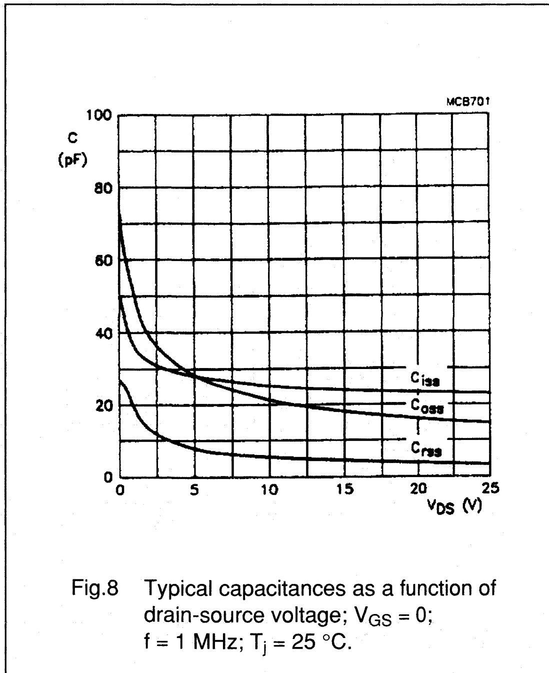
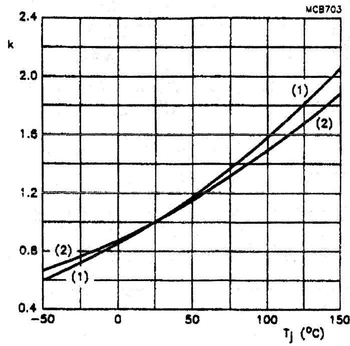


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.



(1) I_D = 500 mA; V_{GS} = 10 V.
(2) I_D = 75 mA; V_{GS} = 4.5 V.

Fig.9 Temperature coefficient of drain-source on resistance;

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C};$$

typical $R_{DS(on)}$.

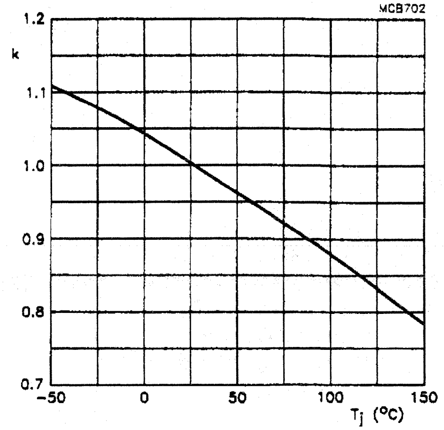


Fig.10 Temperature coefficient of gate-source threshold voltage;

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C};$$

typical $V_{GS(th)}$ at 1 mA.

N-channel vertical D-MOS transistor 2N7002

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope. It is designed for use as a Surface Mounted Device (SMD) in thin and thick-film circuits, with applications in relay, high-speed and line transformer drivers.

PINNING - SOT23

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		60	V
I_D	drain current	DC value	180	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 500 mA V_{GS} = 10 V	5	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	3	V

PIN CONFIGURATION

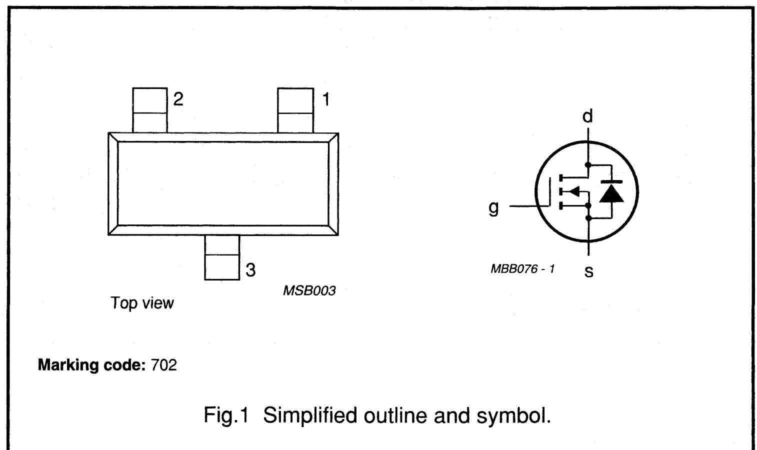


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	60	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	40	V
I_D	drain current	DC value	–	180	mA
I_{DM}	drain current	peak value	–	800	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C (note 1) (note 2)	 – –	 300 250	 mW mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Notes

1. Mounted on a ceramic substrate measuring 10 × 8 × 0.7 mm.
2. Mounted on a printed circuit board.

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	note 1 note 2	430 500	K/W K/W

Notes

1. Mounted on a ceramic substrate measuring 10 × 8 × 0.7 mm.
2. Mounted on a printed circuit board.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	60	90	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 48 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	V_{DS} = 0 $\pm V_{GS}$ = 15 V	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA $V_{GS} = V_{DS}$	0.8	–	3	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 500 mA V_{GS} = 10 V	–	3.5	5	Ω
		I_D = 75 mA V_{GS} = 4.5 V	–	–	5.3	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 200 mA V_{DS} = 10 V	100	200	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	25	40	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	22	30	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	6	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	–	10	ns
t_{off}	turn-off time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	–	15	ns

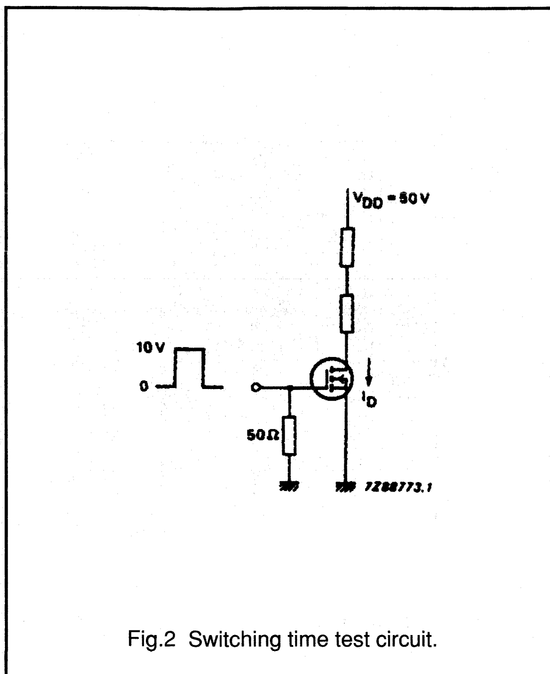


Fig.2 Switching time test circuit.

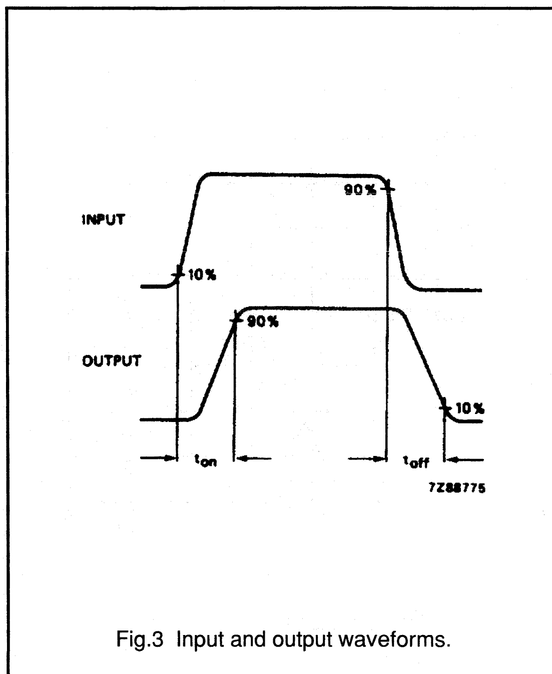
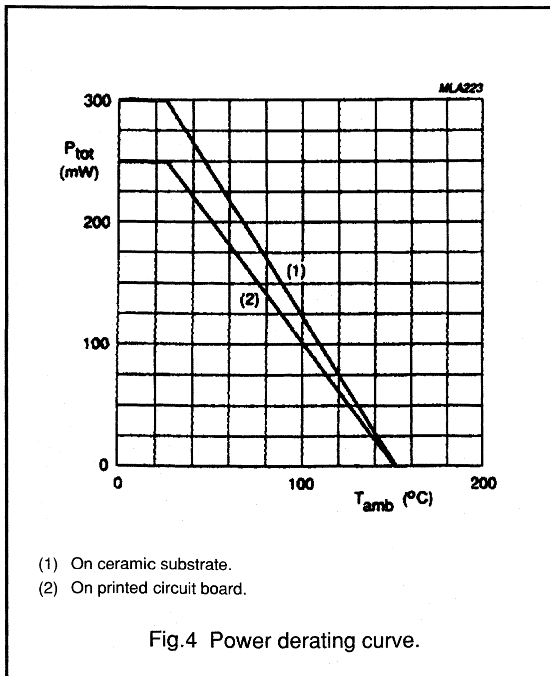


Fig.3 Input and output waveforms.



(1) On ceramic substrate.
(2) On printed circuit board.

Fig.4 Power derating curve.

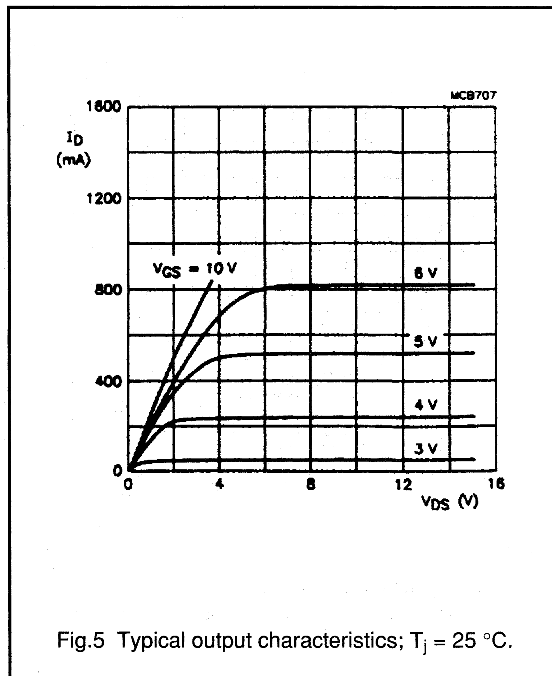


Fig.5 Typical output characteristics; T_j = 25 °C.

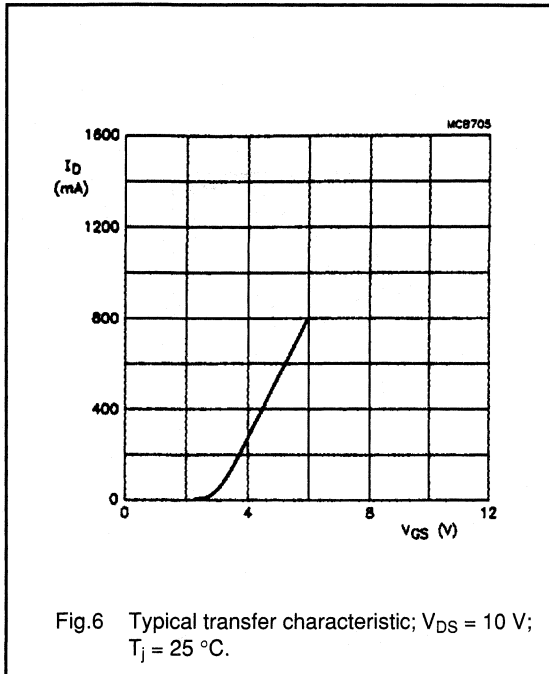


Fig.6 Typical transfer characteristic; V_{DS} = 10 V; T_j = 25 °C.

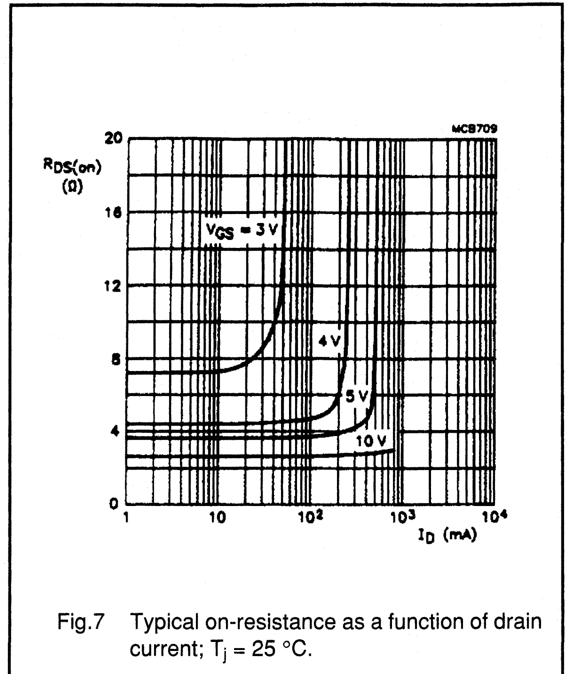


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

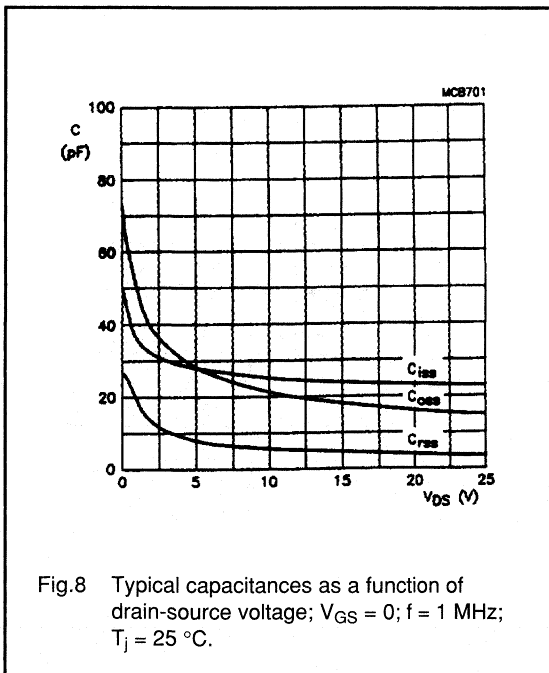
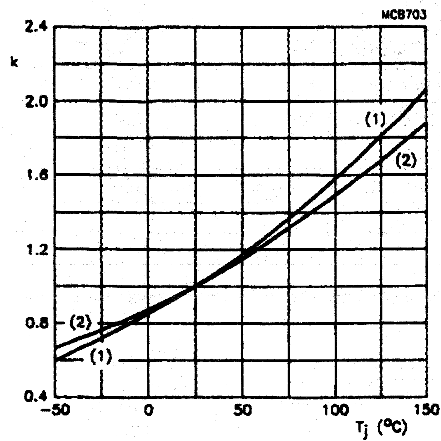


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.



(1) I_D = 500 mA; V_{GS} = 10 V.
(2) I_D = 75 mA; V_{GS} = 4.5 V.

Fig.9 Temperature coefficient of drain-source on-resistance;

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$$

typical $R_{DS(on)}$.

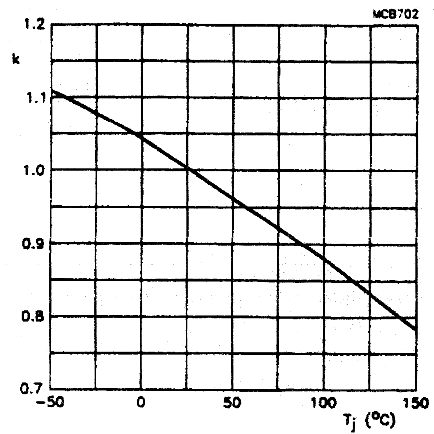


Fig.10 Temperature coefficient of gate-source threshold voltage;

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}$$

typical $V_{GS(th)}$ at 1 mA.

N-channel enhancement mode vertical D-MOS transistor

BS107

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope. Intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage (DC)	200	V
V_{GSth}	gate-source threshold voltage	2.4	V
I_D	drain current (DC)	150	mA
R_{DSon}	drain-source on-state resistance	28	Ω

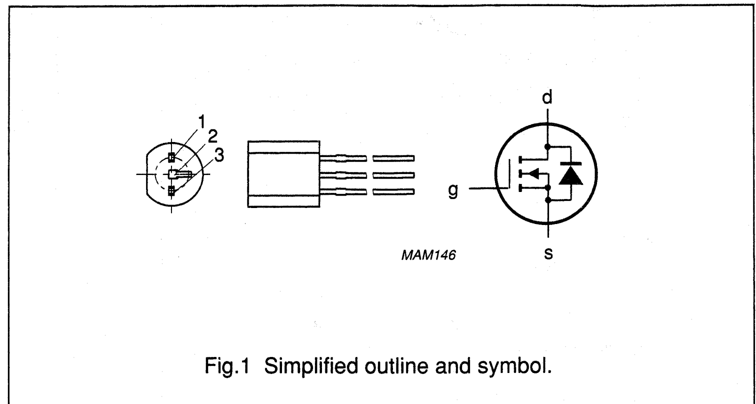


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	drain current	DC	–	150	mA
I_{DM}	drain current	peak	–	300	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	830	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	operating junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	150	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 I_D = 10 μA	200	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 130 V V_{GS} = 0	–	–	30	nA
I_{DSX}	drain-source leakage current	V_{DS} = 70 V V_{GS} = 0.2 V	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 15 V V_{DS} = 0	–	–	10	nA
$V_{GS(th)}$	gate threshold voltage	I_D = 1 mA $V_{DS} = V_{GS}$	0.8	–	2.4	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA V_{GS} = 2.6 V	–	20	28	Ω
$R_{DS(on)}$	drain-source on-resistance	I_D = 150 mA V_{GS} = 10 V	–	14	–	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA V_{DS} = 15 V	90	180	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	50	65	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	16	25	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	4	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	switching-on time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	2	10	ns
t_{off}	switching-off time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	4	20	ns

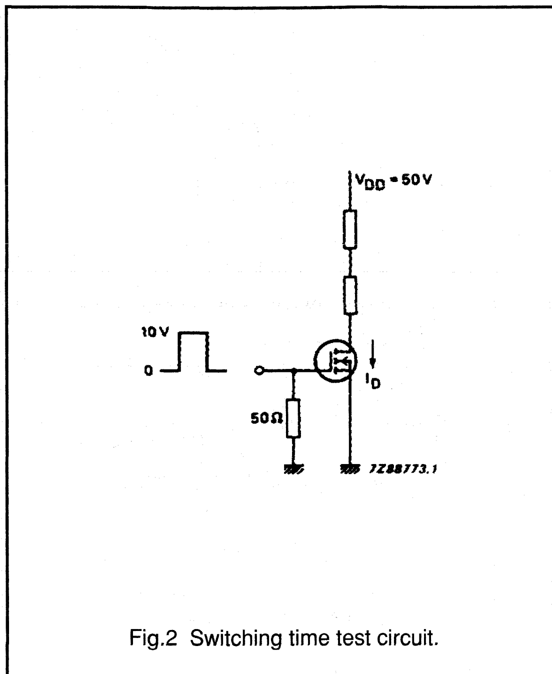


Fig.2 Switching time test circuit.

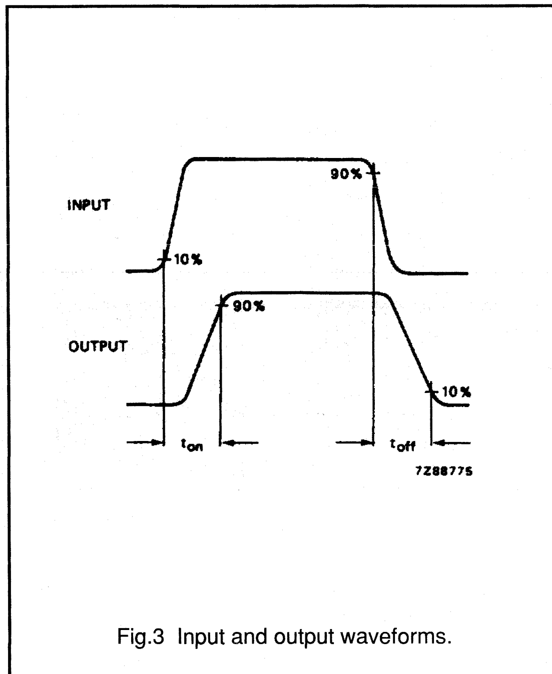


Fig.3 Input and output waveforms.

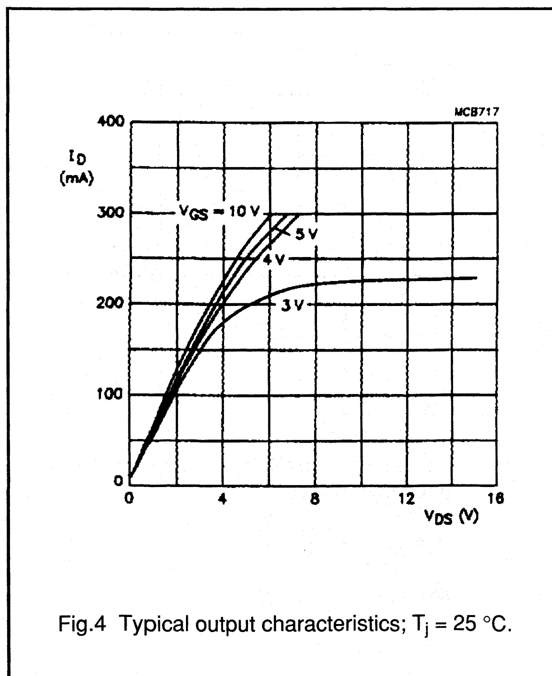


Fig.4 Typical output characteristics; T_j = 25 °C.

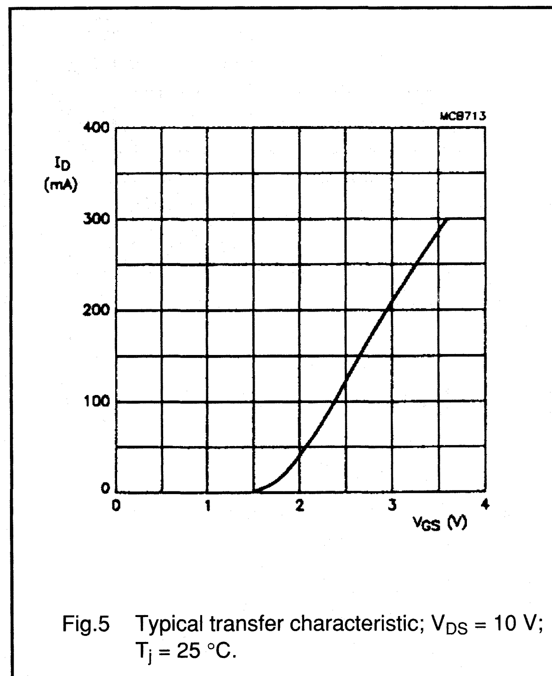


Fig.5 Typical transfer characteristic; V_{DS} = 10 V; T_j = 25 °C.

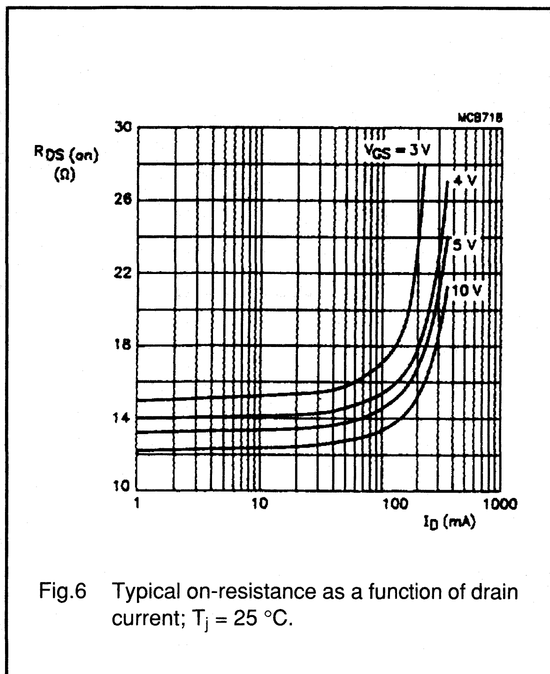


Fig.6 Typical on-resistance as a function of drain current; T_j = 25 °C.

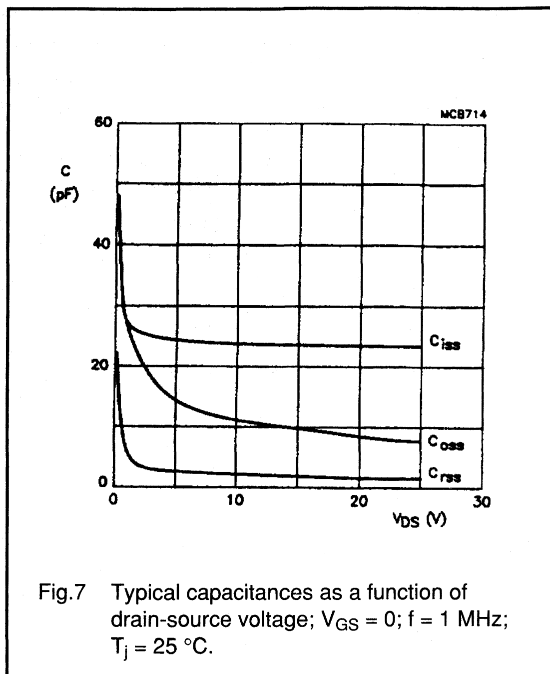
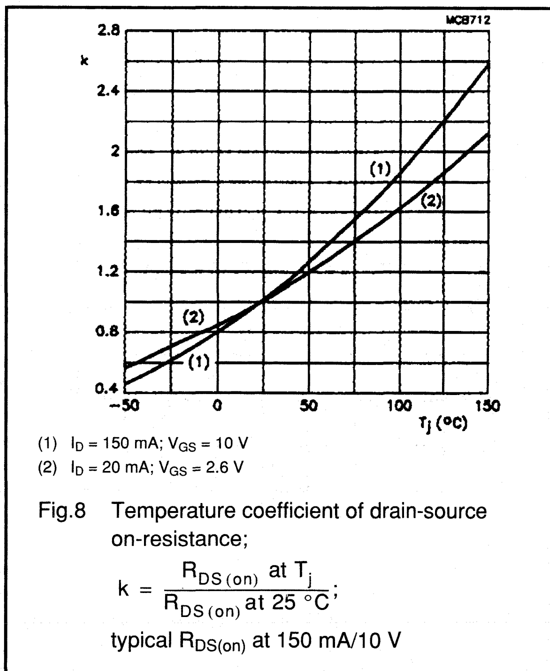


Fig.7 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.



(1) I_D = 150 mA; V_{GS} = 10 V
(2) I_D = 20 mA; V_{GS} = 2.6 V

Fig.8 Temperature coefficient of drain-source on-resistance;

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C};$$

typical $R_{DS(on)}$ at 150 mA/10 V

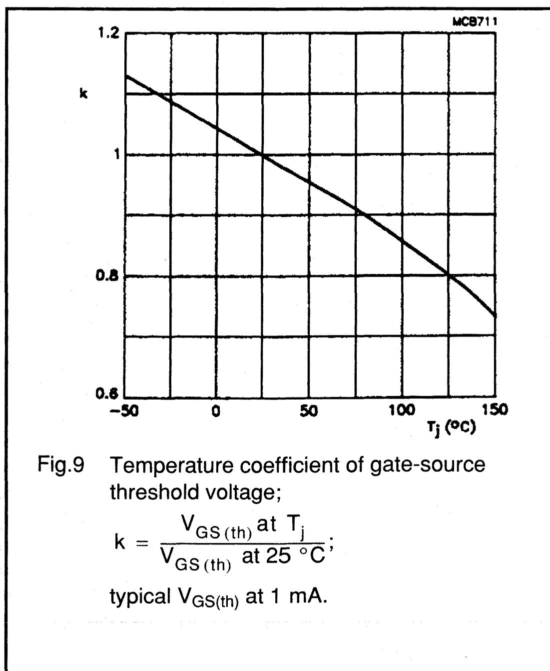


Fig.9 Temperature coefficient of gate-source threshold voltage;

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C};$$

typical $V_{GS(th)}$ at 1 mA.

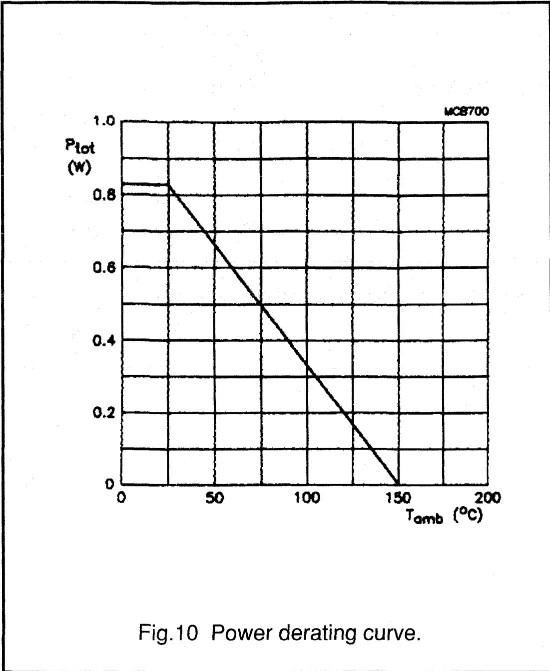


Fig.10 Power derating curve.

N-channel enhancement mode vertical D-MOS transistor

BS107A

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in TO-92 envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

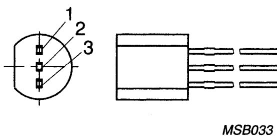
PINNING - TO-92

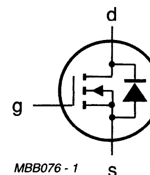
1	=	source
2	=	gate
3	=	drain

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.	0.6	W
Drain-source ON-resistance				
I_D = 250 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	4.5	Ω
		max.	6.4	Ω
Transfer admittance				
I_D = 250 mA; V_{GS} = 25 V	$\lvert Y_{fs} \rvert$	min.	200	mS
		typ.	350	mS

PIN CONFIGURATION





Note: Various pinnings are available.

Fig.1 Simplified outline and symbol.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Drain current (peak)	I_{DM}	max.	500	mA
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.	0.6	W
Storage temperature	T_{stg}		−55 to +150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for collector lead min. 10 mm × 10 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value	Unit
Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200	V
Drain-source leakage current V_{DS} = 130 V; V_{GS} = 0	I_{DSS}	max.	30	nA
Gate-source leakage current V_{GS} = 15 V; V_{DS} = 0	I_{GSS}	max.	10	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	1.0 3.0	V V
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.5 6.4	Ω Ω
I_D = 100 mA; V_{GS} = 10 V	R_{DSon}	typ. max.	4.2 6.0	Ω Ω
Transfer admittance I_D = 250 mA; V_{DS} = 25 V	$\lvert y_{fs} \rvert$	min. typ.	200 350	mS mS
Input capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ.	45	pF
Output capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ.	15	pF
Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ.	3.5	pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	typ. typ.	5 15	ns ns

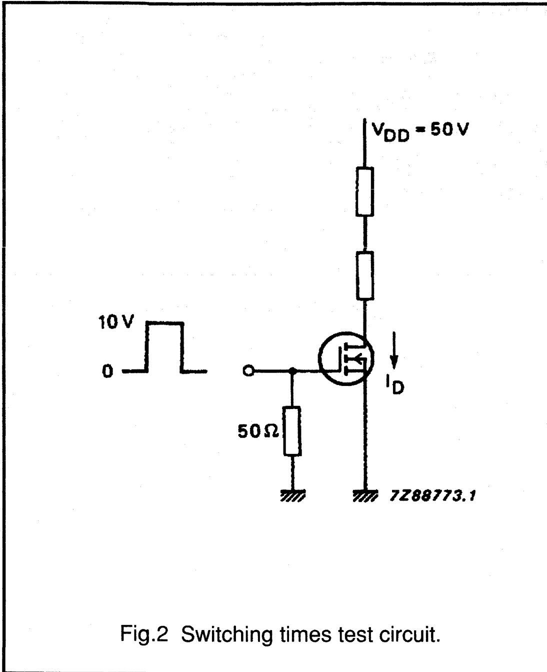


Fig.2 Switching times test circuit.

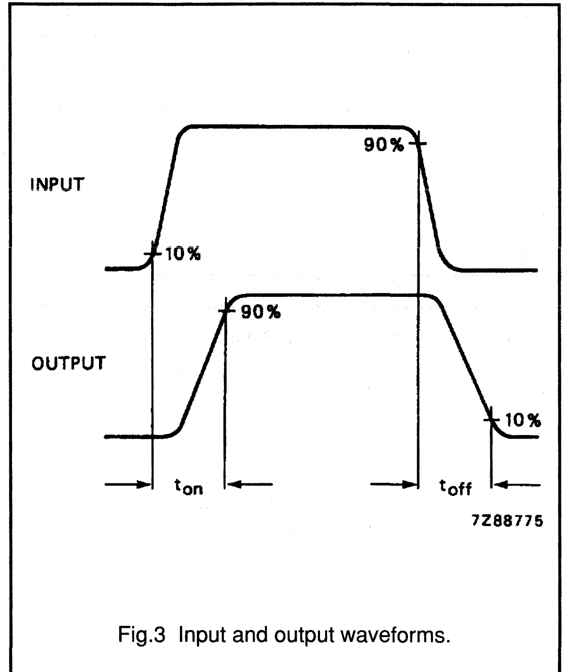


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BS108

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	200	V
I_D	DC drain current	250	mA
$R_{DS(on)}$	drain-source on-resistance	8	Ω
$V_{GS(th)}$	gate-source threshold voltage	1.8	V

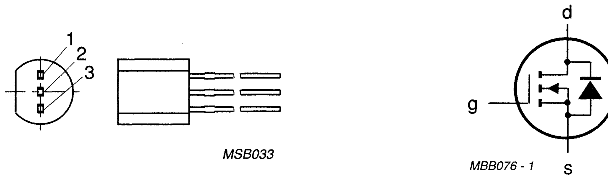


Fig.1 Simplified outline (TO-92 variant) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	250	mA
I_{DM}	peak drain current		–	1	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125 K/W

Note

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 × 10 mm

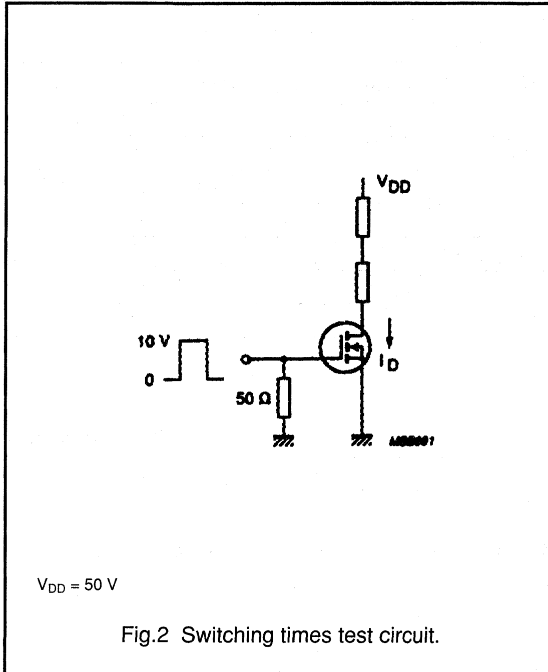
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	200	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 160 V; V_{GS} = 0	–	–	1	μA
I_{GSS}	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.4	–	1.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 100 mA; V_{GS} = 2.8 V	–	5	8	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 300 mA; V_{DS} = 25 V	200	400	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	50	80	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	5	10	pF
Switching times (see Figs 2 and 2)						
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	20	30	ns

N-channel enhancement mode vertical D-MOS transistor

BS108



V_{DD} = 50 V

Fig.2 Switching times test circuit.

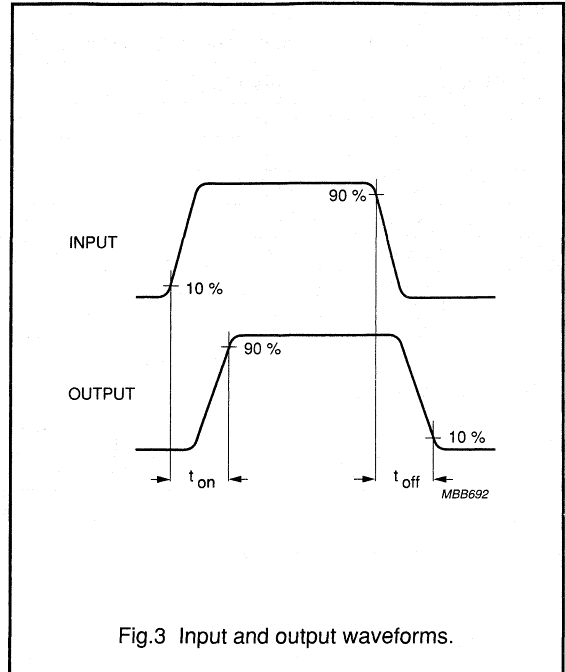


Fig.3 Input and output waveforms.

N-channel vertical D-MOS transistor BS170

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

FEATURES

- Very low $R_{DS(on)}$.
- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

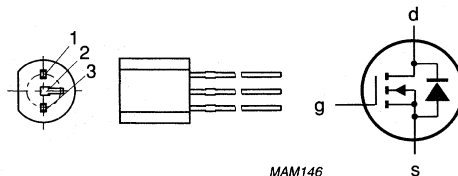
PINNING - TO-92 VARIANT

1 = source
2 = gate
3 = drain

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	60	V
Gate-source voltage	V_{GS}	max.	15	V
Drain current (DC)	I_D	max.	500	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	830	mW
Junction temperature	T_j	max.	150	°C
Drain-source ON-resistance				
V_{GS} = 10 V; I_D = 200 mA	$R_{DS(on)}$	max.	5	Ω

PIN CONFIGURATION



Note: Various pin configurations available.

Fig.1 Simplified outline and symbol.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Parameter	Symbol		Value	Unit
Drain-source voltage	V_{DS}	max.	60	V
Drain-gate voltage	V_{DG}	max.	60	V
Gate-source voltage	V_{GS}	max.	15	V
Drain current (DC) at T_c = 25 °C	I_D	max.	500	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	830	mW
Storage temperature range	T_{stg}		–55 to +150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

Parameter	Symbol		Value	Unit
From junction to ambient	$R_{th\ j\text{-}a}$	=	150	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value	Unit
Drain-source breakdown voltage V_{GS} = 0; I_D = 100 μA	$V_{(BR)DS}$	min.	60	V
		typ.	90	V
Gate threshold voltage V_{GS} = V_{DS}; I_D = 1 mA	$V_{GS(th)}$	min.	0.8	V
		max.	3.0	V
Gate-source leakage current V_{GS} = 15 V; V_{DS} = 0	I_{GSoff}	max.	10	nA
Drain cut-off current V_{DS} = 25 V; V_{GS} = 0	I_{DSS}	max.	0.5	μA
Drain-source ON-resistance (note 1) V_{GS} = 10 V; I_D = 200 mA	$R_{DS(on)}$	typ.	2.5	Ω
		max.	5.0	Ω
Forward transconductance (note 1) V_{DS} = 10 V; I_D = 200 mA; f = 1 kHz	g_{fs}	typ.	200	mS
Capacitances at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ.	25	pF
		max.	40	pF
	C_{os}	typ.	22	pF
		max.	30	pF
	C_{rs}	typ.	6	pF
		max.	10	pF
Switching times at I_D = 200 mA I_D = 200 mA; V_{DS} = 50 V;	t_{on}	typ.	4	ns
		max.	10	ns
V_{GS} = 0 to 10 V	t_{off}	typ.	4	ns
		max.	10	ns

Note

1. t_p = 80 μs; δ = 0,01.

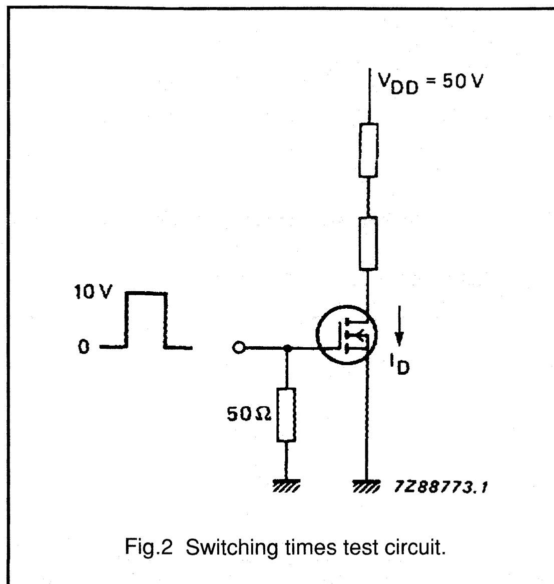


Fig.2 Switching times test circuit.

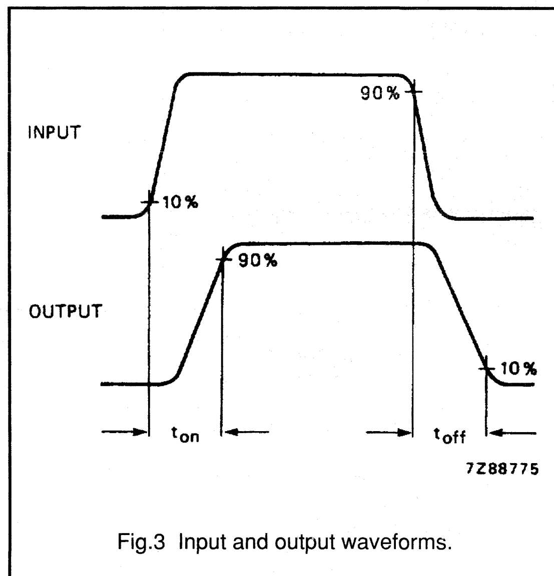


Fig.3 Input and output waveforms.

P-channel enhancement mode vertical D-MOS transistor

BS208

FEATURES

- Direct interface to C-MOS
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a TO-92 envelope. Intended for use in relay, high-speed and line transformer drivers.

PINNING - TO-92

PIN	DESCRIPTION
1	source
2	gate
3	drain

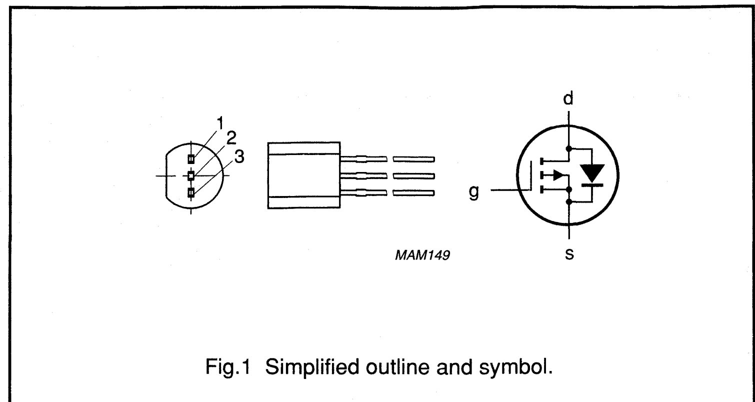


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–	–200	V
V_{GSO}	gate-source voltage (DC)	open drain	–	–	±20	V
$\|Y_{fs}\|$	forward transfer admittance	I_D = –200 mA; V_{DS} = –25 V	100	200	–	mS
I_D	drain current (DC)		–	–	–0.2	A
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = –10 V; I_D = –200 mA	–	10	14	Ω
P_{tot}	total power dissipation	T_{amb} = 25 °C	–	–	0.83	W

P-channel enhancement mode vertical D-MOS transistor

BS208

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$-I_D$	drain current	DC	–	0.2	A
$-I_{DM}$	drain current	peak value	–	0.6	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	–	0.83	W
T_{stg}	storage temperature range		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
R_{thj-a}	from junction to ambient	150	K/W

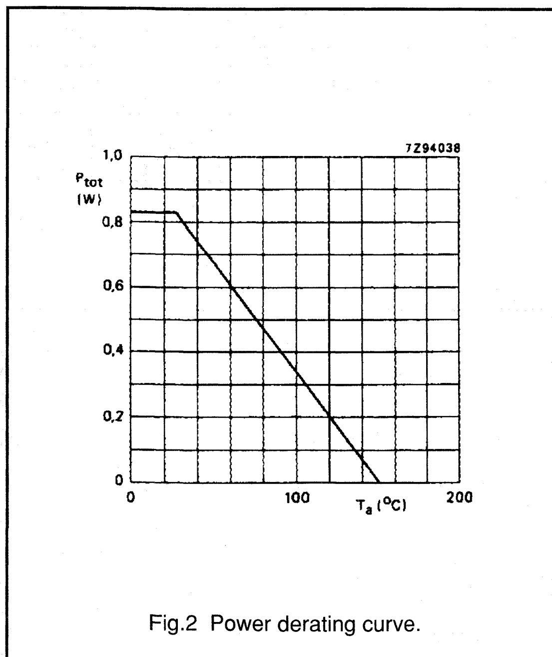


Fig.2 Power derating curve.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-V_{GS}$ = 0 $-I_D$ = 10 μA	200	–	-	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 130 V V_{GS} = 0	–	–	1	μA
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 70 V $-V_{GS}$ = 0.2 V	–	–	25	μA
$-I_{GSS}$	gate-source leakage current	$-V_{GS}$ = 20 V V_{DS} = 0	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$V_{GS} = V_{DS}$ $-I_D$ = 1 mA	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-V_{GS}$ = 10 V $-I_D$ = 200 mA	–	–	14	Ω
$\|Y_{fs}\|$	transfer admittance	$-V_{DS}$ = 25 V $-I_D$ = 200 mA	100	200	–	mS
C_{iss}	input capacitances	note 1	–	55	90	pF
C_{oss}	output capacitance	note 1	–	20	30	pF
C_{rss}	feedback capacitance	note 1	–	5	15	pF
t_{on}	turn-on time	note 2	–	5	10	ns
t_{off}	turn-off time	note 2	–	20	30	ns

Notes

1. Measured at f = 1 MHz; $-V_{DS}$ = 25 V; V_{GS} = 0.
2. $-V_{GS}$ = 0 to 10 V; $-I_D$ = 250 mA; $-V_{DD}$ = 50 V.

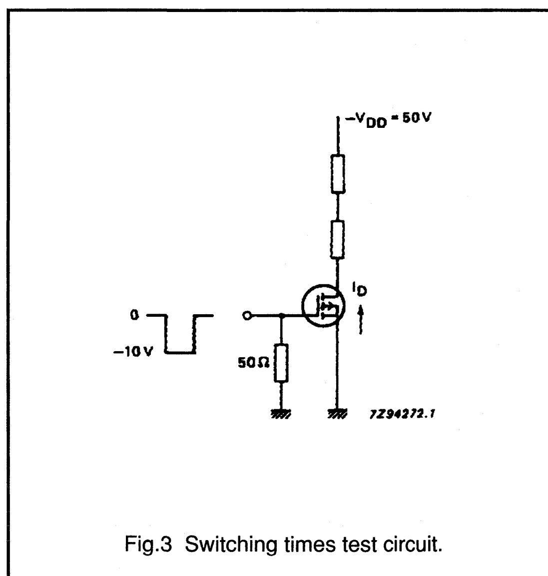


Fig.3 Switching times test circuit.

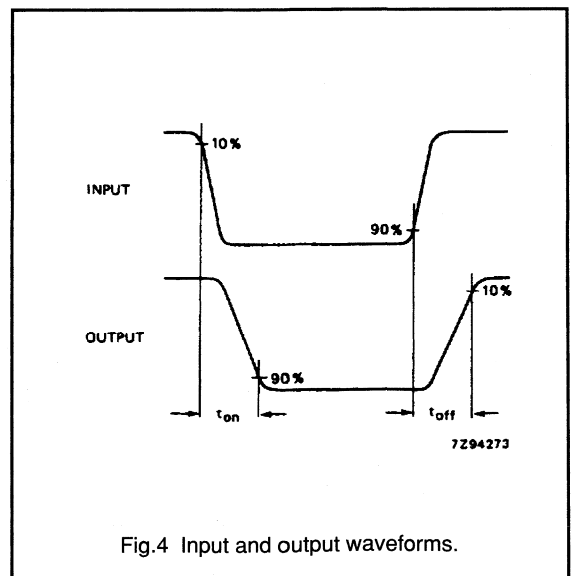


Fig.4 Input and output waveforms.

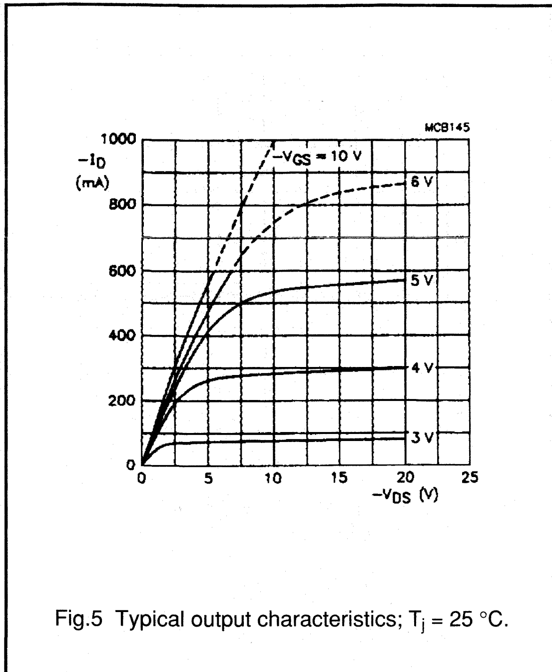


Fig.5 Typical output characteristics; T_j = 25 °C.

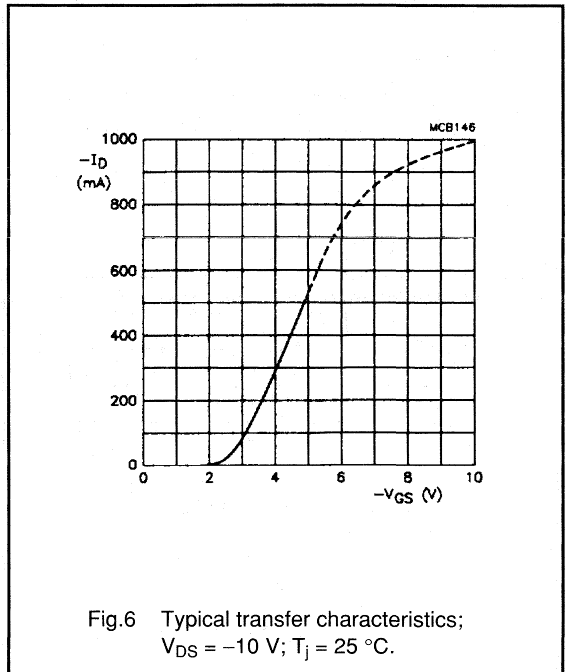


Fig.6 Typical transfer characteristics; V_{DS} = −10 V; T_j = 25 °C.

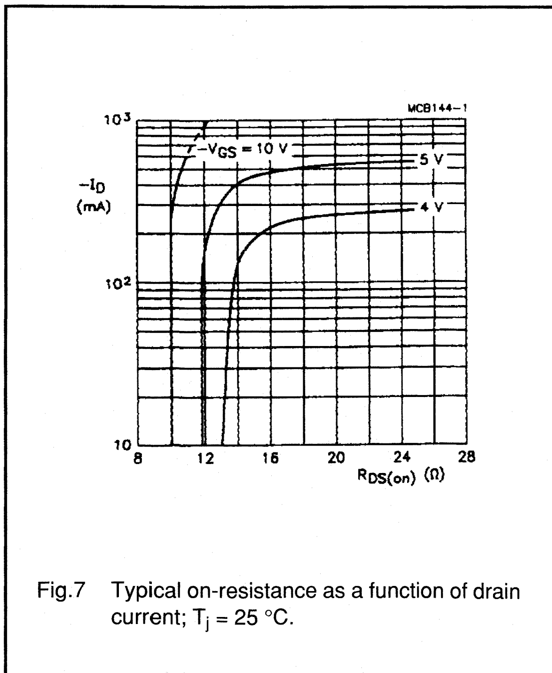


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

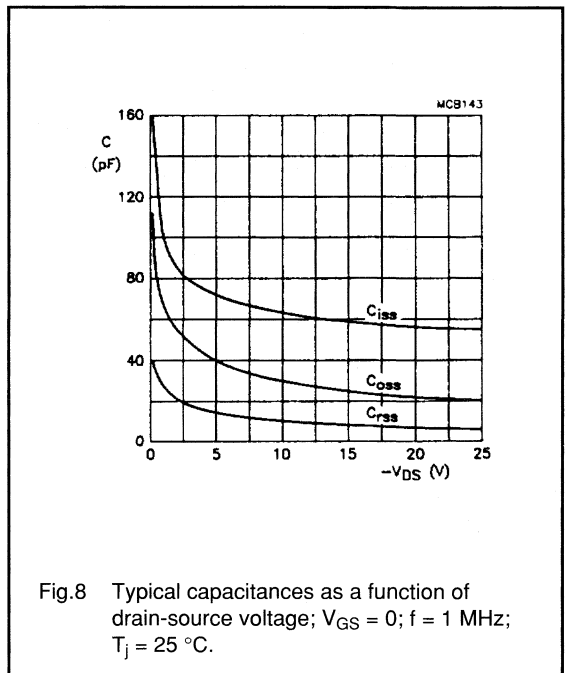


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

P-channel enhancement mode vertical D-MOS transistor

BS208

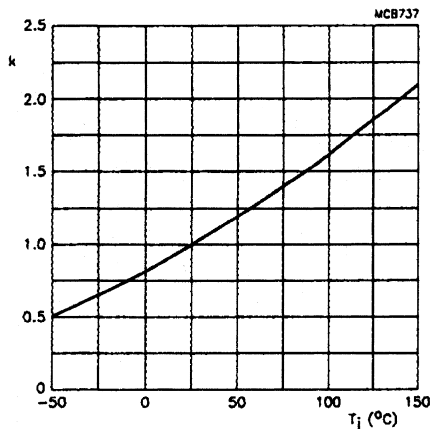


Fig.9 Temperature coefficient of drain-source on-resistance;

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C};$$

typical $R_{DS(on)}$ at 200 mA/10 V.

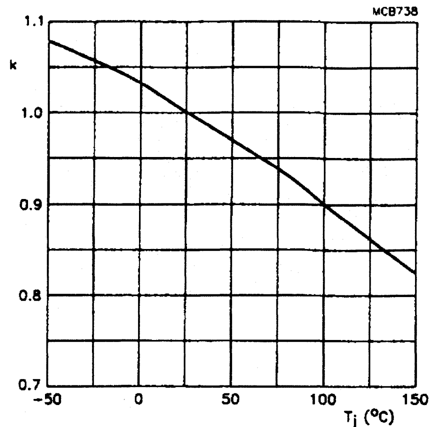


Fig.10 Temperature coefficient of gate-source threshold voltage;

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C};$$

typical VGS(th) at 1 mA.

P-channel enhancement mode vertical D-MOS transistor

BS250

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

FEATURES

- Low $R_{DS(on)}$
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

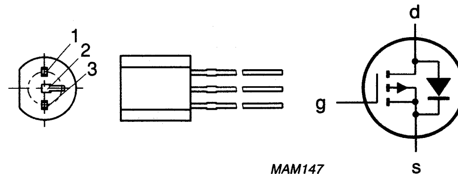
PINNING - TO-92 VARIANT

1 = source
2 = gate
3 = drain

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	45	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0.25	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	0.83	W
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$R_{DS(on)}$	typ.	9	Ω
		max.	14	Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert Y_{fs} \rvert$	typ.	125	mS

PIN CONFIGURATION



Note: Various pinout configurations available.

Fig.1 Simplified outline and symbol.

P-channel enhancement mode vertical D-MOS transistor

BS250

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Parameter	Symbol		Value	Unit
Drain-source voltage	$-V_{DS}$	max.	45	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0.25	A
Drain current (peak value)	$-I_{DM}$	max.	0.5	A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	0.83	W
Storage temperature range	T_{stg}	−65	to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

Parameter	Symbol		Value	Unit
From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	150	K/W

Note

1. Transistor mounted on printed-circuit board, max. lead length 4 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value	Unit
Drain-source breakdown voltage $-I_D$ = 100 μA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	45	V
Drain-source leakage current $-V_{DS}$ = 25 V; V_{GS} = 0	$-I_{DSS}$	max.	0.5	μA
Gate-source leakage current $-V_{GS}$ = 15 V; V_{DS} = 0	$-I_{GSS}$	max.	20	nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	1.0 3.5	V V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$R_{DS(on)}$	typ. max.	9 14	Ω Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert Y_{fs} \rvert$	typ.	125	mS
Input capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max.	30 45	pF pF
Output capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max.	20 30	pF pF
Feedback capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max.	5 10	pF pF

Switching times (see Figs 2 and 3)

$-I_D$ = 200 mA; $-V_{DD}$ = 40 V; $-V_{GS}$ = 0 to 10 V	t_{on}	typ.	4 ns
	t_{off}	typ.	10 ns

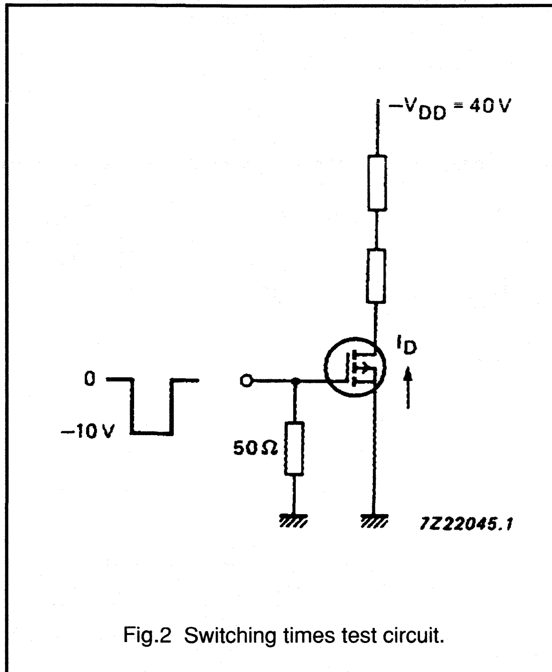


Fig.2 Switching times test circuit.

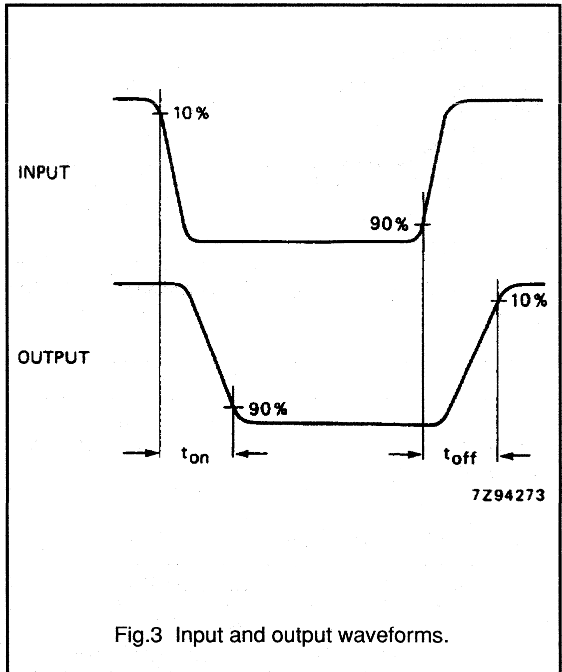


Fig.3 Input and output waveforms.

N-channel enhancement mode MOS transistor

BSH101

FEATURES

- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL etc.

APPLICATIONS

- 'Glue-logic'; interface between logic blocks and/or periphery
- Relay driver
- General purpose switch.

DESCRIPTION

N-channel enhancement mode MOS transistor in a SOT23 package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

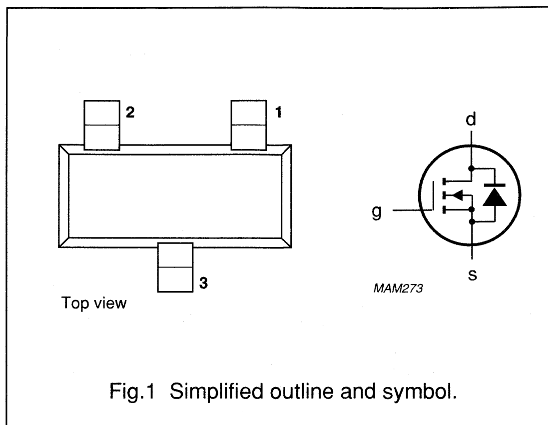


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	60	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.5 A	–	1	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = V_{GS}$; I_D = 1 mA	1	2.8	V
I_D	drain current (DC)	T_s = 80 °C	–	0.7	A
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 0.35 A	–	0.6	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W

PRELIMINARY
See Philips Semiconductors for Design-in information

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IE 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	60	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	$T_s = 80$ °C; note 1	–	0.7	A
I_{DM}	peak drain current	note 2	–	2.8	A
P_{tot}	total power dissipation	$T_s = 80$ °C	–	0.5	W
		$T_{amb} = 25$ °C; note 3	–	0.75	W
		$T_{amb} = 25$ °C; note 4	–	0.54	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	$T_s = 80$ °C	–	0.6	A
I_{SM}	peak pulsed source current	note 2	–	2.4	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	140	K/W
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	360	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	60	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 48 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 0.35 A	–	–	0.6	Ω
		V_{GS} = 4.5 V; I_D = 0.17 A	–	–	0.9	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 48 V; f = 1 MHz	–	67	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 48 V; f = 1 MHz	–	12	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 48 V; f = 1 MHz	–	4	–	pF
Q_G	total gate charge	V_{GS} = 10 V; V_{DD} = 30 V; I_D = 0.35 A; T_{amb} = 25 °C	–	2200	–	pC
Q_{GS}	gate-source charge	V_{GS} = 10 V; V_{DD} = 30 V; I_D = 0.35 A; T_{amb} = 25 °C	–	200	–	pC
Q_{GD}	gate-drain charge	V_{GS} = 10 V; V_{DD} = 30 V; I_D = 0.35 A; T_{amb} = 25 °C	–	700	–	pC
t_{on}	turn-on switching time	V_{GS} = 0 to 10 V; V_{DD} = 30 V; I_D = 0.35 A; R_{gen} = 6 Ω	–	7	–	ns
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 10 V; V_{DD} = 30 V; I_D = 0.35 A; R_{gen} = 6 Ω	–	4	–	ns
t_f	fall time	V_{GS} = 0 to 10 V; V_{DD} = 30 V; I_D = 0.35 A; R_{gen} = 6 Ω	–	3	–	ns
t_{off}	turn-off switching time	V_{GS} = 10 to 0 V; V_{DD} = 30 V; I_D = 0.35 A; R_{gen} = 6 Ω	–	17	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 10 to 0 V; V_{DD} = 30 V; I_D = 0.35 A; R_{gen} = 6 Ω	–	10	–	ns
t_r	rise time	V_{GS} = 10 to 0 V; V_{DD} = 30 V; I_D = 0.35 A; R_{gen} = 6 Ω	–	7	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.5 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 0.5 A; di/dt = −100 A/μs	–	tbf	–	ns

N-channel enhancement mode MOS transistor

BSH102

FEATURES

- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL etc.

APPLICATIONS

- 'Glue-logic'; interface between logic blocks and/or periphery
- Relay driver
- General purpose switch.

DESCRIPTION

N-channel enhancement mode MOS transistor in a SOT23 package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

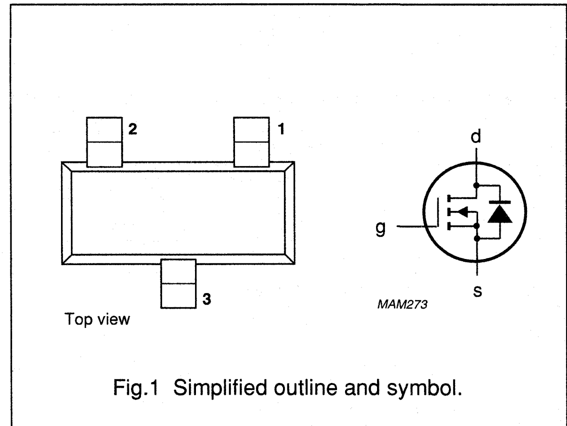


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{SD}	source-drain diode forward voltage	$V_{GD} = 0$; $I_S = 0.5$ A	–	1	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1$ mA	1	2.8	V
I_D	drain current (DC)	$T_s = 80$ °C	–	1	A
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 0.5$ A	–	0.3	Ω
P_{tot}	total power dissipation	$T_s = 80$ °C	–	0.5	W

PRELIMINARY
See Philips Semiconductors for Design-in information

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	1	A
I_{DM}	peak drain current	note 2	–	4	A
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W
		T_{amb} = 25 °C; note 3	–	0.75	W
		T_{amb} = 25 °C; note 4	–	0.54	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	0.6	A
I_{SM}	peak pulsed source current	note 2	–	2.4	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	140	K/W
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	360	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 0.5 A	–	–	0.3	Ω
		V_{GS} = 4.5 V; I_D = 0.25 A	–	–	0.45	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	67	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	27	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	13	–	pF
Q_G	total gate charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 0.5 A; T_{amb} = 25 °C	–	2250	–	pC
Q_{GS}	gate-source charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 0.5 A; T_{amb} = 25 °C	–	200	–	pC
Q_{GD}	gate-drain charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 0.5 A; T_{amb} = 25 °C	–	900	–	pC
t_{on}	turn-on switching time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	8	–	ns
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	4	–	ns
t_f	fall time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	4	–	ns
t_{off}	turn-off switching time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	13	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	9	–	ns
t_r	rise time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 0.5 A; R_{gen} = 6 Ω	–	4	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.5 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 0.5 A; di/dt = −100 A/μs	–	tbf	–	ns

N-channel enhancement mode MOS transistor

BSH103

FEATURES

- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL etc.
- Low threshold.

APPLICATIONS

- 'Glue-logic'; interface between logic blocks and/or periphery
- Relay driver
- General purpose switch
- Battery powered applications.

DESCRIPTION

N-channel enhancement mode MOS transistor in a SOT23 package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

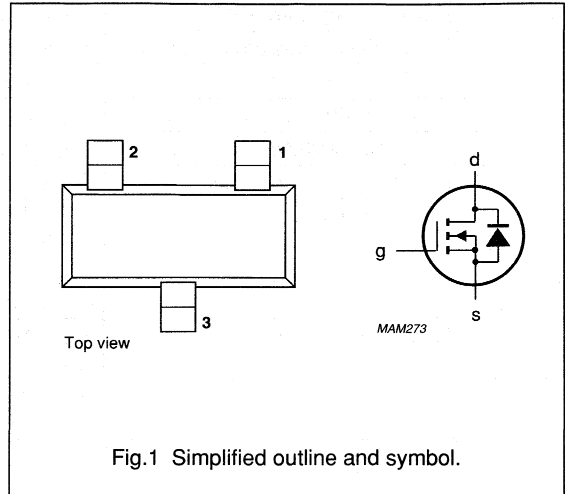


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETERS	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{SD}	source-drain diode forward voltage	$V_{GD} = 0$; $I_S = 0.5$ A	–	1	V
V_{GS}	gate-source voltage (DC)		–	±12	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1$ mA	0.5	1.1	V
I_D	drain current (DC)	$T_s = 80$ °C	–	0.9	A
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5$ V; $I_D = 0.45$ A	–	0.35	Ω
P_{tot}	total power dissipation	$T_s = 80$ °C	–	0.5	W

PRELIMINARY
See Philips Semiconductors for Design-in information

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	±12	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	0.9	A
I_{DM}	peak drain current	note 2	–	3.6	A
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W
		T_{amb} = 25 °C; note 3	–	0.75	W
		T_{amb} = 25 °C; note 4	–	0.54	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	0.6	A
I_{SM}	peak pulsed source current	note 2	–	2.4	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	140	K/W
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	360	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	0.5	–	1.1	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±12 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 0.45 A	–	–	0.35	Ω
		V_{GS} = 2.5 V; I_D = 0.22 A	–	–	0.52	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	87	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	27	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	13	–	pF
Q_G	total gate charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 0.45 A; T_{amb} = 25 °C	–	3800	–	pC
Q_{GS}	gate-source charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 0.45 A; T_{amb} = 25 °C	–	100	–	pC
Q_{GD}	gate-drain charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 0.45 A; T_{amb} = 25 °C	–	850	–	pC
t_{on}	turn-on switching time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 0.45 A; R_{gen} = 6 Ω	–	6	–	ns
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 0.45 A; R_{gen} = 6 Ω	–	3	–	ns
t_f	fall time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 0.45 A; R_{gen} = 6 Ω	–	3	–	ns
t_{off}	turn-off switching time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 0.45 A; R_{gen} = 6 Ω	–	16	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 0.45 A; R_{gen} = 6 Ω	–	13	–	ns
t_r	rise time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 0.45 A; R_{gen} = 6 Ω	–	3	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.5 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 0.5 A; di/dt = −100 A/μs	–	tbf	–	ns

N-channel enhancement mode MOS transistor

BSH105

FEATURES

- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL, etc.
- Very low threshold.

APPLICATIONS

- 'Glue-logic': interface between logic blocks and/or periphery
- Relay driver
- General purpose switch
- Battery powered applications.

DESCRIPTION

N-channel enhancement mode MOS transistor in a SOT23 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

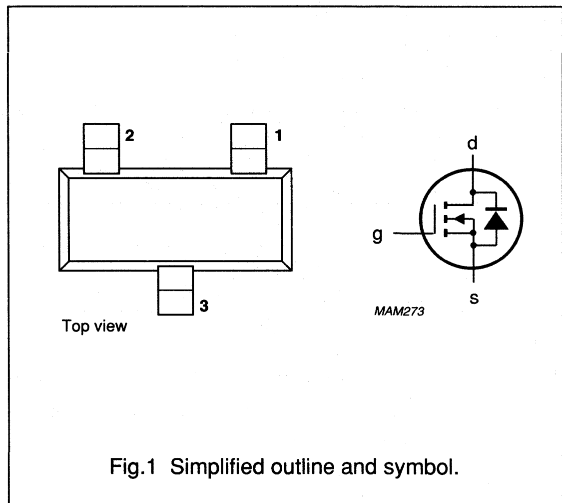


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	12	V
V_{SD}	source-drain diode forward voltage	$V_{GD} = 0$; $I_S = 0.5$ A	–	1	V
V_{GS}	gate-source voltage (DC)		–	±8	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1$ mA	0.4	–	V
I_D	drain current (DC)	$T_s = 80$ °C	–	1.5	A
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5$ V; $I_D = 0.8$ A	–	0.12	Ω
P_{tot}	total power dissipation	$T_s = 80$ °C	–	0.5	W

OBJECTIVE
See Philips Semiconductors for Design-in information

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	12	V
V_{GS}	gate-source voltage (DC)		–	±8	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	1.5	A
I_{DM}	peak drain current	note 2	–	6	A
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W
		T_{amb} = 25 °C; note 3	–	0.75	W
		T_{amb} = 25 °C; note 4	–	0.54	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	0.6	A
I_{SM}	peak pulsed source current	note 2	–	2.4	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	140	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	12	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	0.4	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 9.6 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±8 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 0.8 A	–	–	120	mΩ
		V_{GS} = 2.5 V; I_D = 0.8 A	–	–	150	mΩ
		V_{GS} = 1.8 V; I_D = 0.4 A	–	–	230	mΩ
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 9.6 V; f = 1 MHz	–	t.b.f.	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 9.6 V; f = 1 MHz	–	t.b.f.	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 9.6 V; f = 1 MHz	–	t.b.f.	–	pF
Q_G	total gate charge	V_{GS} = 6 V; V_{DD} = 6 V; I_D = 1 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GS}	gate-source charge	V_{DD} = 6 V; I_D = 1 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GD}	gate-drain charge	V_{DD} = 6 V; I_D = 1 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 6 V; V_{DD} = 6 V; I_D = 1 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_f	fall time	V_{GS} = 0 to 6 V; V_{DD} = 6 V; I_D = 1 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to 6 V; V_{DD} = 6 V; I_D = 1 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 6 to 0 V; V_{DD} = 6 V; I_D = 1 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_r	rise time	V_{GS} = 6 to 0 V; V_{DD} = 6 V; I_D = 1 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{off}	turn-off switching time	V_{GS} = 6 to 0 V; V_{DD} = 6 V; I_D = 1 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.5 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 0.5 A; di/dt = –100 A/μs	–	t.b.f.	–	ns

N-channel enhancement mode MOS transistor

BSH106

FEATURES

- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL, etc.
- Very low threshold.

APPLICATIONS

- 'Glue-logic': interface between logic blocks and/or periphery
- Relay driver
- General purpose switch
- Battery powered applications.

DESCRIPTION

N-channel enhancement mode MOS transistor in a SOT363 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT363

PIN	SYMBOL	DESCRIPTION
1	d	drain
2	d	drain
3	g	gate
4	s	source
5	d	drain
6	d	drain

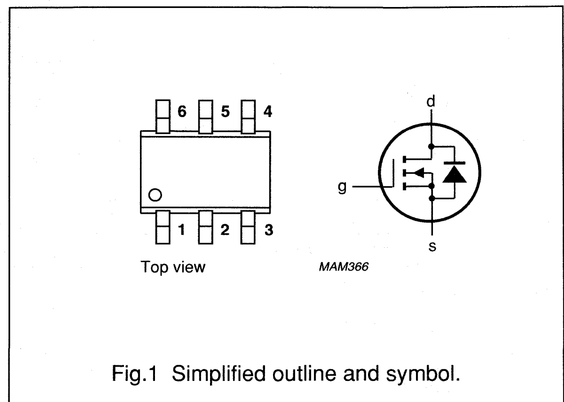


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	12	V
V_{SD}	source-drain diode forward voltage	$V_{GD} = 0$; $I_S = 0.5$ A	–	1	V
V_{GS}	gate-source voltage (DC)		–	±8	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1$ mA	0.4	–	V
I_D	drain current (DC)	$T_s = 80$ °C	–	1.8	A
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5$ V; $I_D = 0.9$ A	–	0.14	Ω
P_{tot}	total power dissipation	$T_s = 80$ °C	–	0.8	W

OBJECTIVE
See Philips Semiconductors for Design-in information

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	12	V
V_{GS}	gate-source voltage (DC)		–	±8	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	1.8	A
I_{DM}	peak drain current	note 2	–	7.2	A
P_{tot}	total power dissipation	T_s = 80 °C	–	0.8	W
		T_{amb} = 25 °C; note 3	–	1.1	W
		T_{amb} = 25 °C; note 4	–	0.7	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	1	A
I_{SM}	peak pulsed source current	note 2	–	4	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	87.5	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	12	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	0.4	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 9.6 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±8 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 0.9 A	–	–	140	mΩ
		V_{GS} = 2.5 V; I_D = 0.9 A	–	–	180	mΩ
		V_{GS} = 1.8 V; I_D = 0.4 A	–	–	270	mΩ
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 9.6 V; f = 1 MHz	–	t.b.f.	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 9.6 V; f = 1 MHz	–	t.b.f.	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 9.6 V; f = 1 MHz	–	t.b.f.	–	pF
Q_G	total gate charge	V_{GS} = 6 V; V_{DD} = 6 V; I_D = 0.9 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GS}	gate-source charge	V_{DD} = 6 V; I_D = 0.9 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GD}	gate-drain charge	V_{DD} = 6 V; I_D = 0.9 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 6 V; V_{DD} = 6 V; I_D = 0.9 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_f	fall time	V_{GS} = 0 to 6 V; V_{DD} = 6 V; I_D = 0.9 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to 6 V; V_{DD} = 6 V; I_D = 0.9 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 6 to 0 V; V_{DD} = 6 V; I_D = 0.9 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_r	rise time	V_{GS} = 6 to 0 V; V_{DD} = 6 V; I_D = 0.9 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{off}	turn-off switching time	V_{GS} = 6 to 0 V; V_{DD} = 6 V; I_D = 0.9 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 0.5 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 0.5 A; di/dt = −100 A/μs	–	t.b.f.	–	ns

P-channel enhancement mode MOS transistor

BSH205

FEATURES

- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL, etc.
- Very low threshold.

APPLICATIONS

- 'Glue-logic': interface between logic blocks and/or periphery
- Relay driver
- Power switching
- Battery powered applications.

DESCRIPTION

P-channel enhancement mode MOS transistor in a SOT23 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

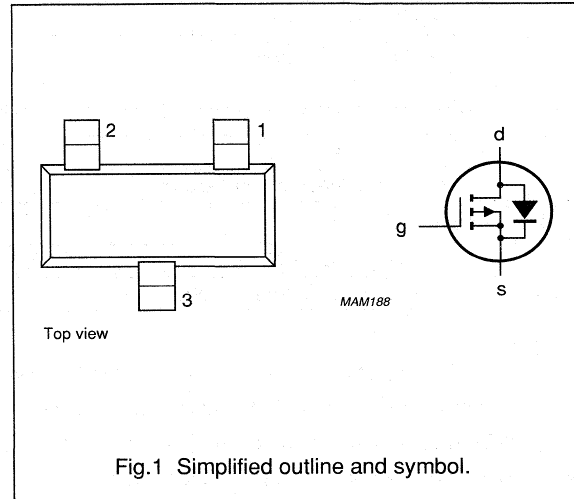


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–12	V
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = –0.5 A	–	–1	V
V_{GS}	gate-source voltage (DC)		–	±8	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = –1 mA	–0.4	–	V
I_D	drain current (DC)	T_s = 80 °C	–	–1	A
R_{DSon}	drain-source on-state resistance	V_{GS} = –4.5 V; I_D = –0.5 A	–	0.3	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W

OBJECTIVE
See Philips Semiconductors for Design-in information

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–12	V
V_{GS}	gate-source voltage (DC)		–	±8	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	–1	A
I_{DM}	peak drain current	note 2	–	–4	A
P_{tot}	total power dissipation	T_s = 80 °C	–	0.5	W
		T_{amb} = 25 °C; note 3	–	0.75	W
		T_{amb} = 25 °C; note 4	–	0.54	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	–0.6	A
I_{SM}	peak pulsed source current	note 2	–	–2.4	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on a printed-circuit board with a $R_{th\ a-tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on a printed-circuit board with a $R_{th\ a-tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-s}$	thermal resistance from junction to soldering point	140	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−12	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−0.4	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −9.6 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±8 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −0.5 A	–	–	0.3	Ω
		V_{GS} = −2.5 V; I_D = −0.5 A	–	–	0.38	Ω
		V_{GS} = −1.8 V; I_D = −0.3 A	–	–	0.57	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −9.6 V; f = 1 MHz	–	t.b.f.	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −9.6 V; f = 1 MHz	–	t.b.f.	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −9.6 V; f = 1 MHz	–	t.b.f.	–	pF
Q_G	total gate charge	V_{GS} = −6 V; V_{DD} = −6 V; I_D = −0.85 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GS}	gate-source charge	V_{DD} = −6 V; I_D = −0.85 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Q_{GD}	gate-drain charge	V_{DD} = −6 V; I_D = −0.85 A; T_{amb} = 25 °C	–	t.b.f.	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −6 V; V_{DD} = −6 V; I_D = −0.85 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_r	rise time	V_{GS} = 0 to −6 V; V_{DD} = −6 V; I_D = −0.85 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to −6 V; V_{DD} = −6 V; I_D = −0.85 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = −6 to 0 V; V_{DD} = −6 V; I_D = −0.85 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_f	fall time	V_{GS} = −6 to 0 V; V_{DD} = −6 V; I_D = −0.85 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
t_{off}	turn-off switching time	V_{GS} = −6 to 0 V; V_{DD} = −6 V; I_D = −0.85 A; R_{gen} = 6 Ω	–	t.b.f.	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = −0.5 A	–	–	−1	V
t_{rr}	reverse recovery time	I_S = −0.5 A; di/dt = 100 A/μs	–	t.b.f.	–	ns

P-channel enhancement mode MOS transistor

BSH206

FEATURES

- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL, etc.
- Very low threshold.

APPLICATIONS

- 'Glue-logic': interface between logic blocks and/or periphery
- Relay driver
- Power switching
- Battery powered applications.

DESCRIPTION

P-channel enhancement mode MOS transistor in a SOT363 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT363

PIN	SYMBOL	DESCRIPTION
1	d	drain
2	d	drain
3	g	gate
4	s	source
5	d	drain
6	d	drain

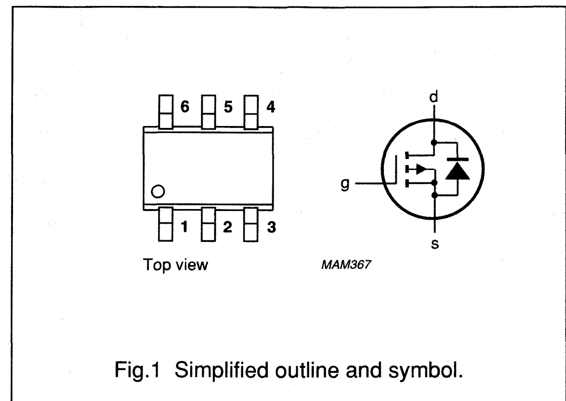


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–12	V
V_{SD}	source-drain diode forward voltage	$V_{GD} = 0$; $I_S = -0.5$ A	–	–1	V
V_{GS}	gate-source voltage (DC)		–	±8	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = V_{GS}$; $I_D = -1$ mA	–0.4	–	V
I_D	drain current (DC)	$T_s = 80$ °C	–	–1.2	A
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5$ V; $I_D = -0.6$ A	–	0.36	Ω
P_{tot}	total power dissipation	$T_s = 80$ °C	–	0.8	W

OBJECTIVE
See Philips Semiconductors for Design-in information

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–12	V
V_{GS}	gate-source voltage (DC)		–	±8	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	–1.2	A
I_{DM}	peak drain current	note 2	–	–4.6	A
P_{tot}	total power dissipation	T_s = 80 °C	–	0.8	W
		T_{amb} = 25 °C; note 3	–	1.1	W
		T_{amb} = 25 °C; note 4	–	0.7	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	–1	A
I_{SM}	peak pulsed source current	note 2	–	–4	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	87.5	K/W

CHARACTERISTICS

$T_j = 25\ °C$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = -10\ \mu A$	–12	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{GS} = V_{DS}$; $I_D = -1$ mA	–0.4	–	–	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = -9.6$ V	–	–	–100	nA
I_{GSS}	gate leakage current	$V_{GS} = \pm 8$ V; $V_{DS} = 0$	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5$ V; $I_D = -0.6$ A	–	–	0.36	Ω
		$V_{GS} = -2.5$ V; $I_D = -0.6$ A	–	–	0.45	Ω
		$V_{GS} = -1.8$ V; $I_D = -0.3$ A	–	–	0.67	Ω
C_{iss}	input capacitance	$V_{GS} = 0$; $V_{DS} = -9.6$ V; f = 1 MHz	–	t.b.f.	–	pF
C_{oss}	output capacitance	$V_{GS} = 0$; $V_{DS} = -9.6$ V; f = 1 MHz	–	t.b.f.	–	pF
C_{rss}	reverse transfer capacitance	$V_{GS} = 0$; $V_{DS} = -9.6$ V; f = 1 MHz	–	t.b.f.	–	pF
Q_G	total gate charge	$V_{GS} = -6$ V; $V_{DD} = -6$ V; $I_D = -0.6$ A; $T_{amb} = 25\ °C$	–	t.b.f.	–	pC
Q_{GS}	gate-source charge	$V_{DD} = -6$ V; $I_D = -0.6$ A; $T_{amb} = 25\ °C$	–	t.b.f.	–	pC
Q_{GD}	gate-drain charge	$V_{DD} = -6$ V; $I_D = -0.6$ A; $T_{amb} = 25\ °C$	–	t.b.f.	–	pC
Switching times						
$t_{d(on)}$	turn-on delay time	$V_{GS} = 0$ to -6 V; $V_{DD} = -6$ V; $I_D = -0.6$ A; $R_{gen} = 6\ \Omega$	–	t.b.f.	–	ns
t_r	rise time	$V_{GS} = 0$ to -6 V; $V_{DD} = -6$ V; $I_D = -0.6$ A; $R_{gen} = 6\ \Omega$	–	t.b.f.	–	ns
t_{on}	turn-on switching time	$V_{GS} = 0$ to -6 V; $V_{DD} = -6$ V; $I_D = -0.6$ A; $R_{gen} = 6\ \Omega$	–	t.b.f.	–	ns
$t_{d(off)}$	turn-off delay time	$V_{GS} = -6$ to 0 V; $V_{DD} = -6$ V; $I_D = -0.6$ A; $R_{gen} = 6\ \Omega$	–	t.b.f.	–	ns
t_f	fall time	$V_{GS} = -6$ to 0 V; $V_{DD} = -6$ V; $I_D = -0.6$ A; $R_{gen} = 6\ \Omega$	–	t.b.f.	–	ns
t_{off}	turn-off switching time	$V_{GS} = -6$ to 0 V; $V_{DD} = -6$ V; $I_D = -0.6$ A; $R_{gen} = 6\ \Omega$	–	t.b.f.	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	$V_{GD} = 0$; $I_S = -0.5$ A	–	–	–1	V
t_{rr}	reverse recovery time	$I_S = -0.5$ A; di/dt = 100 A/μs	–	t.b.f.	–	ns

N-channel enhancement mode vertical D-MOS transistors

BSN10; BSN10A

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 envelope, intended for use in general purpose fast switching applications.

PINNING

PIN	DESCRIPTION
BSN10	
1	gate
2	drain
3	source
BSN10A	
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	50	V
I_D	DC drain current	175	mA
$R_{DS(on)}$	drain-source on-resistance	15	Ω
$V_{GS(th)}$	gate-source threshold voltage	1.8	V

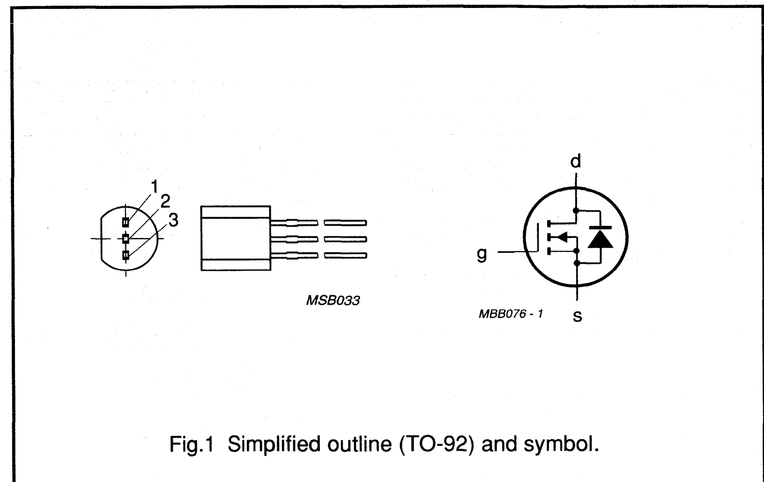


Fig.1 Simplified outline (TO-92) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	50	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	175	mA
I_{DM}	peak drain current		–	300	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	830	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	150 K/W

Note

1. Device mounted on a printed circuit board, maximum lead length 4 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	50	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 40 V; V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.4	–	1.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 100 mA; V_{GS} = 10 V	–	8	15	Ω
		I_D = 100 mA; V_{GS} = 5 V	–	12	20	Ω
		I_D = 10 mA; V_{GS} = 2.5 V	–	18	30	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 100 mA; V_{DS} = 10 V	40	80	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	8	15	pF
C_{oss}	output capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	7	15	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V; V_{GS} = 0; f = 1 MHz	–	2	5	pF
Switching times						
t_{on}	turn-on time	I_D = 100 mA; V_{DD} = 20 V; V_{GS} = 0 to 10 V	–	2	5	ns
t_{off}	turn-off time	I_D = 100 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	5	10	ns

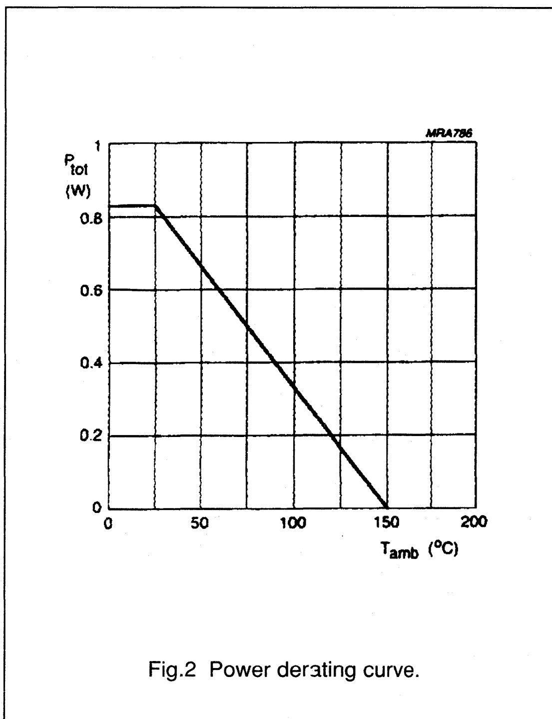
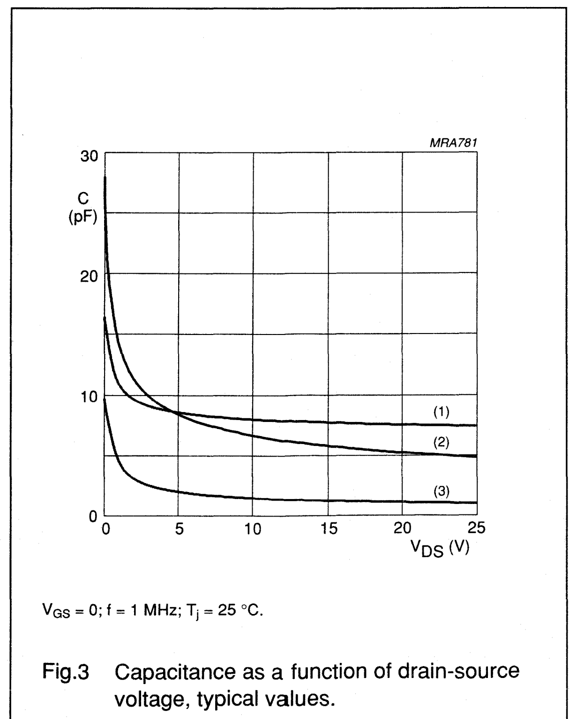
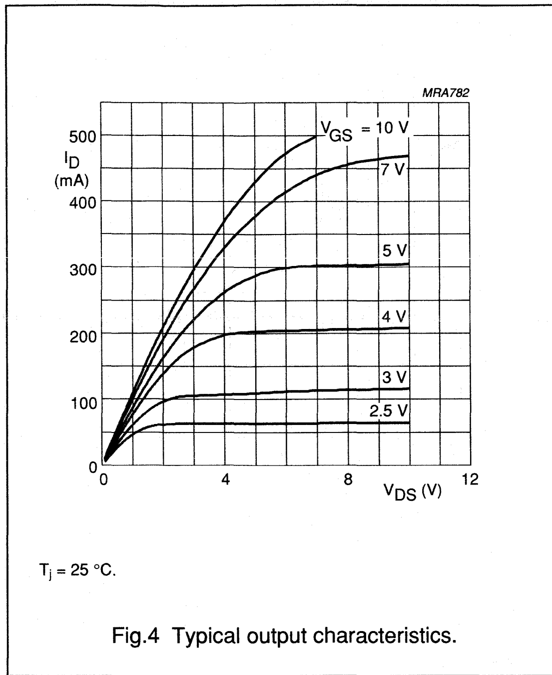


Fig.2 Power derating curve.



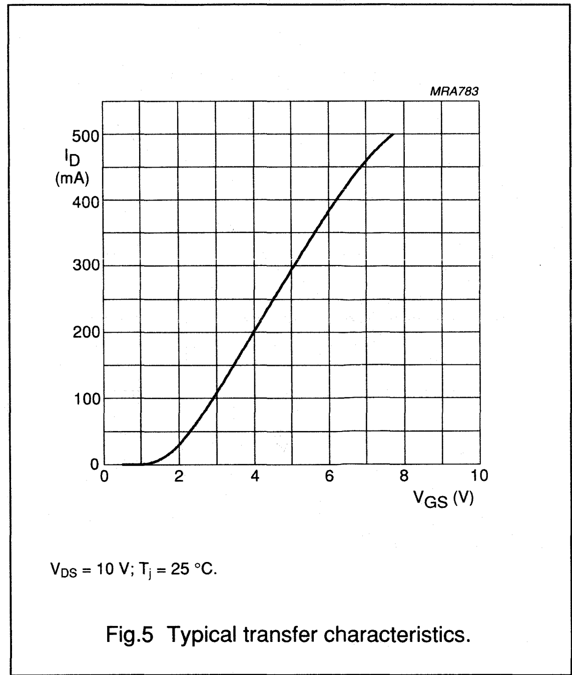
V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.3 Capacitance as a function of drain-source voltage, typical values.



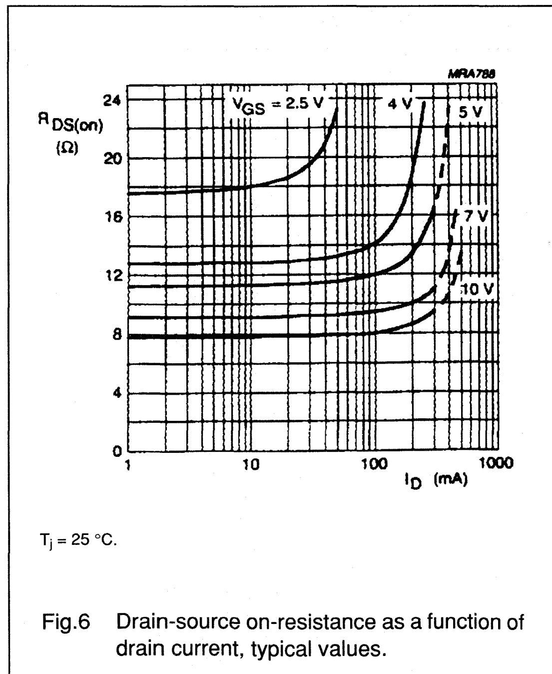
T_j = 25 °C.

Fig.4 Typical output characteristics.



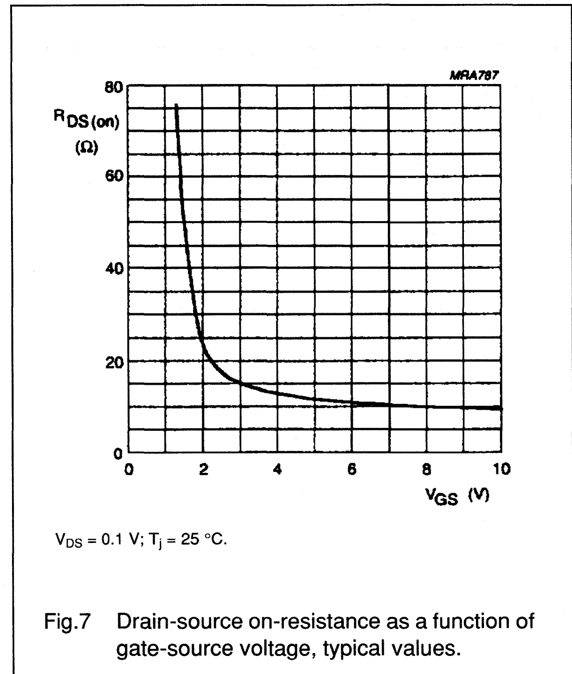
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Typical transfer characteristics.



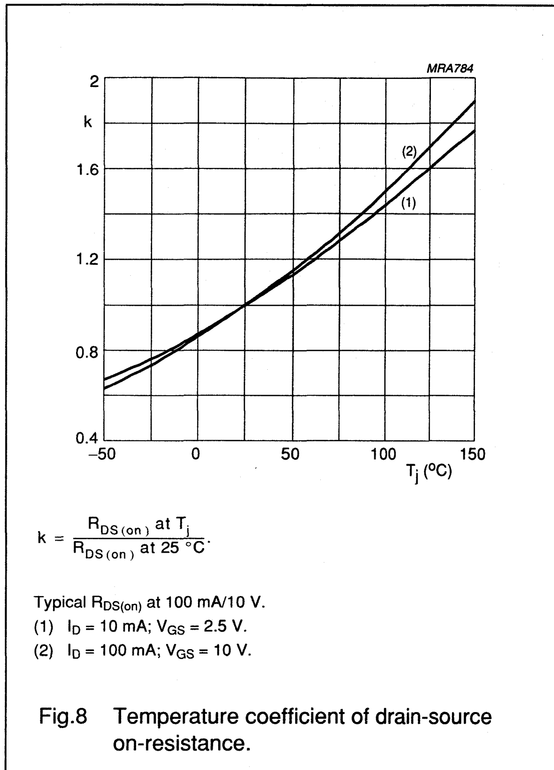
T_j = 25 °C.

Fig.6 Drain-source on-resistance as a function of drain current, typical values.



V_{DS} = 0.1 V; T_j = 25 °C.

Fig.7 Drain-source on-resistance as a function of gate-source voltage, typical values.



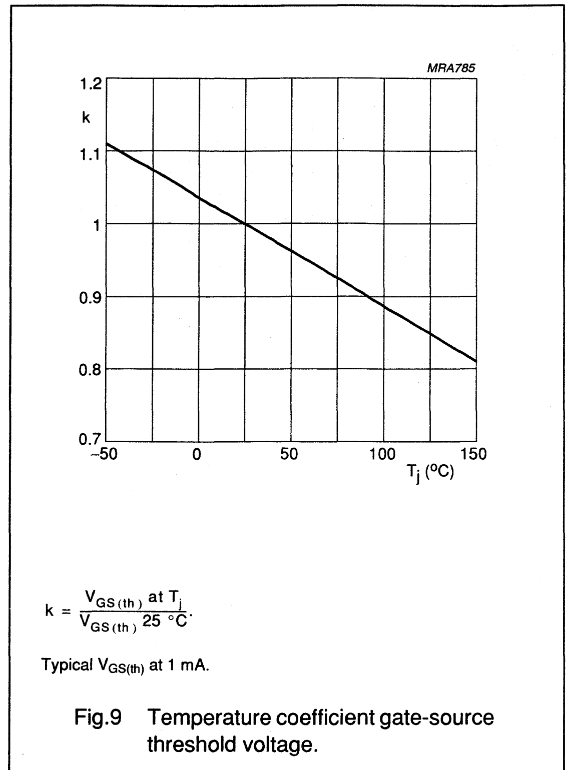
$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}.$$

Typical $R_{DS(on)}$ at 100 mA/10 V.

(1) I_D = 10 mA; V_{GS} = 2.5 V.

(2) I_D = 100 mA; V_{GS} = 10 V.

Fig.8 Temperature coefficient of drain-source on-resistance.



$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)}\ 25\ °C}.$$

Typical $V_{GS(th)}$ at 1 mA.

Fig.9 Temperature coefficient gate-source threshold voltage.

N-channel enhancement mode vertical D-MOS transistor

BSN20

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Thin and thick film circuits
- General purpose fast switching applications.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

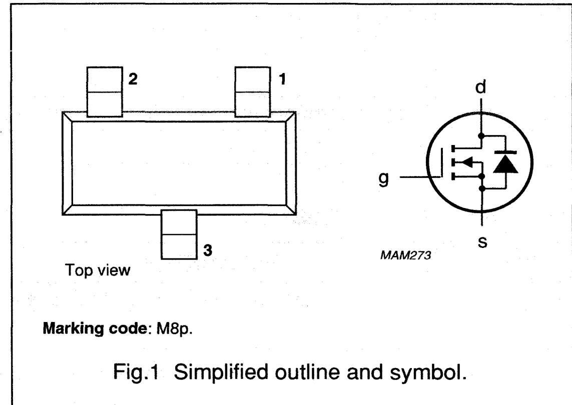


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		50	V
I_D	drain current (DC)		100	mA
R_{DSon}	drain-source on-state resistance	I_D = 100 mA; V_{GS} = 10 V	15	Ω
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	1.8	V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	50	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	100	mA
I_{DM}	peak drain current		–	300	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	300	mW
		up to T_{amb} = 25 °C; note 2	–	250	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	430	K/W
		note 2	500	K/W

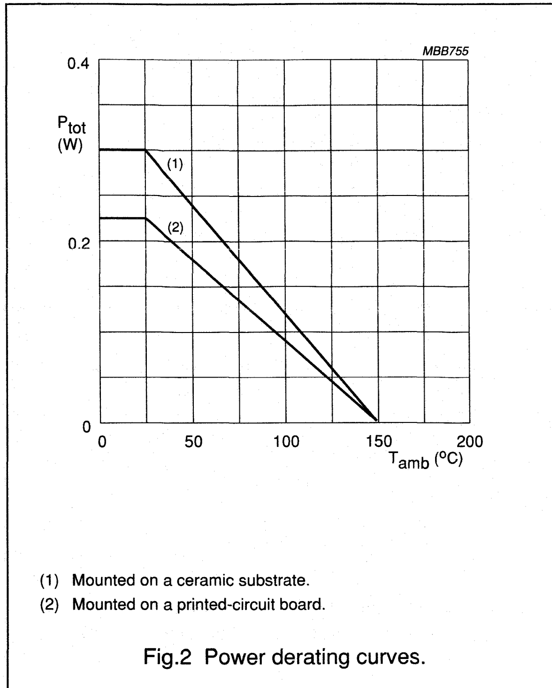
Notes to the Limiting values and Thermal characteristics

1. Device mounted on a ceramic substrate, 10 × 8 × 0.7 mm.
2. Device mounted on a printed-circuit board.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

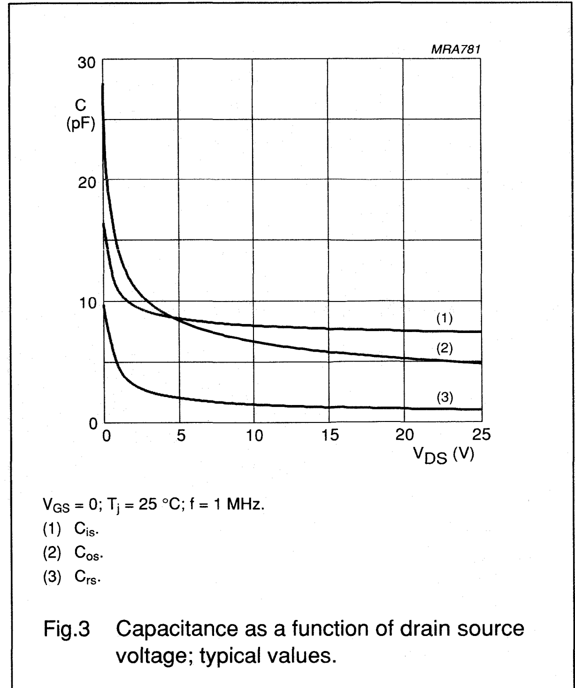
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	50	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	0.4	–	1.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 40 V	–	–	1	μA
I_{GSS}	gate-source leakage current	V_{DS} = 0; V_{GS} = ±20 V	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 100 mA	–	8	15	Ω
		V_{GS} = 5 V; I_D = 100 mA	–	14	20	Ω
		V_{GS} = 2.5 V; I_D = 10 mA	–	18	30	Ω
$\|y_{fs}\|$	forward transfer admittance	V_{DS} = 10 V; I_D = 100 mA	40	80	–	mS
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 10 V; f = 1 MHz	–	8	15	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 10 V; f = 1 MHz	–	7	15	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 10 V; f = 1 MHz	–	2	5	pF
Switching times						
t_{on}	turn-on time	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 100 mA	–	2	5	ns
t_{off}	turn-off time	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 100 mA	–	5	10	ns



(1) Mounted on a ceramic substrate.

(2) Mounted on a printed-circuit board.

Fig.2 Power derating curves.



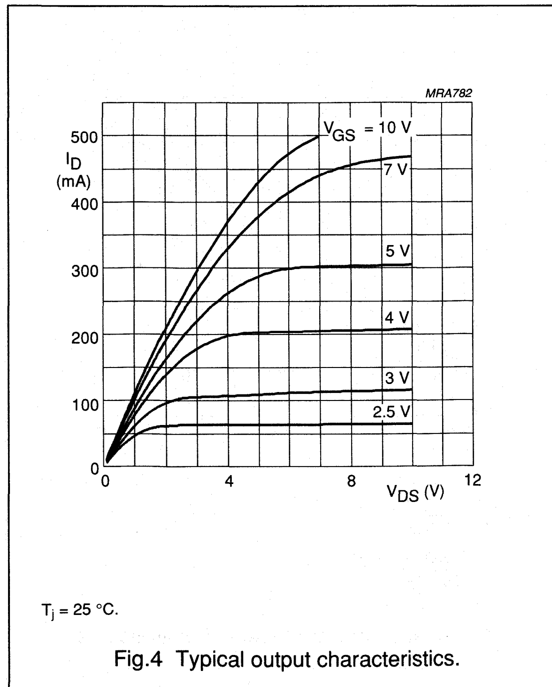
V_{GS} = 0; T_j = 25 °C; f = 1 MHz.

(1) C_{is}.

(2) C_{os}.

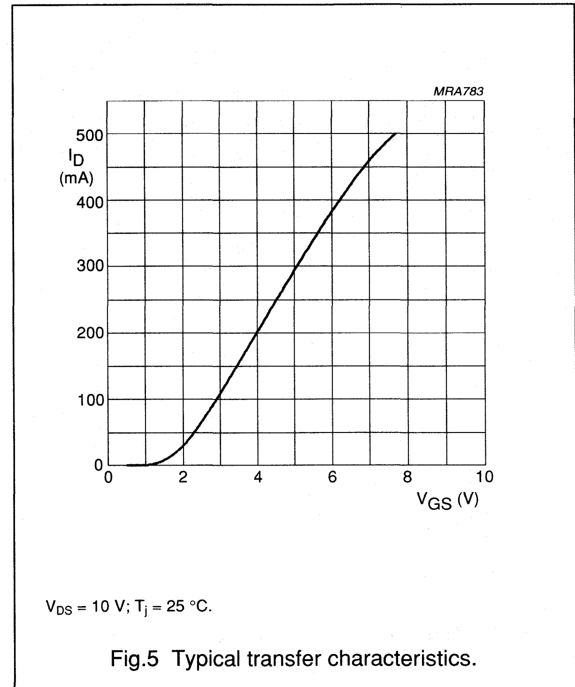
(3) C_{rs}.

Fig.3 Capacitance as a function of drain source voltage; typical values.



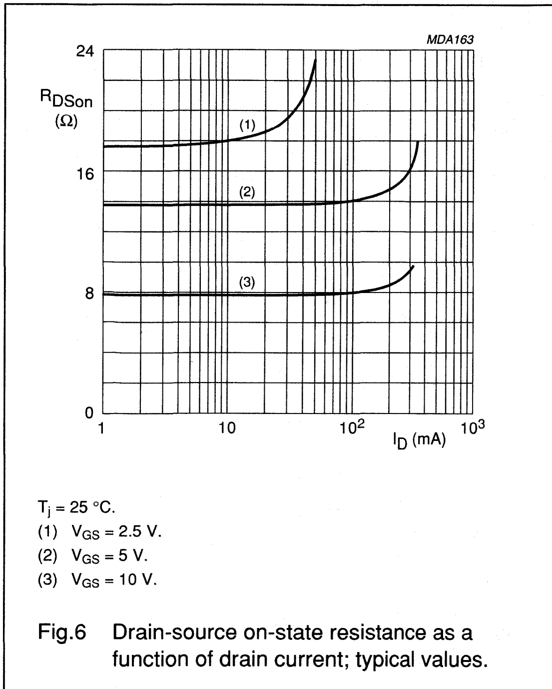
T_j = 25 °C.

Fig.4 Typical output characteristics.



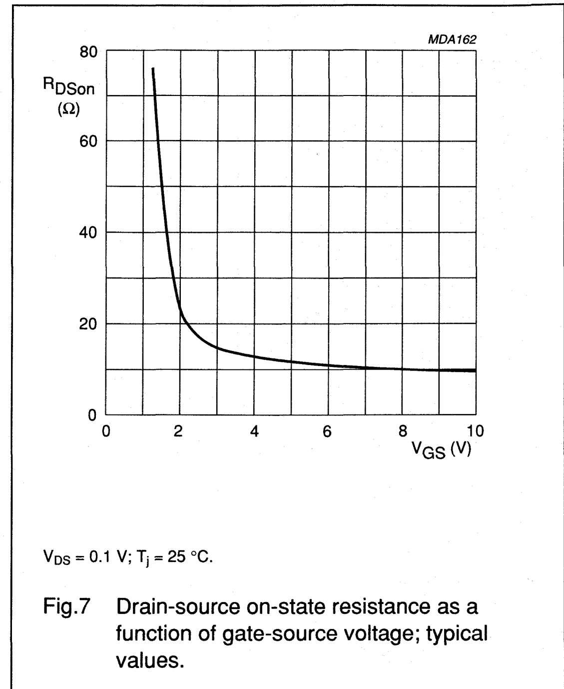
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Typical transfer characteristics.



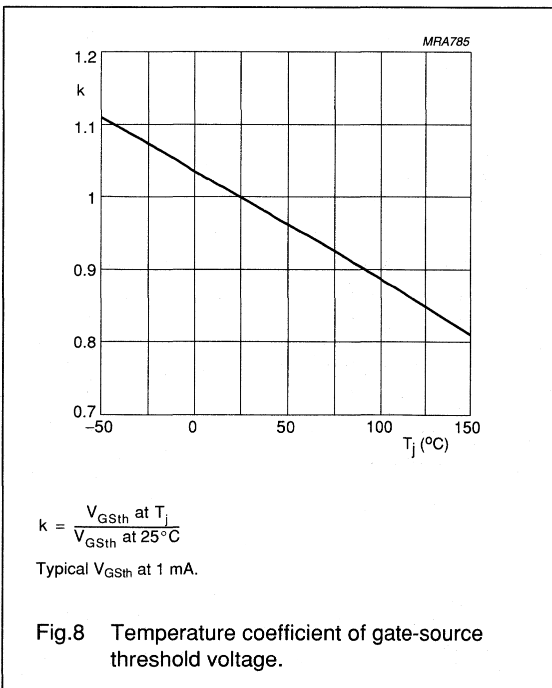
T_j = 25 °C.
(1) V_{GS} = 2.5 V.
(2) V_{GS} = 5 V.
(3) V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of drain current; typical values.



V_{DS} = 0.1 V; T_j = 25 °C.

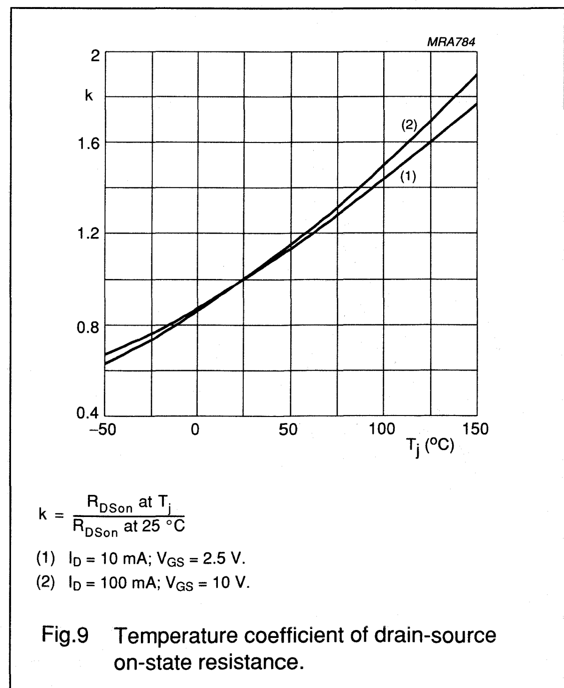
Fig.7 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

Typical V_{GSth} at 1 mA.

Fig.8 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25 °C}$$

(1) I_D = 10 mA; V_{GS} = 2.5 V.
(2) I_D = 100 mA; V_{GS} = 10 V.

Fig.9 Temperature coefficient of drain-source on-state resistance.

N-channel enhancement mode vertical D-MOS transistor

BSN20W

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Thin and thick film circuits
- General purpose fast switching applications.

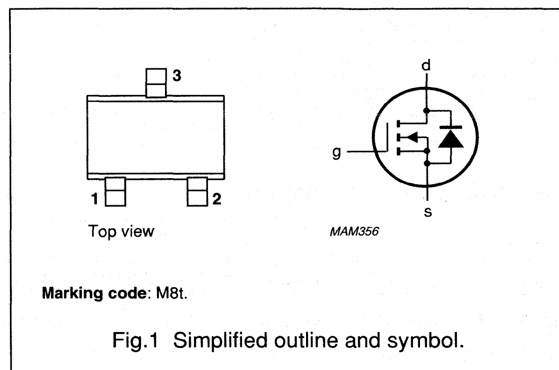
DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a 3 pin plastic SOT323 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT323

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain



Marking code: M8t.

Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		50	V
V_{GSth}	gate-source threshold voltage		1.8	V
I_D	drain current (DC)		80	mA
R_{DSon}	drain-source on-state resistance		15	Ω
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	200	mW

Note

1. Device mounted on a printed-circuit board.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	50	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	80	mA
I_{DM}	peak drain current		–	300	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	625	K/W

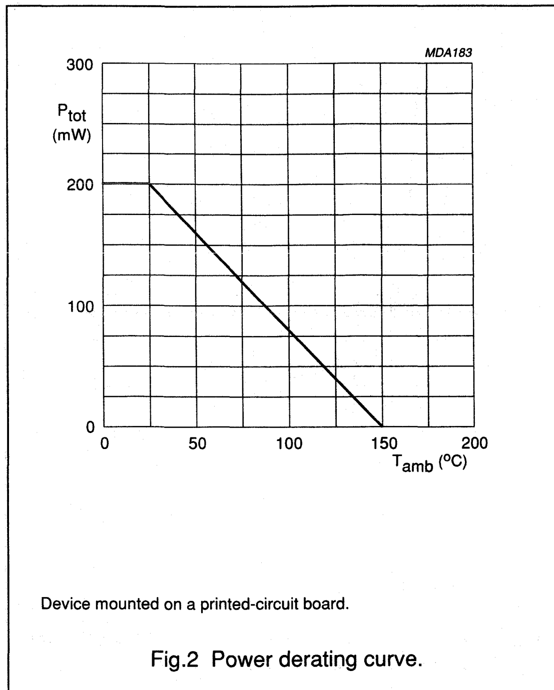
Note to the Limiting values and Thermal characteristics

1. Device mounted on a printed-circuit board.

CHARACTERISTICS

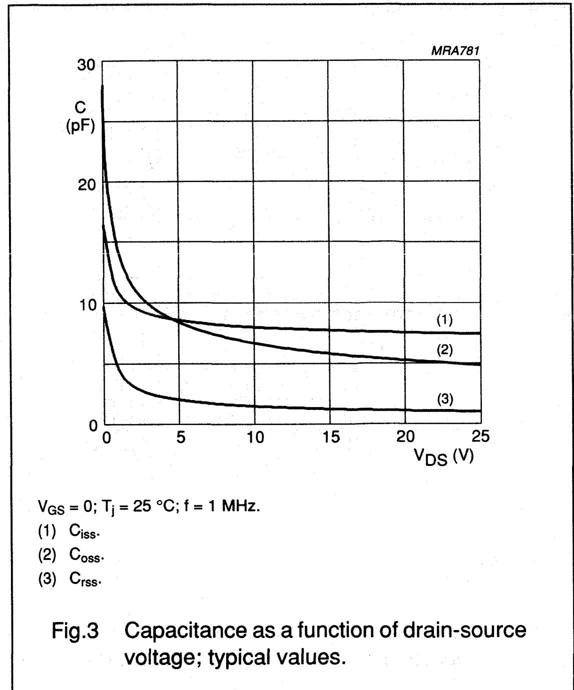
$T_j = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = 10$ µA	50	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{GS} = V_{DS}$; $I_D = 1$ mA	0.4	–	1.8	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = 40$ V	–	–	1	µA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm20$ V; $V_{DS} = 0$	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 80$ mA	–	8	15	Ω
		$V_{GS} = 5$ V; $I_D = 80$ mA	–	14	20	Ω
		$V_{GS} = 2.5$ V; $I_D = 10$ mA	–	18	30	Ω
C_{iss}	input capacitance	$V_{GS} = 0$; $V_{DS} = 10$ V; f = 1 MHz	–	8	15	pF
C_{oss}	output capacitance	$V_{GS} = 0$; $V_{DS} = 10$ V; f = 1 MHz	–	7	15	pF
C_{rss}	reverse transfer capacitance	$V_{GS} = 0$; $V_{DS} = 10$ V; f = 1 MHz	–	2	5	pF
Switching times						
t_{on}	turn-on time	$V_{GS} = 0$ to 10 V; $V_{DD} = 20$ V; $I_D = 80$ mA	–	2	5	ns
t_{off}	turn-off time	$V_{GS} = 10$ to 0 V; $V_{DD} = 20$ V; $I_D = 80$ mA	–	5	10	ns



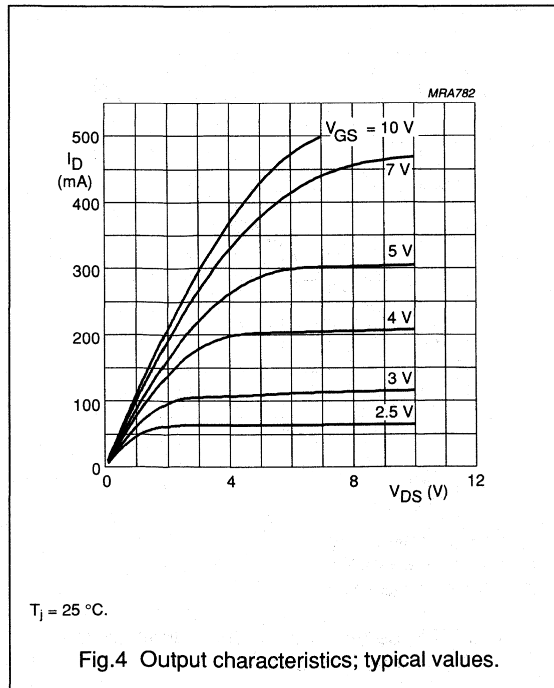
Device mounted on a printed-circuit board.

Fig.2 Power derating curve.



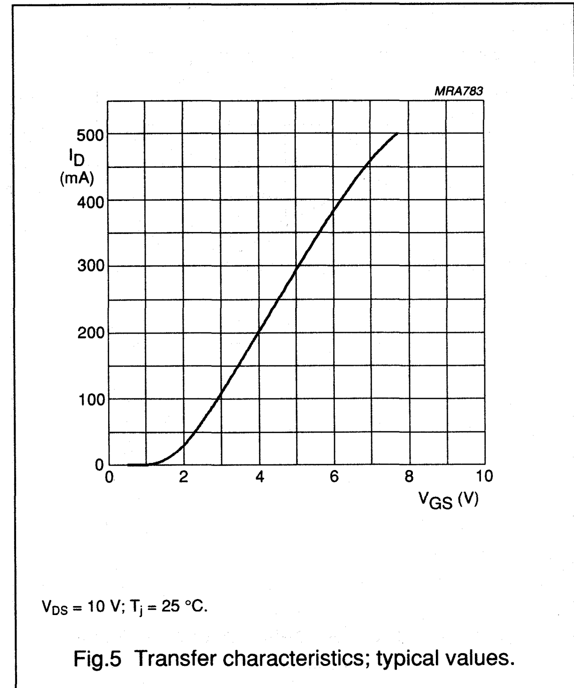
V_{GS} = 0; T_j = 25 °C; f = 1 MHz.
(1) C_{iss}.
(2) C_{oss}.
(3) C_{rss}.

Fig.3 Capacitance as a function of drain-source voltage; typical values.



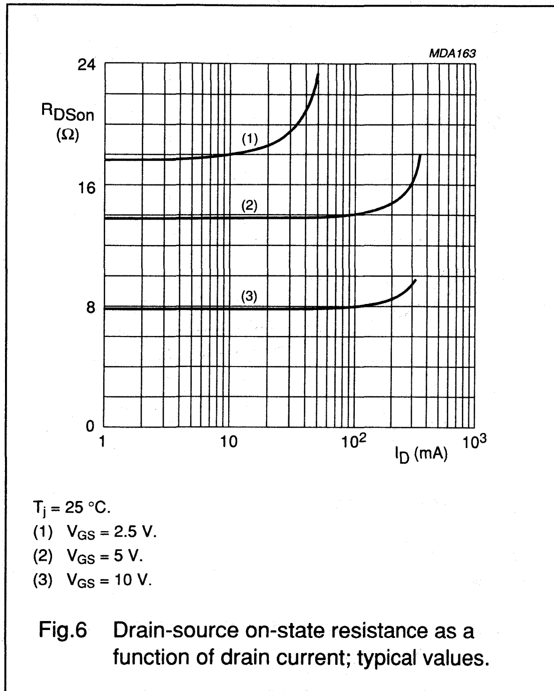
T_j = 25 °C.

Fig.4 Output characteristics; typical values.



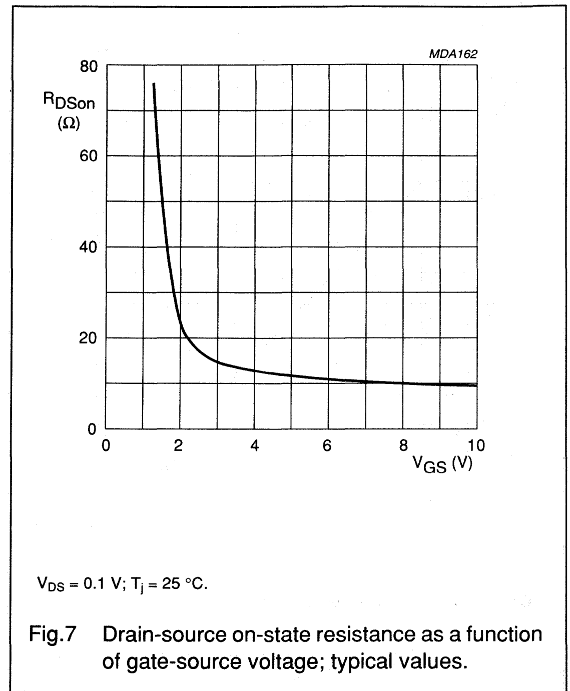
V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Transfer characteristics; typical values.



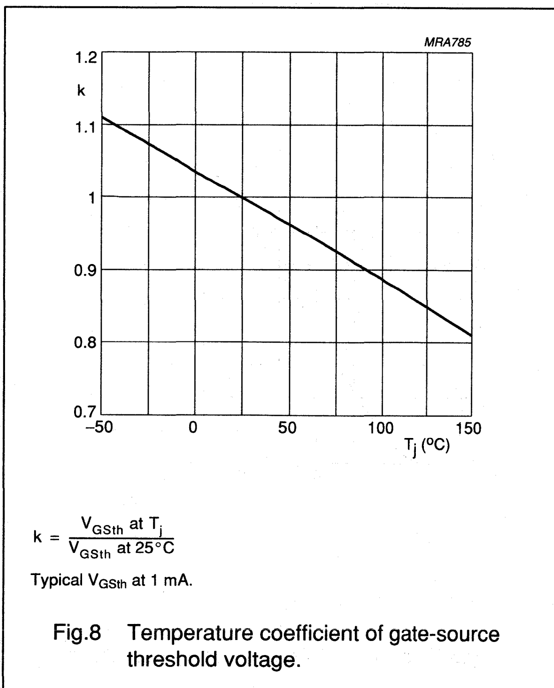
T_j = 25 °C.
(1) V_{GS} = 2.5 V.
(2) V_{GS} = 5 V.
(3) V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of drain current; typical values.



V_{DS} = 0.1 V; T_j = 25 °C.

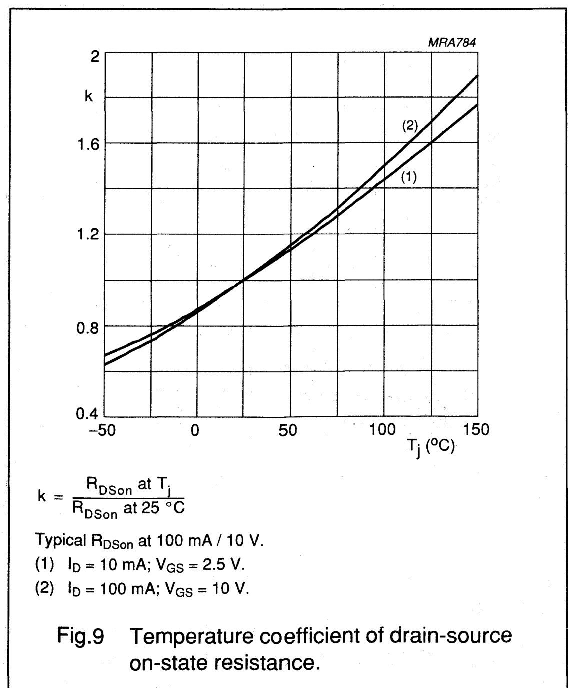
Fig.7 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

Typical V_{GSth} at 1 mA.

Fig.8 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

Typical R_{DSon} at 100 mA / 10 V.
(1) I_D = 10 mA; V_{GS} = 2.5 V.
(2) I_D = 100 mA; V_{GS} = 10 V.

Fig.9 Temperature coefficient of drain-source on-state resistance.

N-channel enhancement mode vertical D-MOS transistor

BSN205; BSN205A

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope. Designed primarily as a line current interrupter in telephone sets, it can also be applied in other applications such as in relays, line and high speed transformer drivers etc.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown
- Low $R_{DS(on)}$

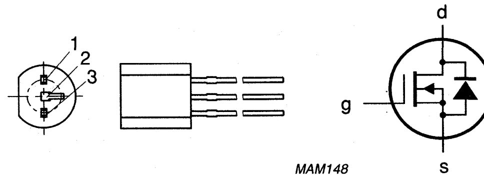
QUICK REFERENCE DATA

Parameter	Symbol		Value	Unit
Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	4.5	Ω
		max.	6	Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\|Y_{fs}\|$	min.	200	mS
		typ.	350	mS

PINNING - TO-92 VARIANT

BSN205		BSN205A	
1	= gate	1	= source
2	= drain	2	= gate
3	= source	3	= drain

PIN CONFIGURATION



Note: various pinout configurations available.

Fig.1 Simplified outline and symbol.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Drain current (peak)	I_{DM}	max.	1.2	A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

Note

1. Transistor mounted on printed-circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm × 10 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)\ DSS}$	min.	200	V
Drain-source leakage current V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	max.	1	μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 2.8	V V
Drain-source ON-resistance I_D = 400 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	4 6	Ω Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert Y_{fs} \rvert$	min. typ.	200 350	mS mS
Input capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ. max.	45 60	pF pF

Output capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ. max.	15 pF 25 pF
Feedback capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ. max.	3.5 pF 10 pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V V_{GS} = 0 to 10 V	t_{on}	typ. max.	5 ns 10 ns
	t_{off}	typ. max.	15 ns 20 ns

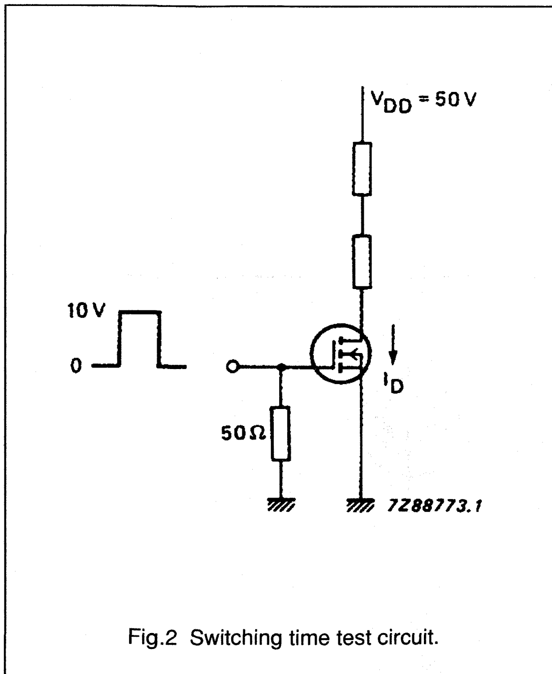


Fig.2 Switching time test circuit.

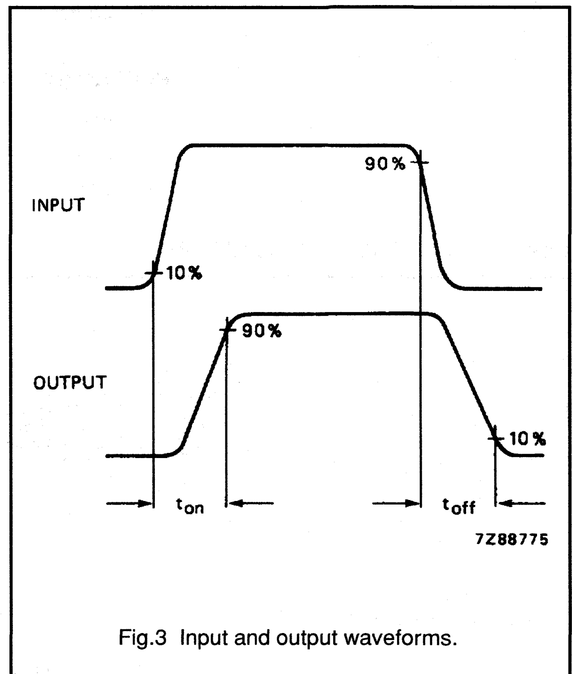


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistors

BSN254 BSN254A

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistors in TO-92 variant envelope and designed for use as line current interrupters in telephone sets and for application in relay, high-speed and line-transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low $R_{DS\ (on)}$

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	250	V
Drain current (DC)	I_D	max.	300	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source on-resistance				
I_D = 300 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	5.0	Ω
		max.	7.0	Ω
Gate-source threshold voltage	$V_{GS(th)}$	max.	2	V

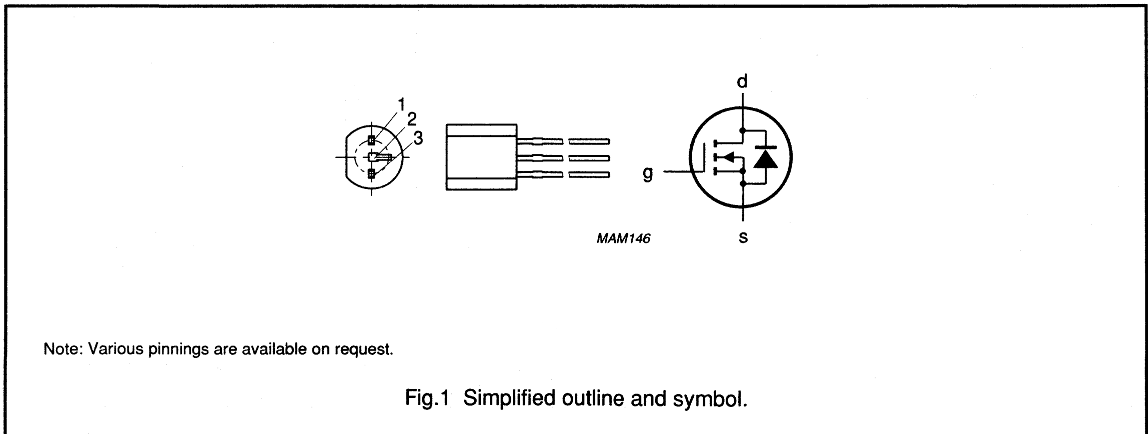
PINNING (BSN254)

1 = gate
2 = drain
3 = source

PINNING (BSN254A)

1 = source
2 = gate
3 = drain

PIN CONFIGURATION - TO-92 VARIANT



Note: Various pinnings are available on request.

Fig.1 Simplified outline and symbol.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	250	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Drain current (peak)	I_{DM}	max.	1.2	A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}	−65 to + 150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j-a}$	=	125	K/W

Note

1. Device mounted on printed-circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm × 10 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 µA; V_{GS} = 0	$V_{(BR)\ DSS}$	min.	250	V
Drain-source leakage current V_{DS} = 200 V; V_{GS} = 0	I_{DSS}	max.	1	µA
Gate-source leakage current $\pm V_{GS}$ = 20 V; V_{DS} = 0	$\pm I_{GSS}$	max.	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	0.8 2.0	V V
Drain-source on-resistance I_D = 300 mA; V_{GS} = 10 V	$R_{DS\ (on)}$	typ. max.	5.0 7.0	Ω Ω
I_D = 20 mA; V_{GS} = 2.4 V	$R_{DS(on)}$	max.	10	Ω
Transfer admittance I_D = 300 mA; V_{DS} = 25 V	$\lvert Y_{fs} \rvert$	min. typ.	200 400	mS mS
Input capacitance at f = 1 MHz V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ. max.	65 90	pF pF

Output capacitance at f = 1 MHz			
V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ.	20 pF
		max.	30 pF
Feedback capacitance at f = 1 MHz			
V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ.	5 pF
		max.	15 pF
Switching times (see Figs 2 and 3)			
I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	5 ns
		max.	10 ns
	t_{off}	typ.	20 ns
		max.	30 ns

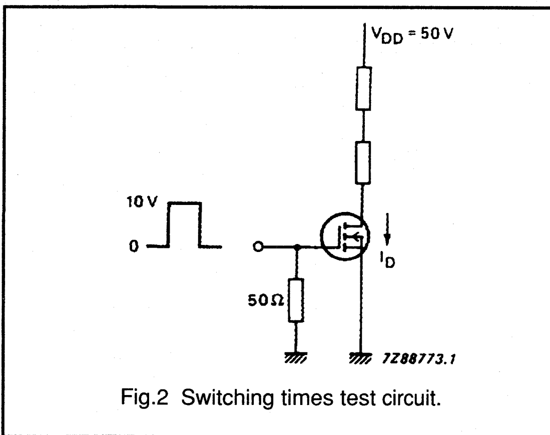


Fig.2 Switching times test circuit.

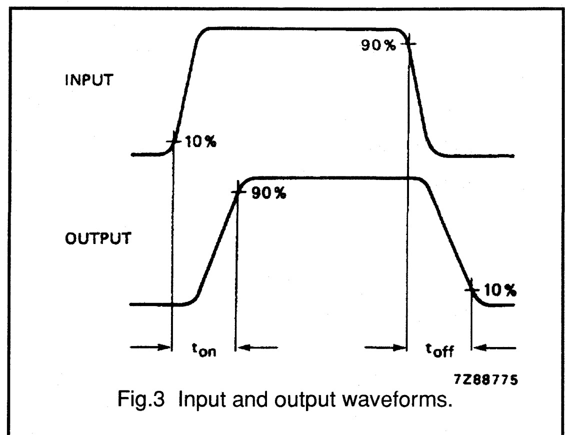


Fig.3 Input and output waveforms.

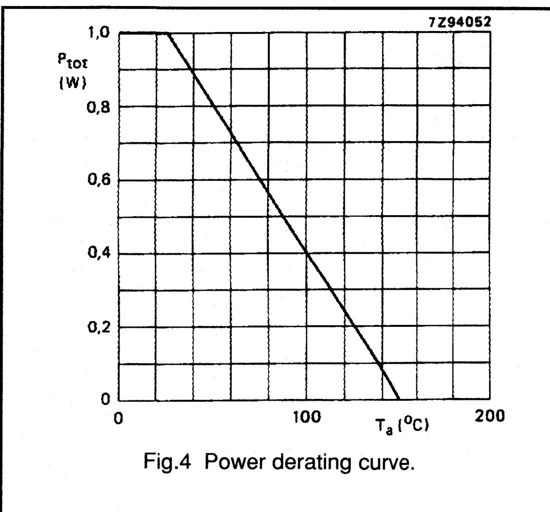


Fig.4 Power derating curve.

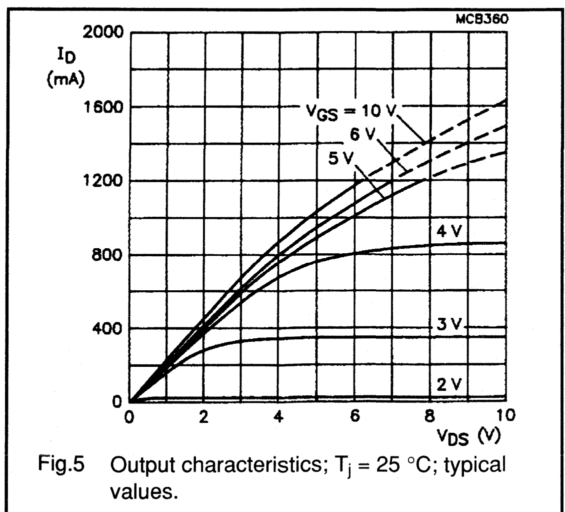


Fig.5 Output characteristics; T_j = 25 °C; typical values.

N-channel enhancement mode vertical D-MOS transistors

BSN254
BSN254A

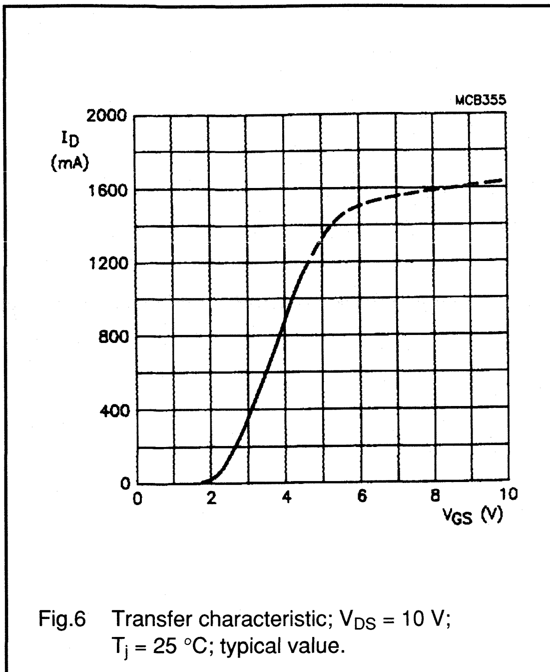


Fig.6 Transfer characteristic; V_{DS} = 10 V; T_j = 25 °C; typical value.

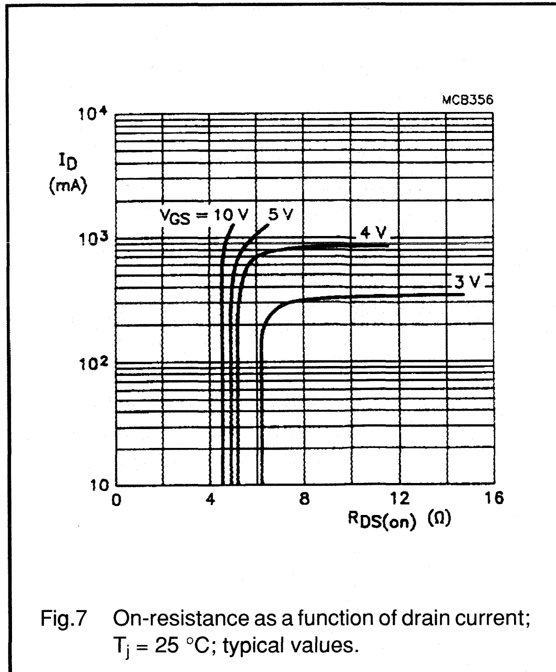


Fig.7 On-resistance as a function of drain current; T_j = 25 °C; typical values.

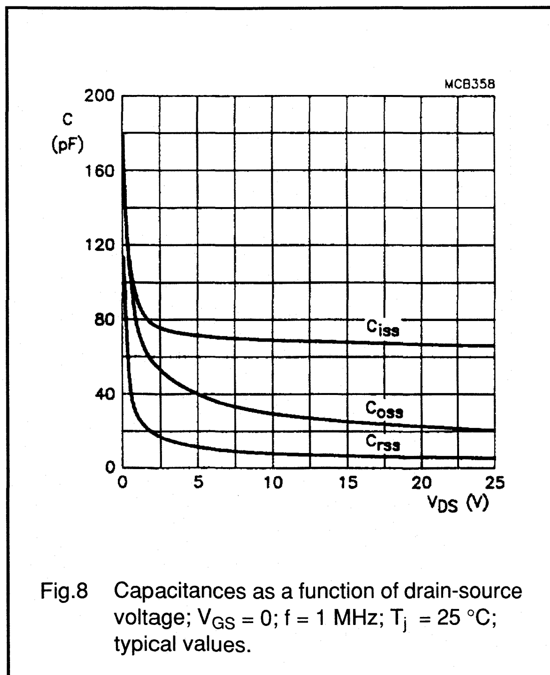


Fig.8 Capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C; typical values.

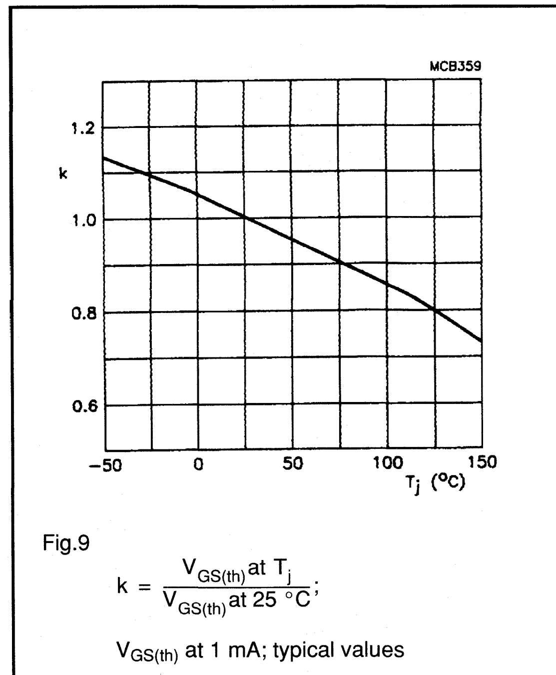


Fig.9

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C};$$

$V_{GS(th)}$ at 1 mA; typical values

N-channel enhancement mode vertical D-MOS transistors

BSN254 BSN254A

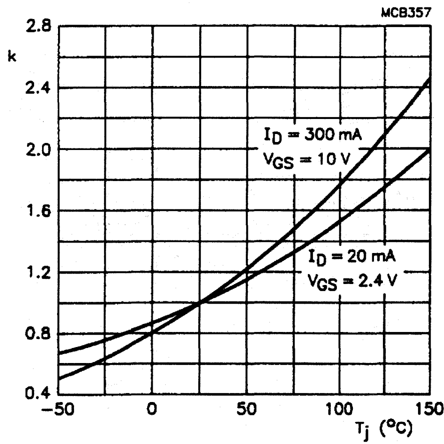


Fig.10

$$k = \frac{R_{DS\,(on)}\text{ at }T_j}{R_{DS\,(on)}\text{ at }25\ °C};$$

typical values.

N-channel enhancement mode vertical D-MOS transistor

BSN274; BSN274A

FEATURES

- Direct interface to C-MOS, TTL, etc., due to low threshold voltage
- High speed switching
- No secondary breakdown

DESCRIPTION

Silicon n-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high speed and line transformer drivers.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	270	V
I_D	drain current (DC)	250	mA
$R_{DS(on)}$	drain-source on-resistance	8	Ω
$V_{GS(th)}$	threshold voltage	2	V

PINNING (BSN274)

PIN	DESCRIPTION
1	gate
2	drain
3	source

PINNING (BSN274A)

PIN	DESCRIPTION
1	source
2	gate
3	drain

Note: Other pinnings are available on request.

PIN CONFIGURATION - TO-92 VARIANT

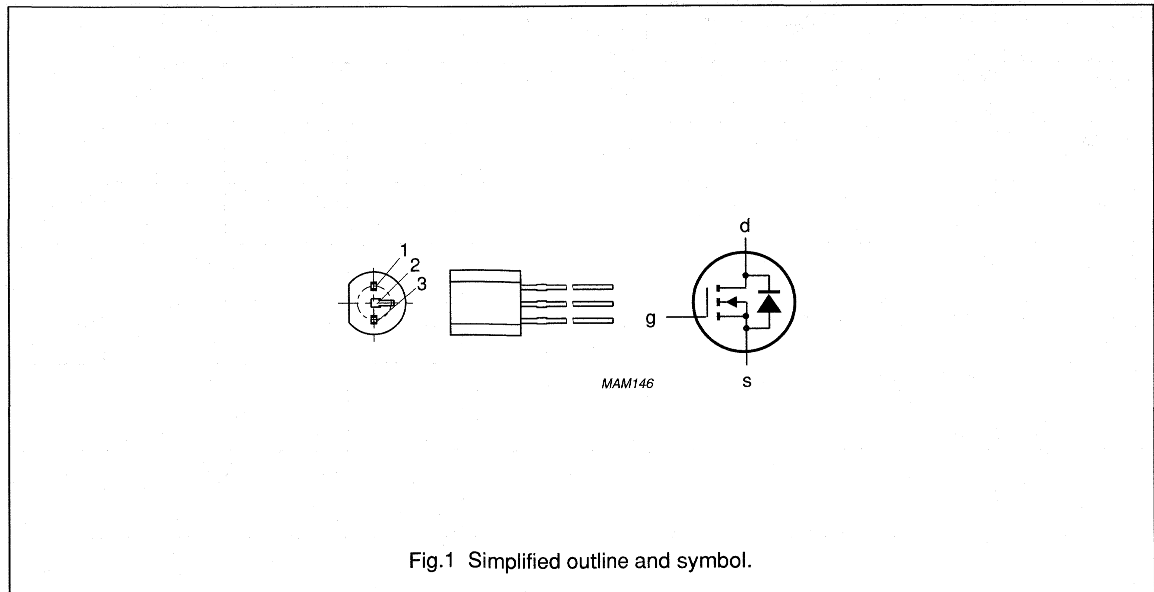


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	270	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	drain current	DC	–	250	mA
I_{DM}	drain current	peak	–	1	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1	W
T_{stg}	storage temperature range		−65	150	°C
T_j	operating junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125	K/W

Notes

1. Transistor mounted on printed circuit board, maximum lead length 4 mm, mounting pad for drain leads minimum 10 mm × 10 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 I_D = 10 μA	270	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 220 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate threshold voltage	I_D = 1 mA V_{DS} = V_{GS}	0.8	–	2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 250 mA V_{GS} = 10 V	–	6.5	8	Ω
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA V_{GS} = 2.4 V	–	9	14	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA V_{DS} = 25 V	200	400	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	65	90	pF
C_{oss}	output capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	20	30	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{rss}	feedback capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	5	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	switching-on time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	5	10	ns
t_{off}	switching-off time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	20	30	ns

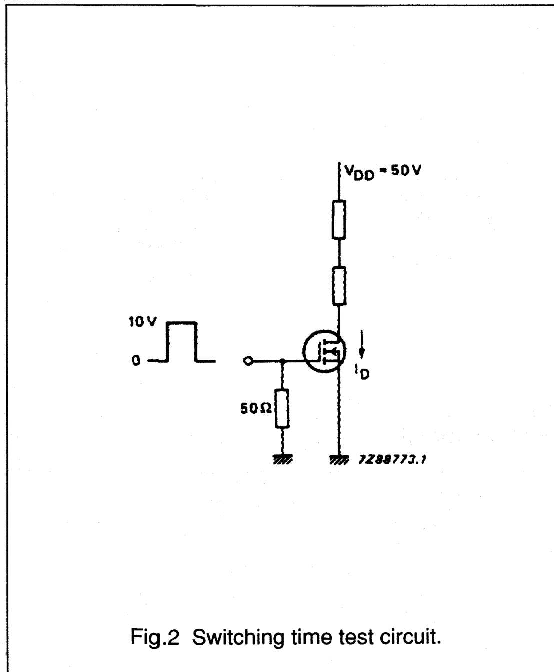


Fig.2 Switching time test circuit.

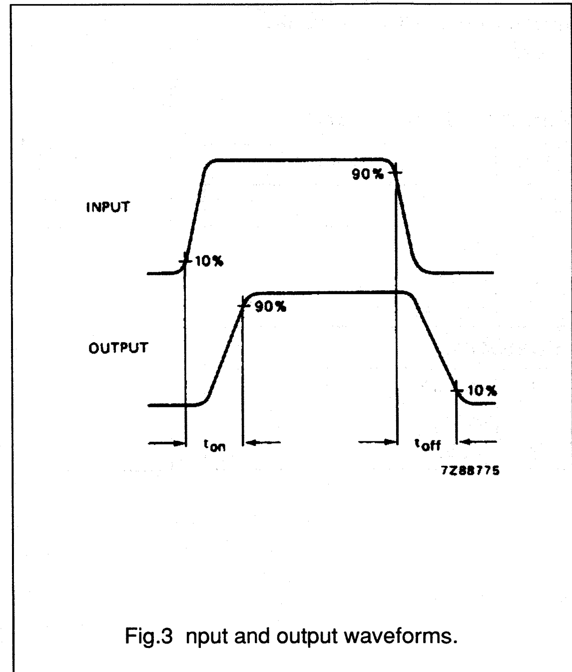


Fig.3 nput and output waveforms.

N-channel enhancement mode vertical D-MOS transistors

BSN304; BSN304A

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant

PIN	DESCRIPTION
BSN304	
1	gate
2	drain
3	source
BSN304A	
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	
V_{DS}	drain-source voltage		–	300	V
I_D	DC drain current		–	250	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	1	W
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 250 mA; V_{GS} = 10 V	–	8	Ω
$V_{GS(off)}$	gate-source cut-off voltage	I_D = 1 mA; $V_{GS} = V_{DS}$	0.8	2	V

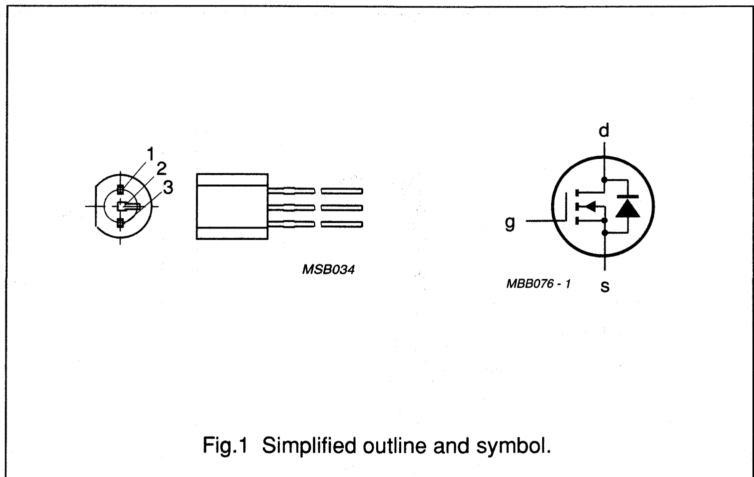


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	300	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	250	mA
I_{DM}	peak drain current		–	1	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	1	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient; note 1	125 K/W

Note

1. Device mounted on an epoxy printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm^2.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	300	–	–	V
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}	0.8	–	2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 250 mA; V_{GS} = 10 V	–	6.7	8	Ω
		I_D = 20 mA; V_{GS} = 2.4 V	–	7.9	14	Ω
I_{DSS}	drain-source leakage current	V_{DS} = 240 V; V_{GS} = 0	–	–	100	nA
$\|Y_{fs}\|$	transfer admittance	I_D = 250 mA; V_{DS} = 25 V	200	380	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	57	90	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	15	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	2.6	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	2.5	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 10 to 0 V	–	17	30	ns

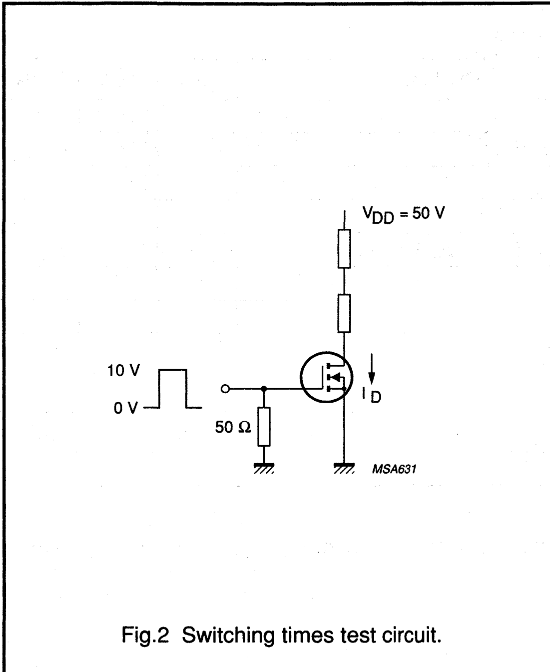


Fig.2 Switching times test circuit.

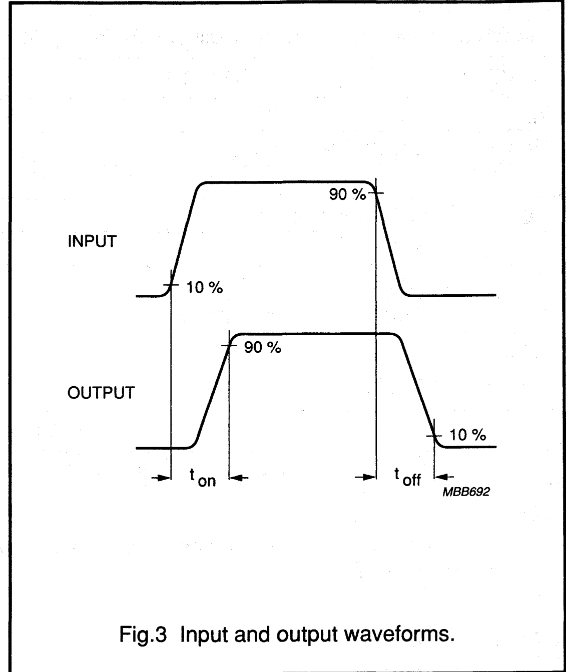


Fig.3 Input and output waveforms.

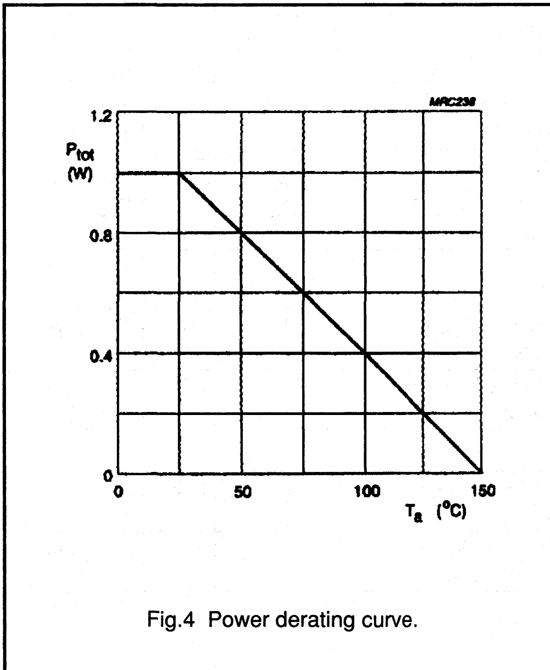
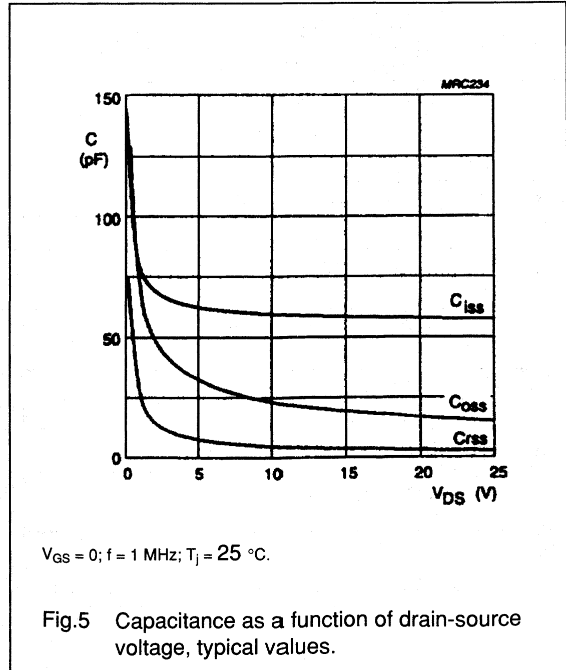
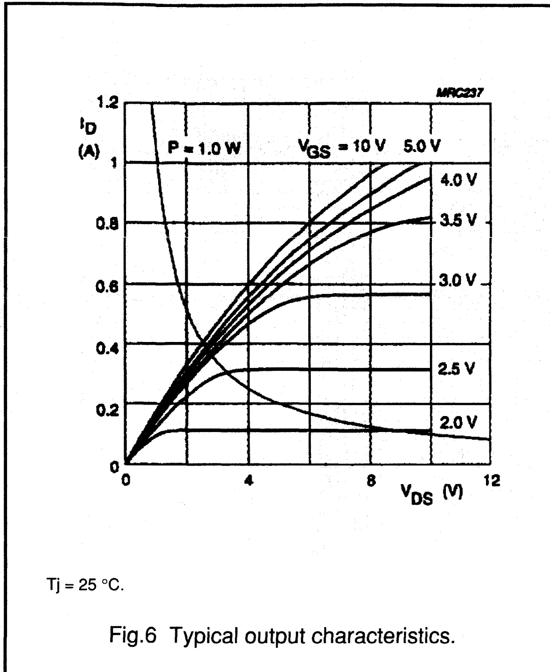


Fig.4 Power derating curve.



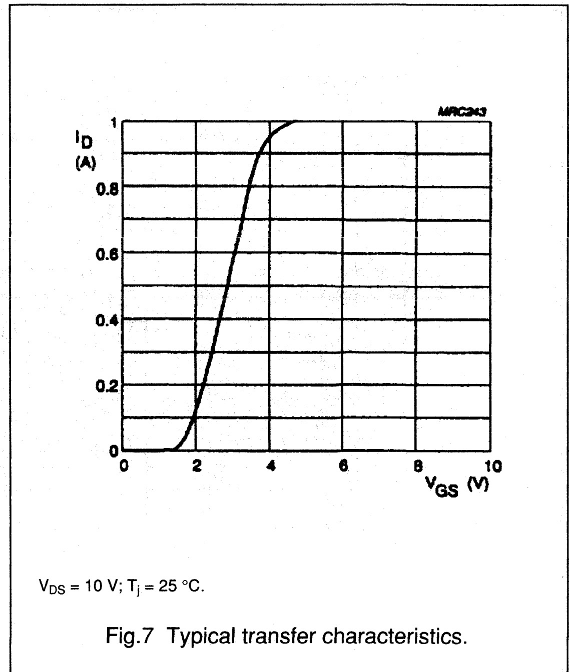
V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.5 Capacitance as a function of drain-source voltage, typical values.



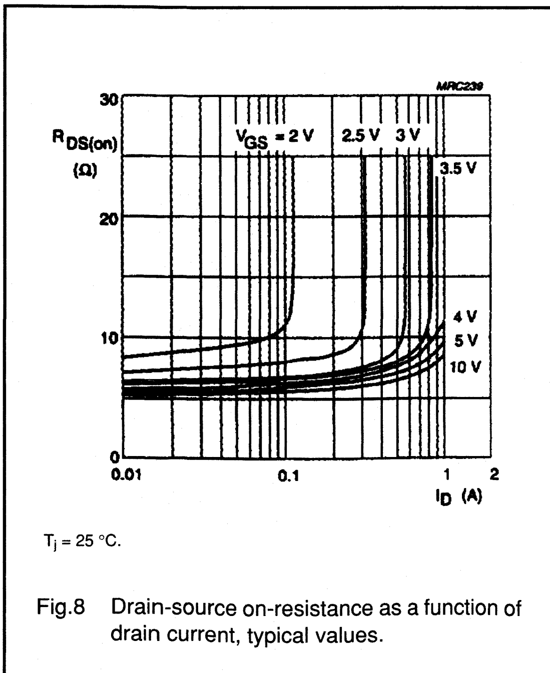
T_j = 25 °C.

Fig.6 Typical output characteristics.



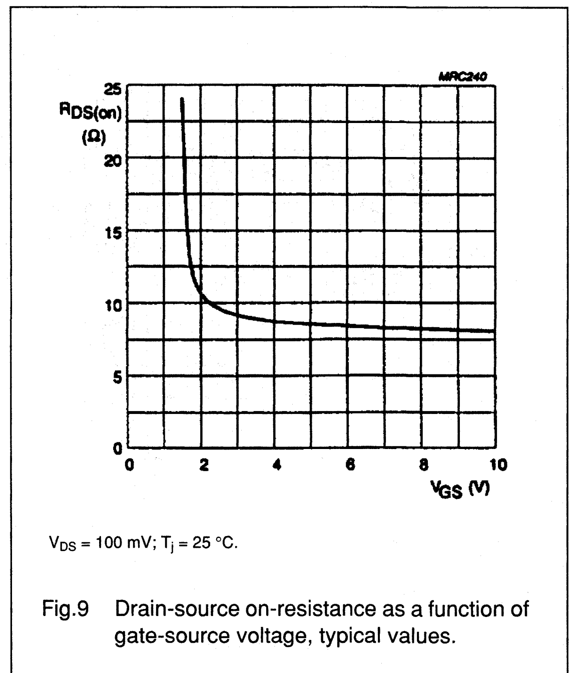
V_{DS} = 10 V; T_j = 25 °C.

Fig.7 Typical transfer characteristics.



T_j = 25 °C.

Fig.8 Drain-source on-resistance as a function of drain current, typical values.



V_{DS} = 100 mV; T_j = 25 °C.

Fig.9 Drain-source on-resistance as a function of gate-source voltage, typical values.

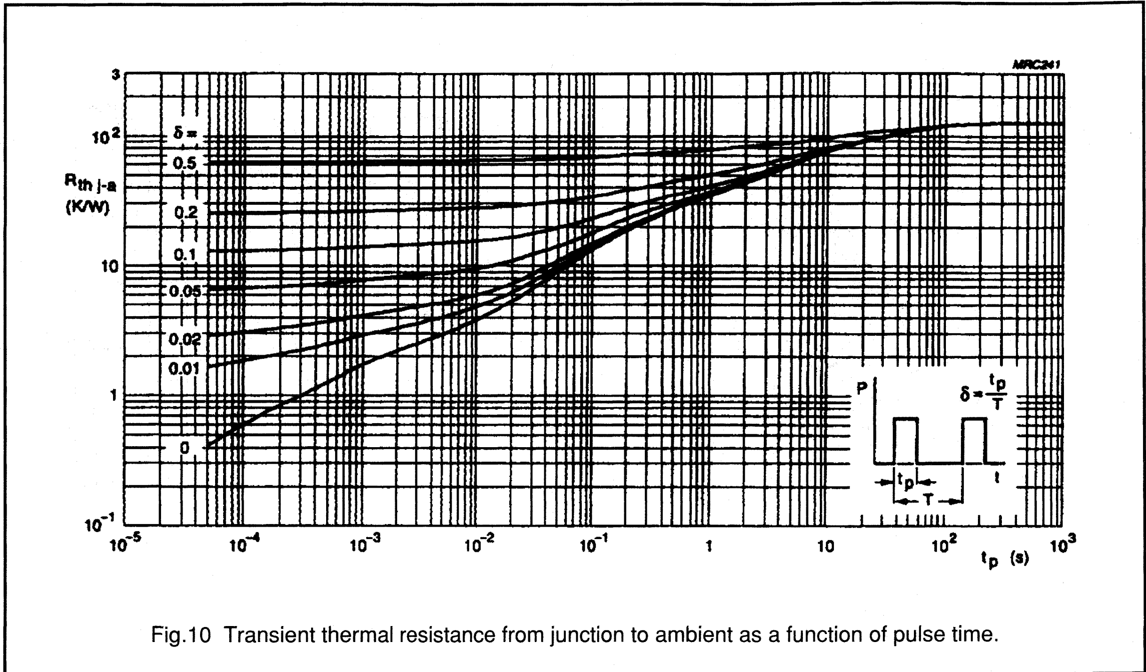
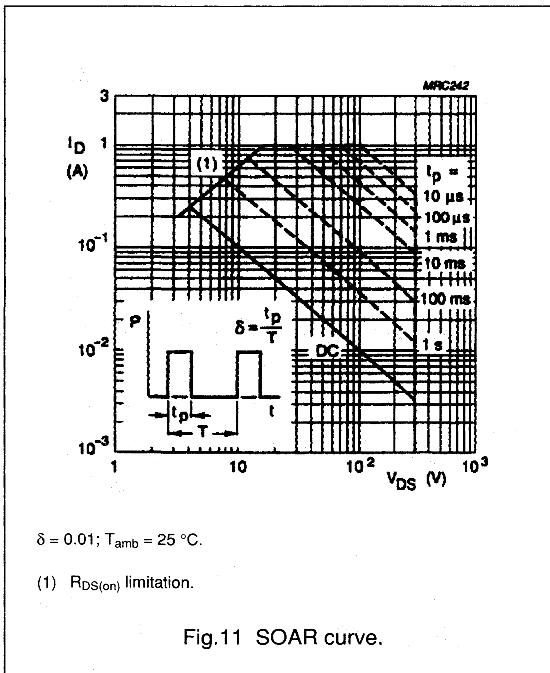


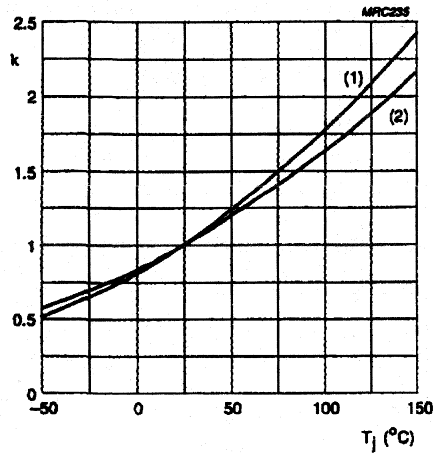
Fig.10 Transient thermal resistance from junction to ambient as a function of pulse time.



$\delta = 0.01$; $T_{amb} = 25$ °C.

(1) $R_{DS(on)}$ limitation.

Fig.11 SOAR curve.

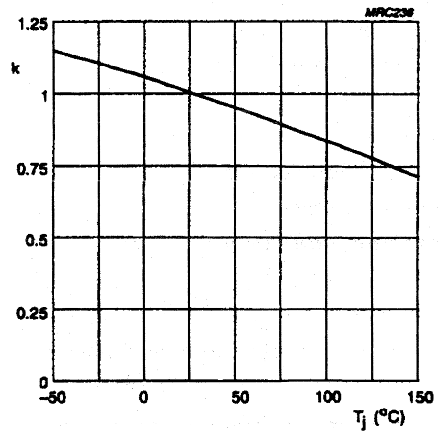


$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$.

Typical $R_{DS(on)}$;

(1) $I_D = 250$ mA; $V_{GS} = 10$ V.
(2) $I_D = 20$ mA; $V_{GS} = 2.4$ V.

Fig.12 Temperature coefficient of drain-source on-resistance.



$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}$.

Fig.13 Temperature coefficient of gate-source threshold voltage.

N-channel enhancement mode vertical D-MOS transistor

BSP030

FEATURES

- High speed switching
- No secondary breakdown
- Very low on-state resistance.

APPLICATIONS

- Motor and actuator drivers
- Power management
- Synchronized rectification.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a 4-pin plastic SOT223 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT223

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source
4	d	drain

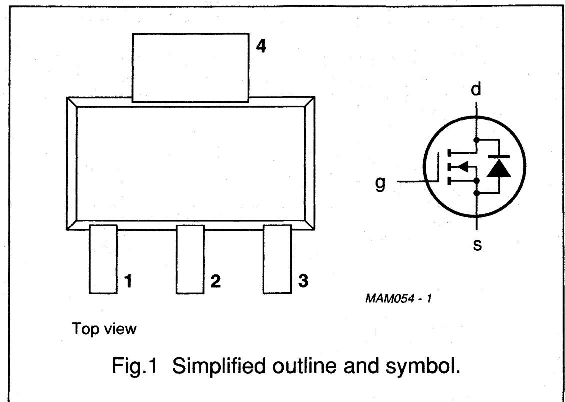


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{SD}	source-drain diode forward voltage	$I_S = 1.25$ A	–	1	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	$I_D = 1$ mA; $V_{DS} = V_{GS}$	1	2.8	V
I_D	drain current (DC)	$T_s = 100$ °C	–	10	A
R_{DSon}	drain-source on-state resistance	$I_D = 5$ A; $V_{GS} = 10$ V	–	0.03	Ω
P_{tot}	total power dissipation	$T_s = 100$ °C	–	5	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 100 °C; note 1	–	10	A
I_{DM}	peak drain current	note 2	–	40	A
P_{tot}	total power dissipation	T_s = 100 °C	–	5	W
		T_{amb} = 25 °C; note 3	–	3.3	W
		T_{amb} = 25 °C; note 4	–	1.25	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–65	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 100 °C	–	5	A
I_{SM}	peak pulsed source current	note 2	–	20	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Value based on printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Value based on printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	10	K/W

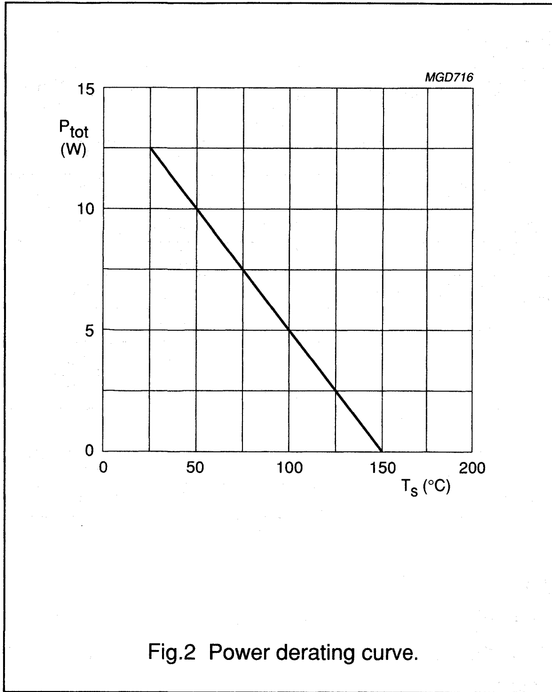
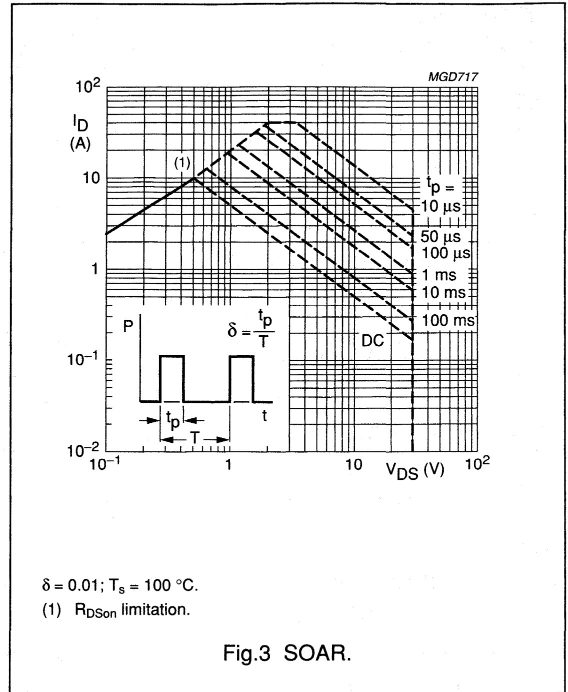


Fig.2 Power derating curve.



δ = 0.01; T_s = 100 °C.

(1) R_{DSon} limitation.

Fig.3 SOAR.

CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 24 V	–	–	500	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 2.5 A	–	–	0.05	Ω
		V_{GS} = 10 V; I_D = 5 A	–	–	0.03	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	750	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	450	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	200	–	pF
Q_g	total gate charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 5 A; T_{amb} = 25 °C	–	28	–	nC
Q_{gs}	gate-source charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 5 A; T_{amb} = 25 °C	–	2.5	–	nC
Q_{gd}	gate-drain charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 5 A; T_{amb} = 25 °C	–	10.5	–	nC
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	14	–	ns
t_f	fall time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	18	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	32	60	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	29	–	ns
t_r	rise time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	33	–	ns
t_{off}	turn-off switching time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	62	150	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 1.25 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 1.25 A; di/dt = −100 A/μs	–	70	–	ns

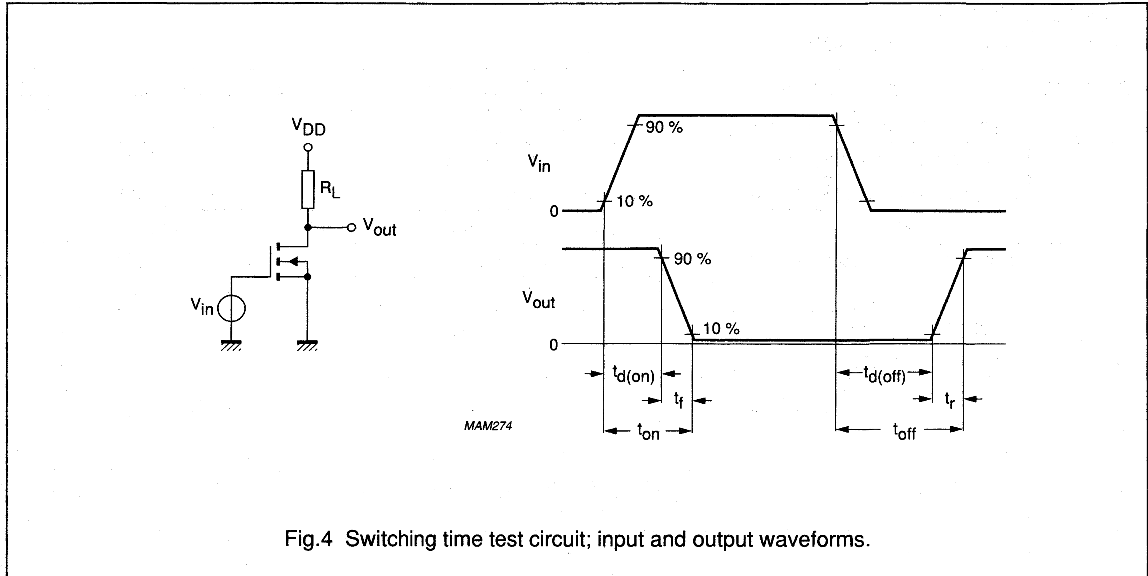


Fig.4 Switching time test circuit; input and output waveforms.

MGD718

$R_{th\ j-s}$ (K/W)

δ = 0.75, 0.5, 0.33, 0.2, 0.1, 0.05, 0.02, 0.01, 0

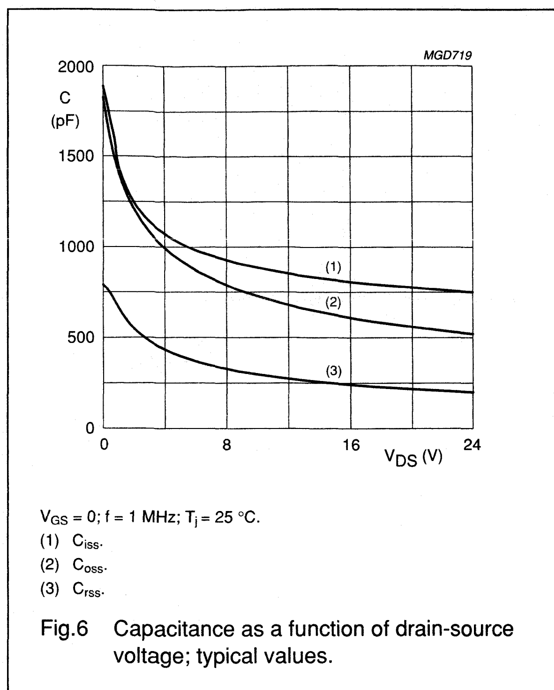
10^2, 10, 1, 10^{-1}

10^{-5}, 10^{-4}, 10^{-3}, 10^{-2}, 10^{-1}, 1, 10

t_p (s)

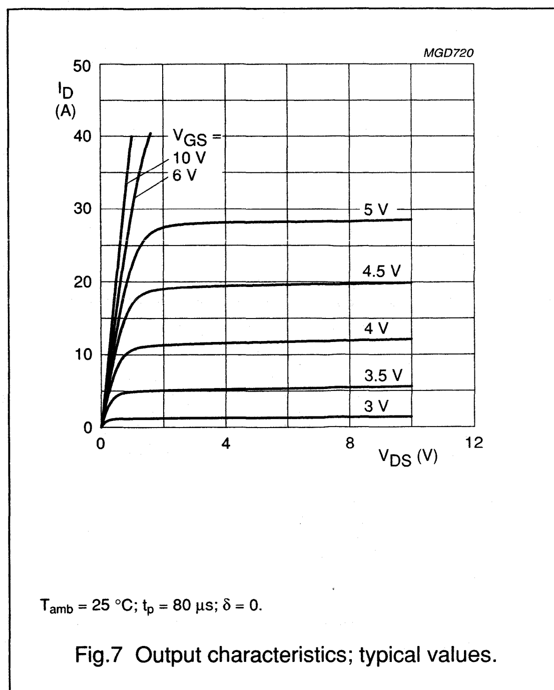
P, $\delta = \frac{t_p}{T}$, t_p, T, t

Fig.5 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.



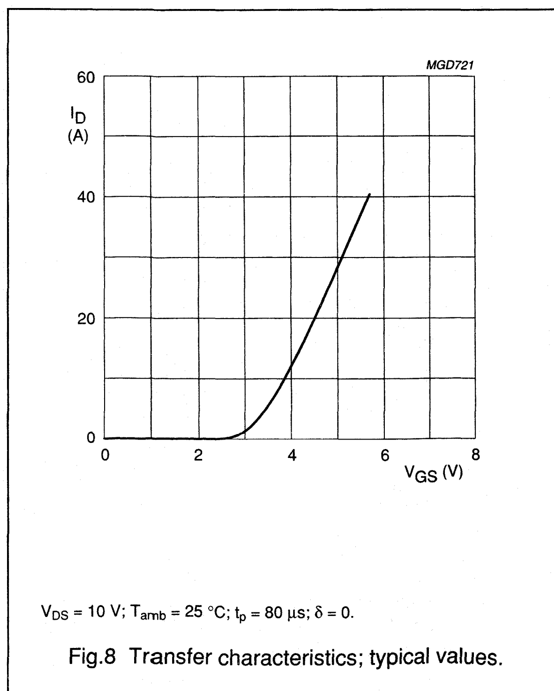
V_{GS} = 0; f = 1 MHz; T_j = 25 °C.
(1) C_{iss}.
(2) C_{oss}.
(3) C_{rss}.

Fig.6 Capacitance as a function of drain-source voltage; typical values.



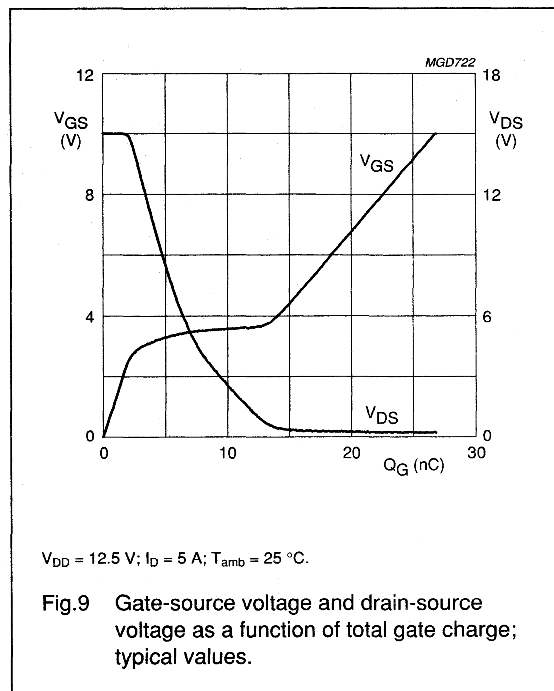
T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

Fig.7 Output characteristics; typical values.



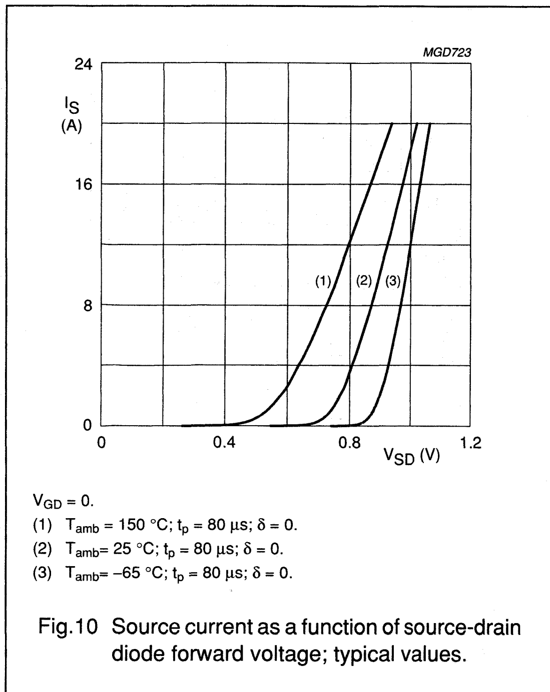
V_{DS} = 10 V; T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

Fig.8 Transfer characteristics; typical values.



V_{DD} = 12.5 V; I_D = 5 A; T_{amb} = 25 °C.

Fig.9 Gate-source voltage and drain-source voltage as a function of total gate charge; typical values.



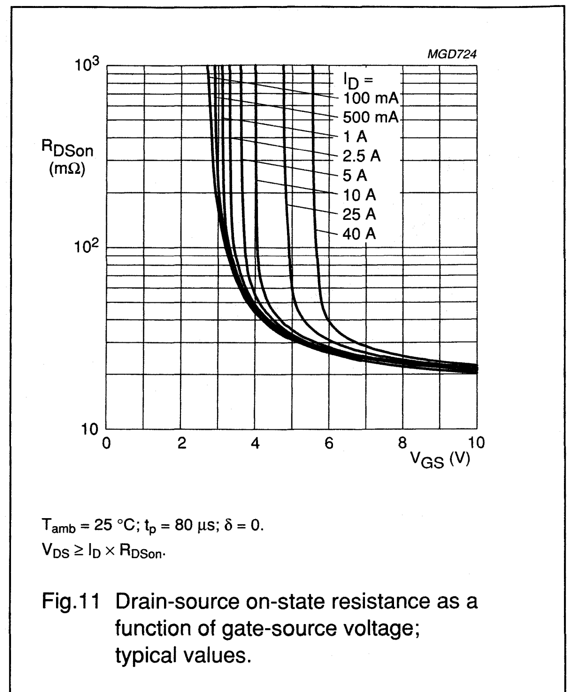
$V_{GD} = 0$.

(1) $T_{amb} = 150\ °C$; $t_p = 80\ \mu s$; $\delta = 0$.

(2) $T_{amb} = 25\ °C$; $t_p = 80\ \mu s$; $\delta = 0$.

(3) $T_{amb} = -65\ °C$; $t_p = 80\ \mu s$; $\delta = 0$.

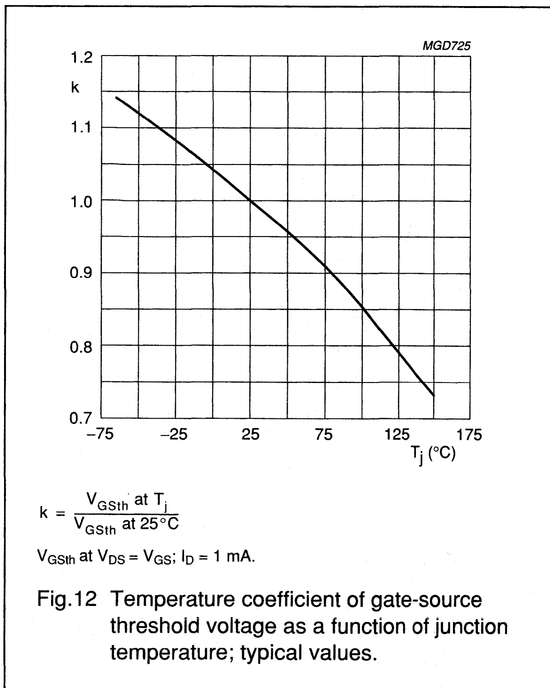
Fig.10 Source current as a function of source-drain diode forward voltage; typical values.



$T_{amb} = 25\ °C$; $t_p = 80\ \mu s$; $\delta = 0$.

$V_{DS} \geq I_D \times R_{DSon}$.

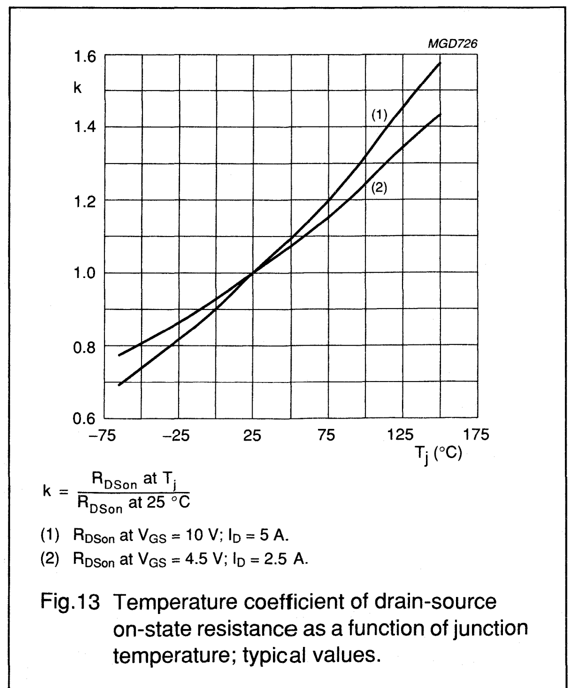
Fig.11 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth}\ \text{at}\ T_j}{V_{GSth}\ \text{at}\ 25°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; $I_D = 1$ mA.

Fig.12 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; typical values.



$$k = \frac{R_{DSon}\ \text{at}\ T_j}{R_{DSon}\ \text{at}\ 25\ °C}$$

(1) R_{DSon} at $V_{GS} = 10$ V; $I_D = 5$ A.

(2) R_{DSon} at $V_{GS} = 4.5$ V; $I_D = 2.5$ A.

Fig.13 Temperature coefficient of drain-source on-state resistance as a function of junction temperature; typical values.

P-channel enhancement mode vertical D-MOS transistor

BSP090

FEATURES

- High speed switching
- No secondary breakdown
- Very low on-state resistance.

APPLICATIONS

- Motor and actuator drivers
- Power management
- Synchronized rectification.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a 4-pin plastic SOT223 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT223

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source
4	d	drain

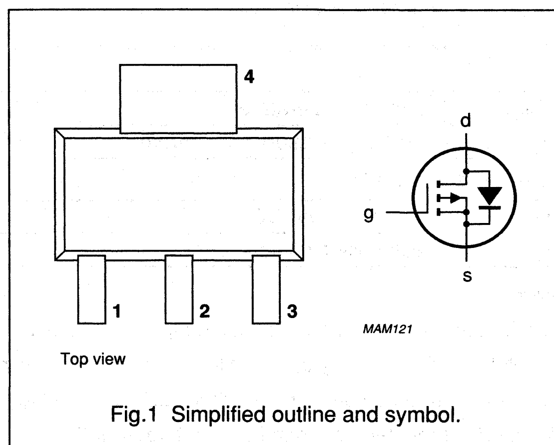


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	I_S = –1.25 A	–	–1.3	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = –1 mA; $V_{DS} = V_{GS}$	–1	–2.8	V
I_D	drain current (DC)	T_s = 100 °C	–	–5.7	A
R_{DSon}	drain-source on-state resistance	I_D = –2.8 A; V_{GS} = –10 V	–	0.09	Ω
P_{tot}	total power dissipation	T_s = 100 °C	–	5	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 100 °C; note 1	–	–5.7	A
I_{DM}	peak drain current	note 2	–	–22	A
P_{tot}	total power dissipation	T_s = 100 °C	–	5	W
		T_{amb} = 25 °C; note 3	–	3.3	W
		T_{amb} = 25 °C; note 4	–	1.25	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–65	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 100 °C	–	–3.8	A
I_{SM}	peak pulsed source current	note 2	–	–15	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	10	K/W

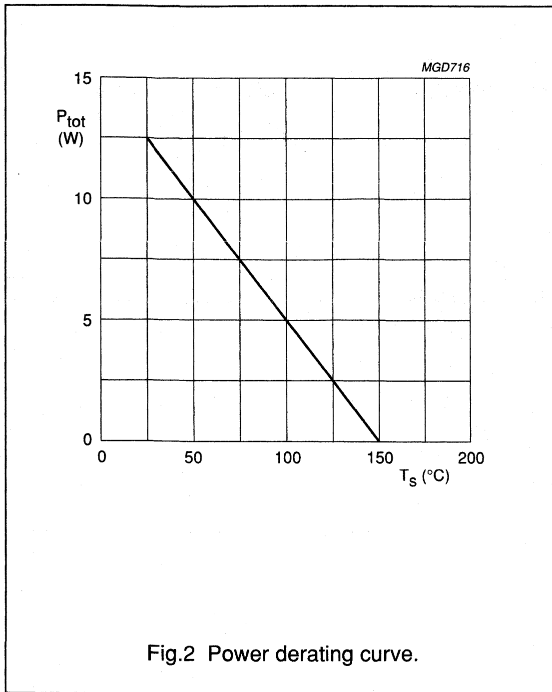
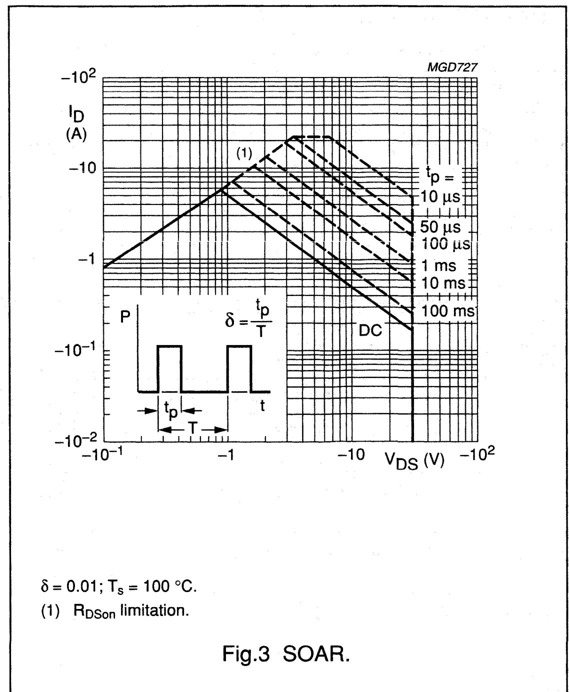


Fig.2 Power derating curve.



δ = 0.01; T_s = 100 °C.

(1) R_{DSon} limitation.

Fig.3 SOAR.

CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−1	–	−2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −24 V	–	–	−500	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −1.4 A	–	–	0.15	Ω
		V_{GS} = −10 V; I_D = −2.8 A	–	–	0.09	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	800	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	400	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	100	–	pF
Q_g	total gate charge	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −2.8 A; T_{amb} = 25 °C	–	21	–	nC
Q_{gs}	gate-source charge	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −2.8 A; T_{amb} = 25 °C	–	2.5	–	nC
Q_{gd}	gate-drain charge	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −2.8 A; T_{amb} = 25 °C	–	6	–	nC
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	6	–	ns
t_r	rise time	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	6	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	12	25	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	55	–	ns
t_f	fall time	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	40	–	ns
t_{off}	turn-off switching time	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	95	190	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = −1.25 A	–	–	−1.3	V
t_{rr}	reverse recovery time	I_S = −1.25 A; di/dt = 100 A/μs	–	70	–	ns

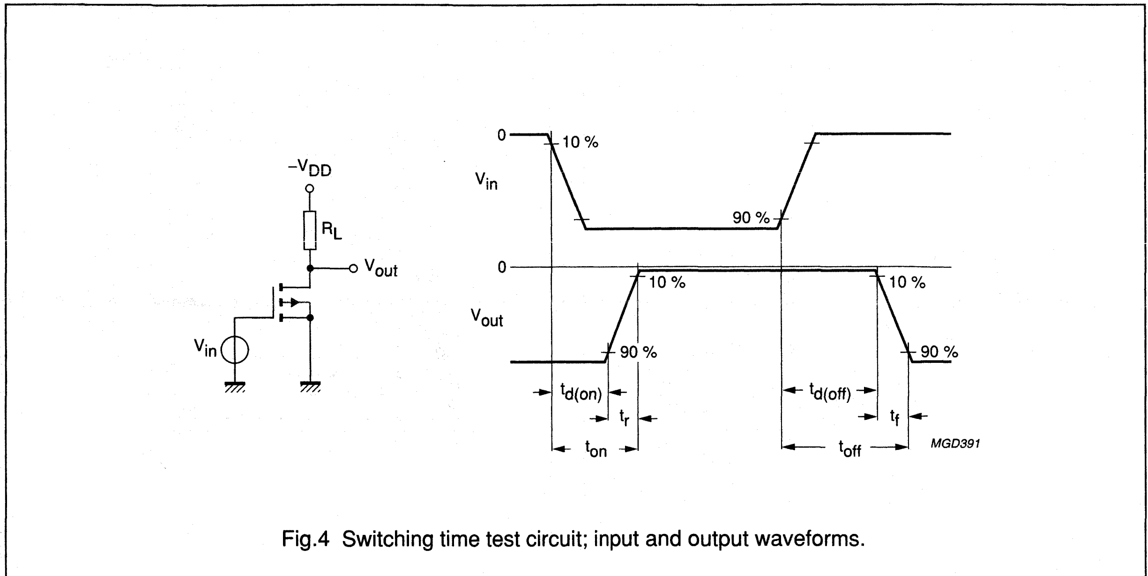
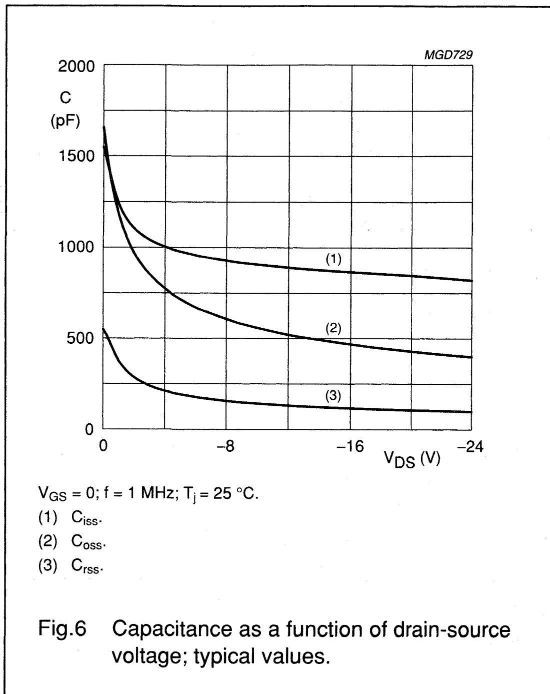


Fig.4 Switching time test circuit; input and output waveforms.

Fig.5 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.



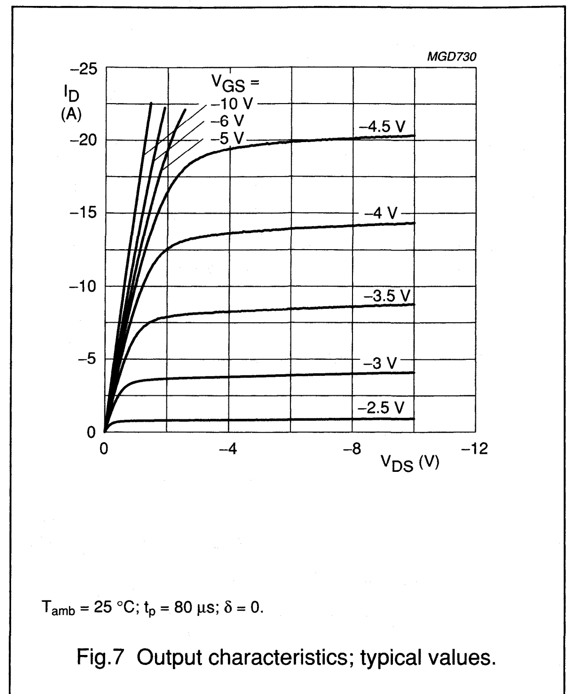
$V_{GS} = 0$; f = 1 MHz; $T_j = 25$ °C.

(1) C_{iss}.

(2) C_{oss}.

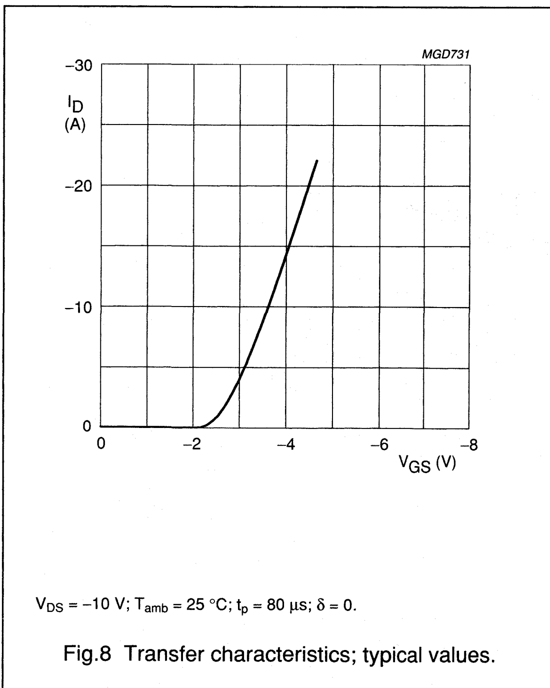
(3) C_{rss}.

Fig.6 Capacitance as a function of drain-source voltage; typical values.



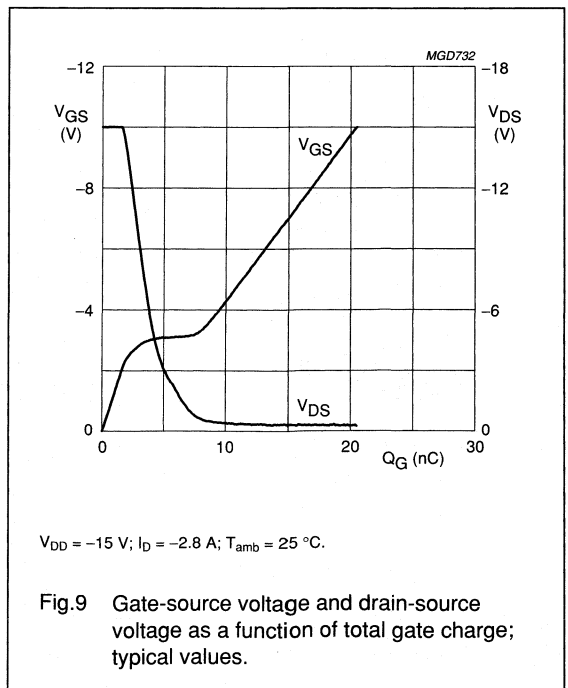
$T_{amb} = 25$ °C; $t_p = 80$ µs; δ = 0.

Fig.7 Output characteristics; typical values.



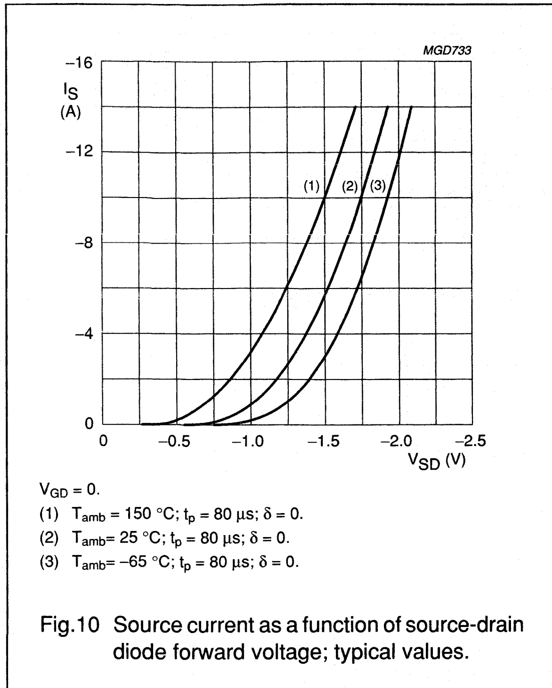
$V_{DS} = -10$ V; $T_{amb} = 25$ °C; $t_p = 80$ µs; δ = 0.

Fig.8 Transfer characteristics; typical values.



$V_{DD} = -15$ V; $I_D = -2.8$ A; $T_{amb} = 25$ °C.

Fig.9 Gate-source voltage and drain-source voltage as a function of total gate charge; typical values.



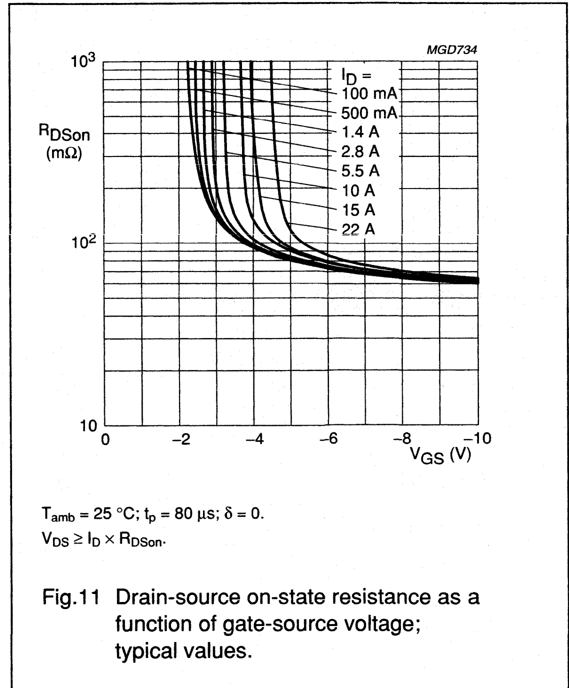
$V_{GD} = 0$.

(1) $T_{amb} = 150$ °C; $t_p = 80$ µs; $\delta = 0$.

(2) $T_{amb} = 25$ °C; $t_p = 80$ µs; $\delta = 0$.

(3) $T_{amb} = -65$ °C; $t_p = 80$ µs; $\delta = 0$.

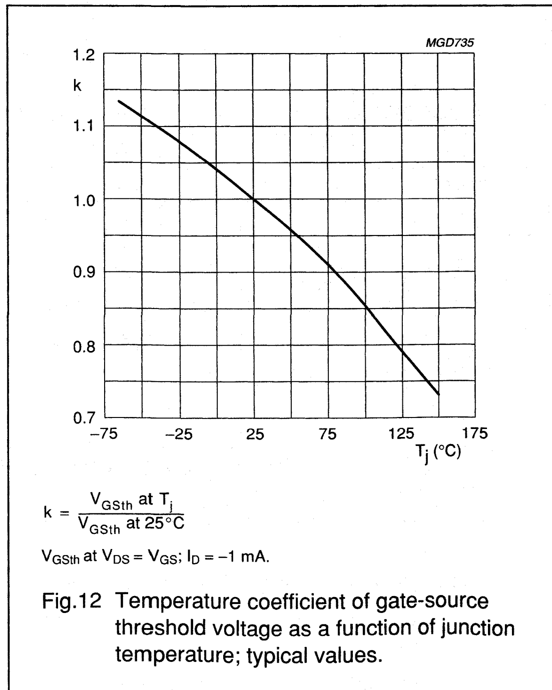
Fig.10 Source current as a function of source-drain diode forward voltage; typical values.



$T_{amb} = 25$ °C; $t_p = 80$ µs; $\delta = 0$.

$V_{DS} \geq I_D \times R_{DSon}$.

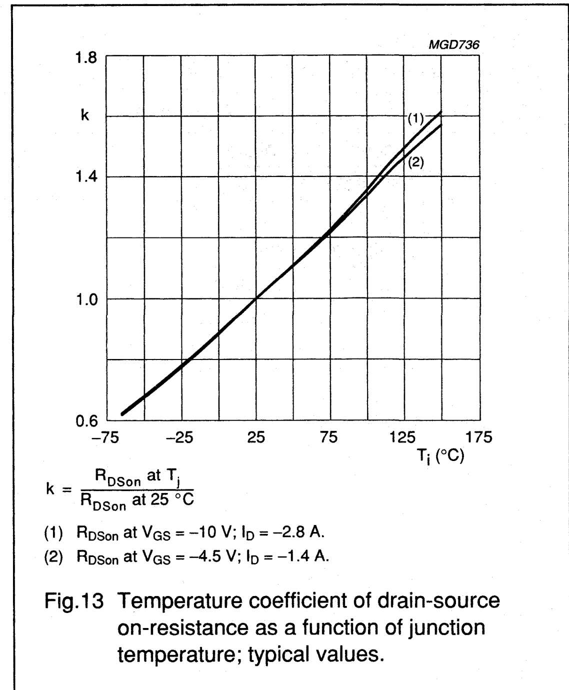
Fig.11 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25\,°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; $I_D = -1$ mA.

Fig.12 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\,°C}$$

(1) R_{DSon} at $V_{GS} = -10$ V; $I_D = -2.8$ A.

(2) R_{DSon} at $V_{GS} = -4.5$ V; $I_D = -1.4$ A.

Fig.13 Temperature coefficient of drain-source on-resistance as a function of junction temperature; typical values.

N-channel enhancement mode vertical D-MOS transistor

BSP89

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope, intended for use as a surface-mounted device in line current interrupters in telephone sets and for application in relay, high speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
Code: BSP89	
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	240	V
I_D	DC drain current	350	mA
$R_{DS(on)}$	drain-source on-resistance	6	Ω
$V_{GS(th)}$	gate-source threshold voltage	2	V

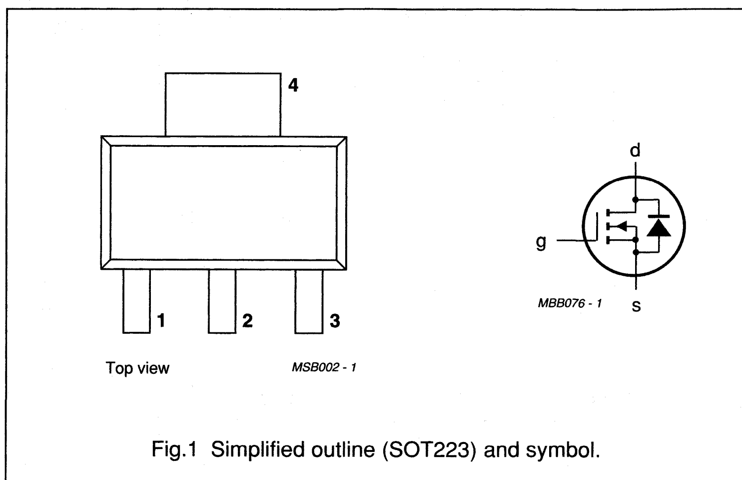


Fig.1 Simplified outline (SOT223) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	240	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	350	mA
I_{DM}	peak drain current		–	1.4	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3 K/W

Note

1. Transistor mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	240	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 60 V; V_{GS} = 0	–	–	200	nA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.8	–	2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 340 mA; V_{GS} = 10 V	–	4	6	Ω
		I_D = 340 mA; V_{GS} = 4.5 V	–	–	10	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 340 mA; V_{DS} = 25 V	140	350	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	65	140	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	5	9	pF
Switching times (see Figs 3 and 4)						
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	20	30	ns

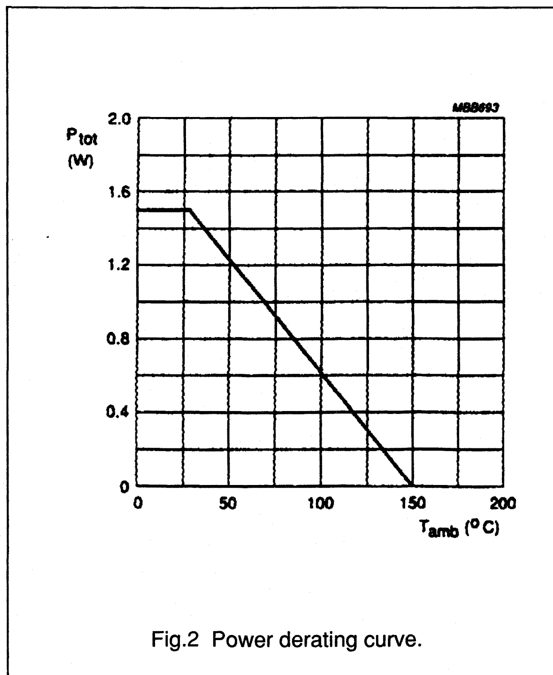


Fig.2 Power derating curve.

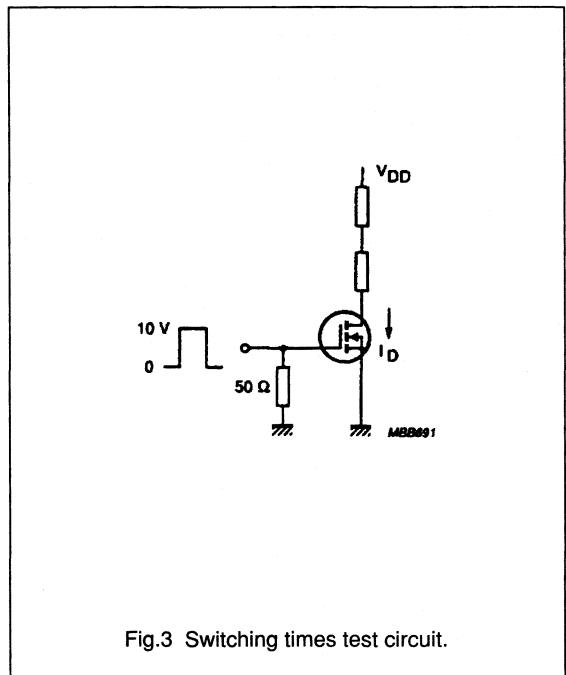


Fig.3 Switching times test circuit.

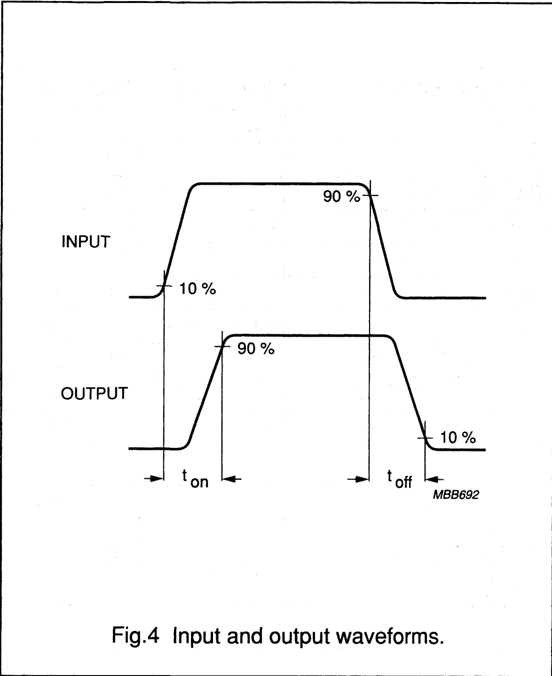


Fig.4 Input and output waveforms.

P-channel enhancement mode vertical D-MOS transistor

BSP92

FEATURES

- Low threshold voltage $V_{GS(th)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$-V_{DS}$	drain-source voltage	240	V
$-I_D$	DC drain current	180	mA
$R_{DS(on)}$	drain-source on-resistance	20	Ω
$-V_{GS(th)}$	gate-source threshold voltage	1.8	V

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope, intended for use as a surface-mounted device in line current interruptor in telephone sets and for application in relay, high speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

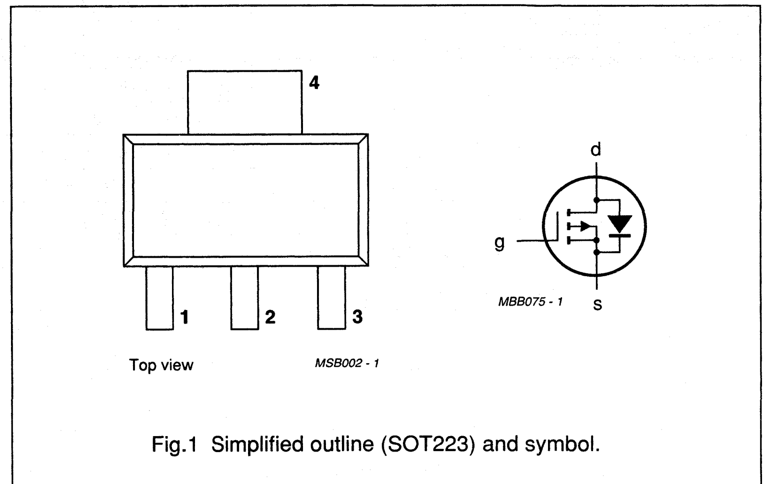


Fig.1 Simplified outline (SOT223) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	240	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$-I_D$	DC drain current		–	180	mA
$-I_{DM}$	peak drain current		–	720	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3 K/W

Note

1. Transistor mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-I_D$ = 10 µA; V_{GS} = 0	240	–	–	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 200 V; V_{GS} = 0	–	–	1	µA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA; V_{GS} = V_{DS}	0.8	–	2	V
$-V_{GS}$	gate-source voltage	$-I_D$ = 50 mA; $-V_{DS}$ = 5 V	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 180 mA; $-V_{GS}$ = 10 V	–	10	20	Ω
		$-I_D$ = 100 mA; $-V_{GS}$ = 5 V	–	–	18	Ω
		$-I_D$ = 25 mA; $-V_{GS}$ = 2.8 V	–	–	20	Ω
$\|Y_{fs}\|$	transfer admittance	$-I_D$ = 180 mA; $-V_{DS}$ = 25 V	100	200	–	mS
C_{iss}	input capacitance	$-V_{DS}$ = 25 V; V_{GS} = 0; f = 1 MHz	–	65	90	pF
C_{oss}	output capacitance	$-V_{DS}$ = 25 V; V_{GS} = 0; f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	$-V_{DS}$ = 25 V; V_{GS} = 0; f = 1 MHz	–	6	15	pF
Switching times (see Figs 3 and 4)						
t_{on}	turn-on time	$-I_D$ = 250 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	$-I_D$ = 250 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	–	20	30	ns

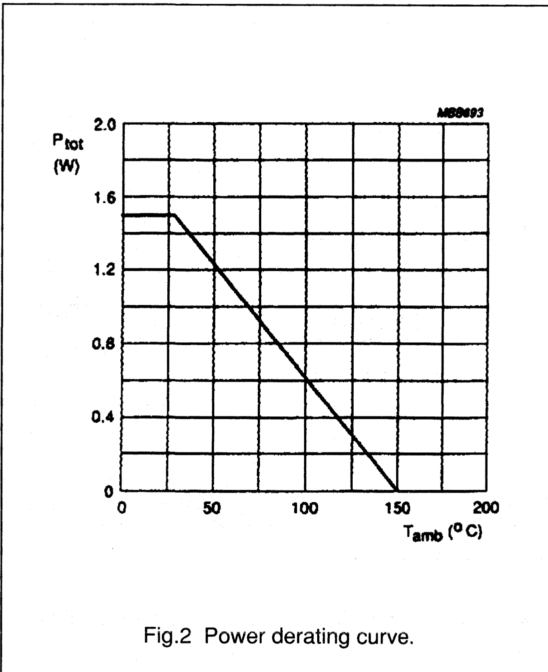
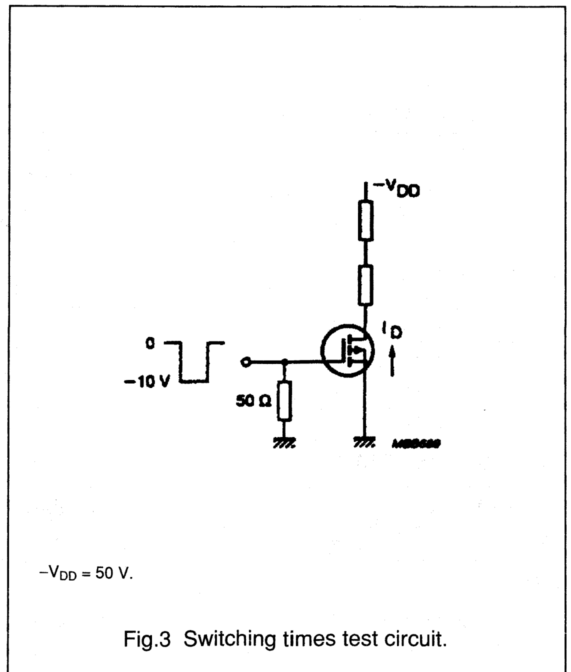


Fig.2 Power derating curve.



$-V_{DD}$ = 50 V.

Fig.3 Switching times test circuit.

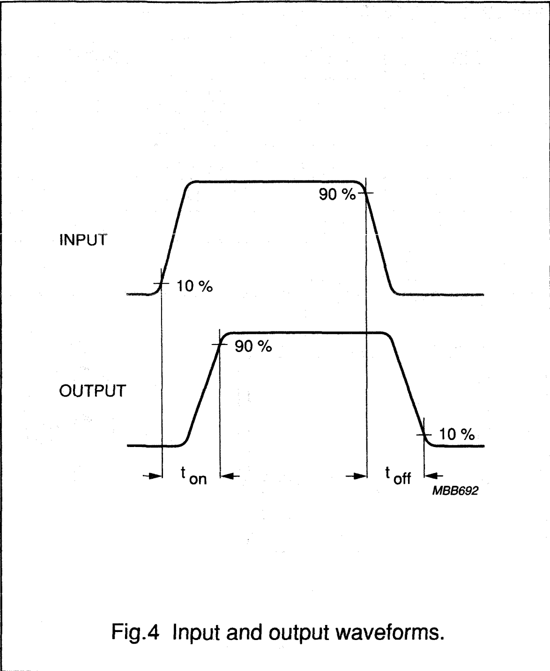


Fig.4 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BSP100

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Low-loss motor and actuator drivers
- Power switching.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a plastic SOT223 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT223

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source
4	d	drain

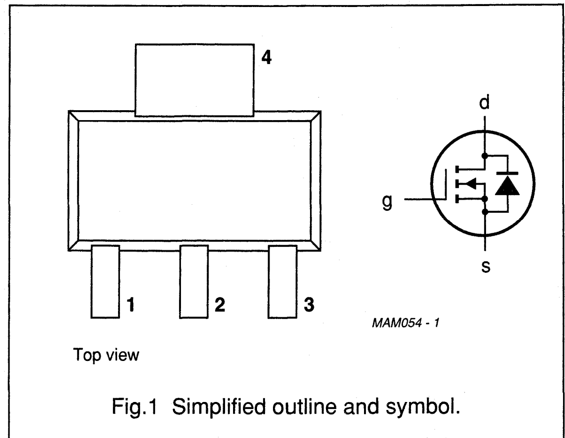


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{SD}	source-drain diode forward voltage	I_S = 1.25 A	–	1.2	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; $V_{DS} = V_{GS}$	1	2.8	V
I_D	drain current (DC)		–	3.5	A
R_{DSon}	drain-source on-state resistance	I_D = 2.2 A; V_{GS} = 10 V	–	0.1	Ω
P_{tot}	total power dissipation	T_s = 100 °C	–	5	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)	$T_s \leq 100°C$	–	3.5	A
I_{DM}	peak drain current	note 1	–	14	A
P_{tot}	total power dissipation	T_s = 100 °C	–	5	W
		T_{amb} = 25 °C; note 2	–	1.65	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C
Source-drain diode					
I_S	source current (DC)	$T_s \leq 100°C$	–	2	A
I_{SM}	peak pulsed source current	note 1	–	7	A

Notes

1. Pulse width and duty cycle limited by maximum junction temperature.
2. Device mounted on an epoxy printed-circuit board, 40 × 40 × 1.5 mm; mounting pad for drain lead minimum 6 cm^2.

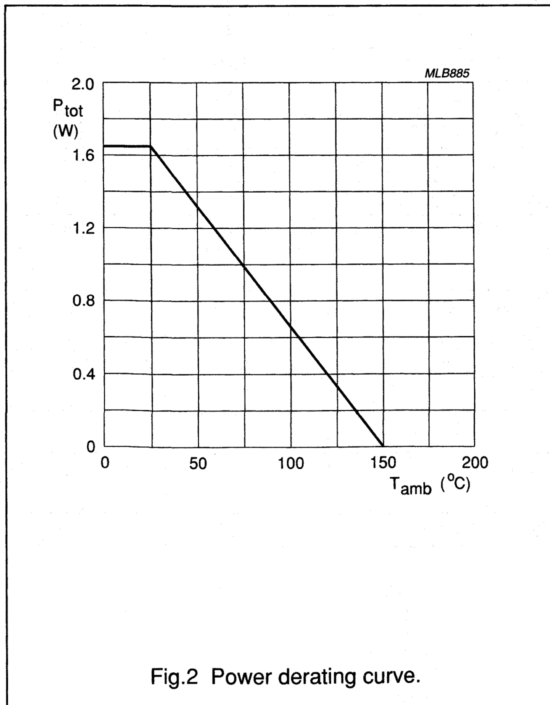
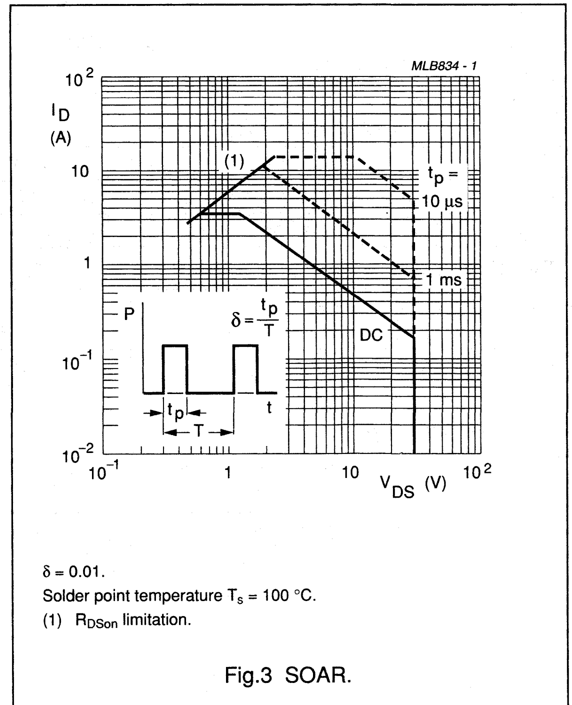


Fig.2 Power derating curve.



δ = 0.01.
Solder point temperature T_s = 100 °C.
(1) R_{DSon} limitation.

Fig.3 SOAR.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	75	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point		10	K/W

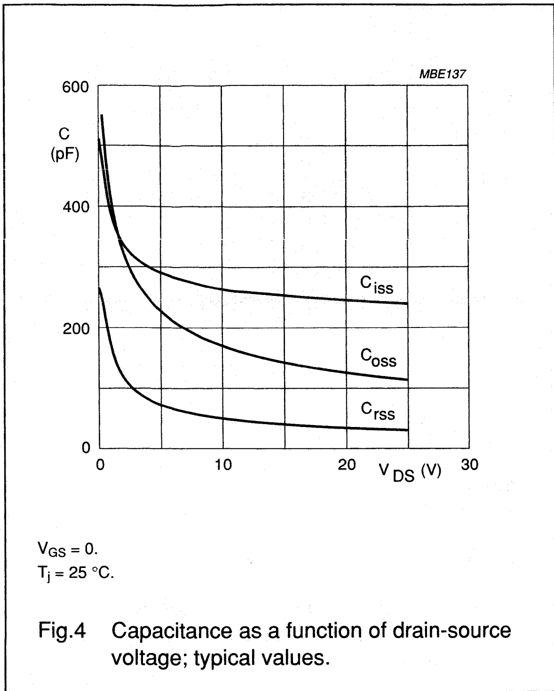
Note

1. Device mounted on an epoxy printed-circuit board, 40 × 40 × 1.5 mm; mounting pad for drain lead minimum 6 cm^2.

CHARACTERISTICS

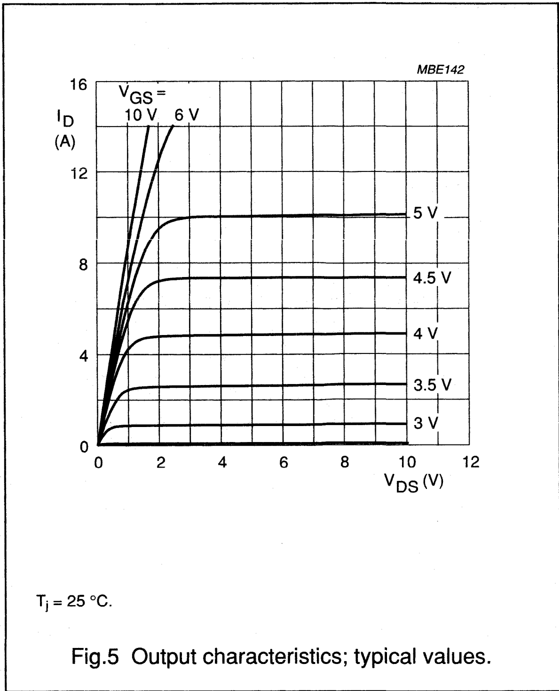
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
I_{Don}	on-state drain current	V_{GS} = 10 V; V_{DS} = 1 V	3.5	–	–	A
		V_{GS} = 4.5 V; V_{DS} = 5 V	2	–	–	A
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 1 A	–	0.11	0.2	Ω
		V_{GS} = 10 V; I_D = 2.2 A	–	0.08	0.1	Ω
$\|y_{fs}\|$	forward transfer admittance	V_{DS} = 20 V; I_D = 2.2 A	2	4.5	–	S
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	250	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	140	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	50	–	pF
Q_G	total gate charge	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	10	30	nC
Q_{GS}	gate-source charge	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	1	–	nC
Q_{GD}	gate-drain charge	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	2.5	–	nC
Switching times						
t_{on}	turn-on time	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 1 A; R_L = 20 Ω	–	15	40	ns
t_{off}	turn-off time	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_L = 20 Ω	–	25	75	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 1.25 A	–	–	1.2	V
t_{rr}	reverse recovery time	I_S = 1.25 A; di/dt = 100 A/μs	–	35	100	ns



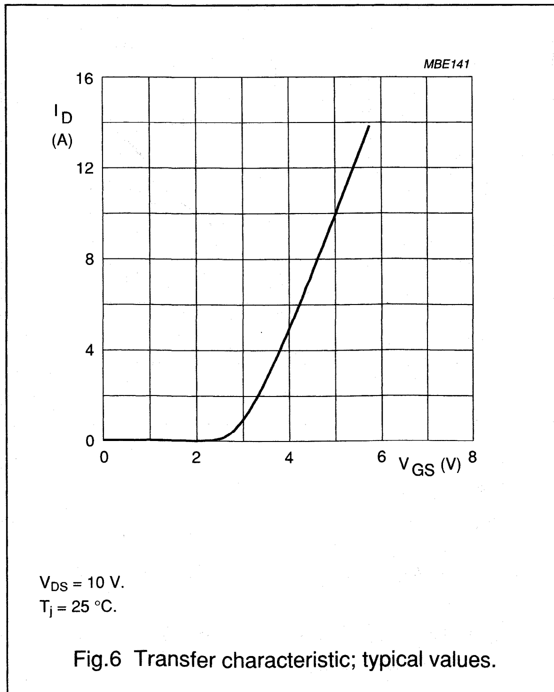
V_{GS} = 0.
T_j = 25 °C.

Fig.4 Capacitance as a function of drain-source voltage; typical values.



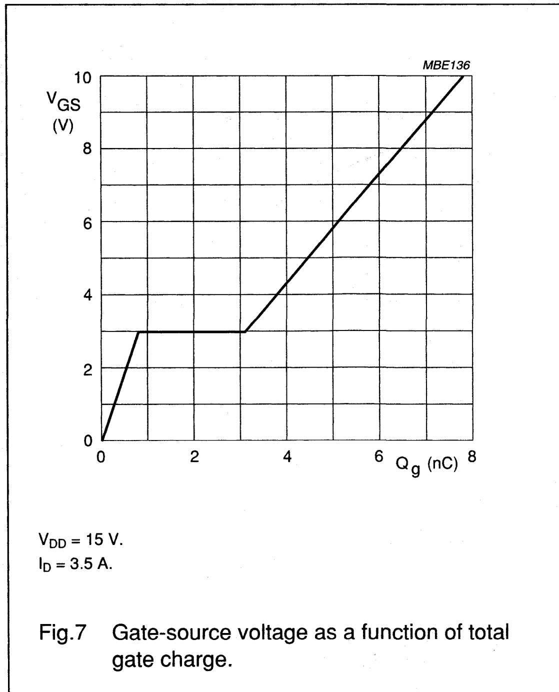
T_j = 25 °C.

Fig.5 Output characteristics; typical values.



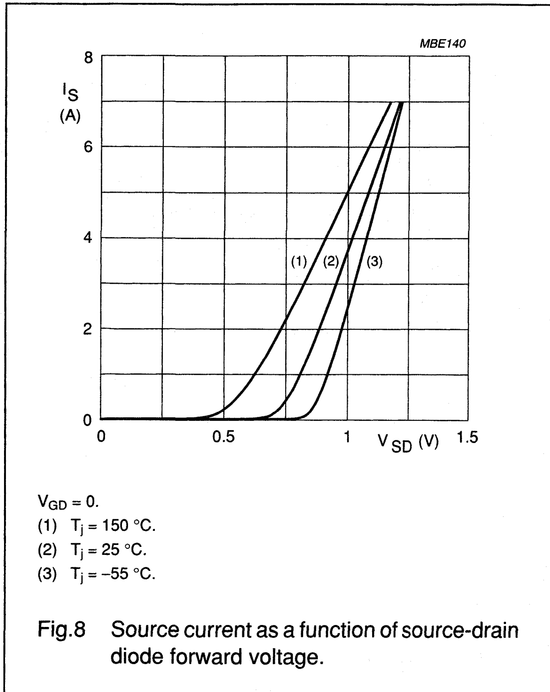
V_{DS} = 10 V.
T_j = 25 °C.

Fig.6 Transfer characteristic; typical values.



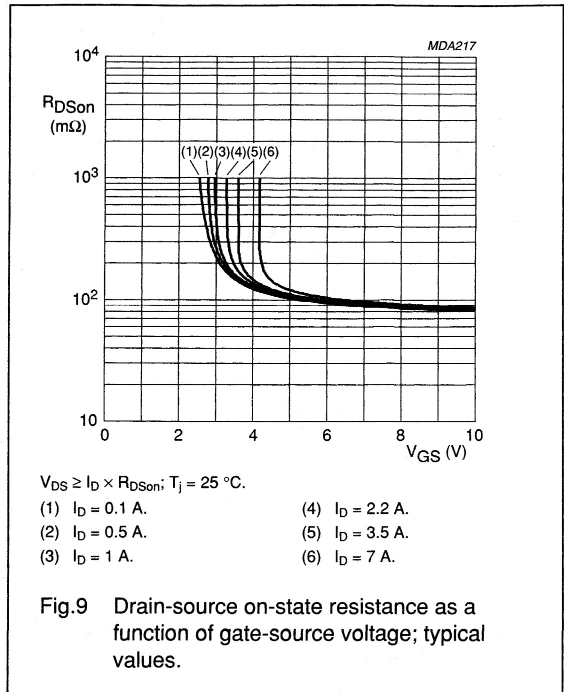
V_{DD} = 15 V.
I_D = 3.5 A.

Fig.7 Gate-source voltage as a function of total gate charge.



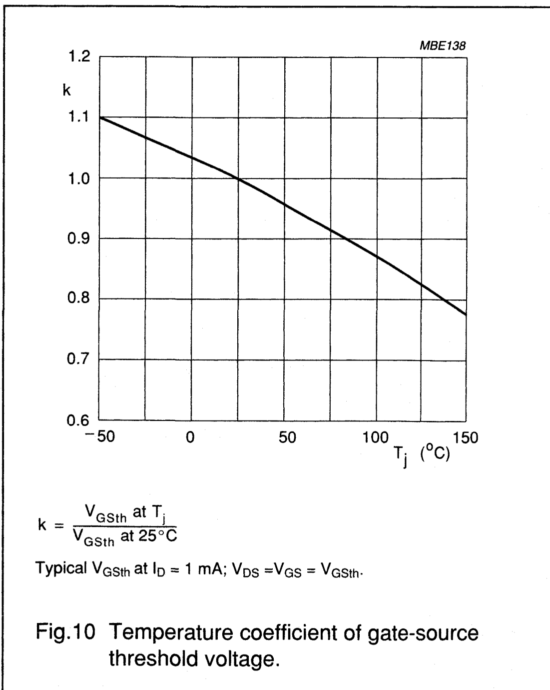
$V_{GD} = 0$.
(1) $T_j = 150$ °C.
(2) $T_j = 25$ °C.
(3) $T_j = -55$ °C.

Fig.8 Source current as a function of source-drain diode forward voltage.



$V_{DS} \geq I_D \times R_{DSon}$; $T_j = 25$ °C.
(1) $I_D = 0.1$ A.
(2) $I_D = 0.5$ A.
(3) $I_D = 1$ A.
(4) $I_D = 2.2$ A.
(5) $I_D = 3.5$ A.
(6) $I_D = 7$ A.

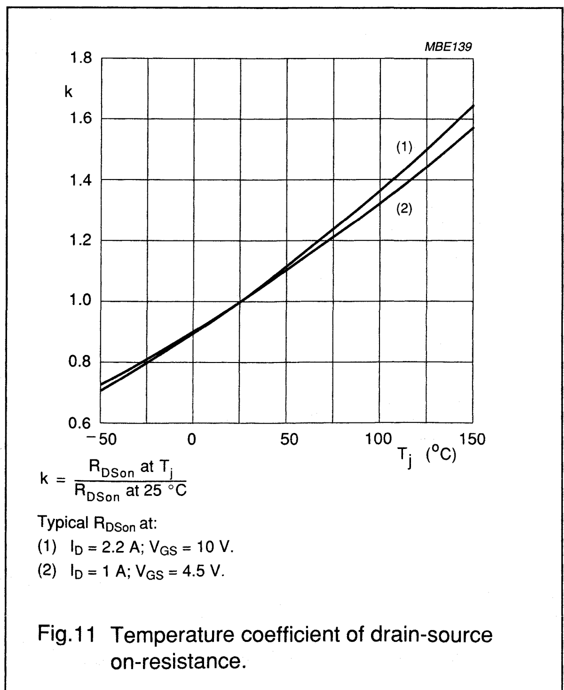
Fig.9 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25 °C}$$

Typical V_{GSth} at $I_D = 1$ mA; $V_{DS} = V_{GS} = V_{GSth}$.

Fig.10 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25 °C}$$

Typical R_{DSon} at:
(1) $I_D = 2.2$ A; $V_{GS} = 10$ V.
(2) $I_D = 1$ A; $V_{GS} = 4.5$ V.

Fig.11 Temperature coefficient of drain-source on-resistance.

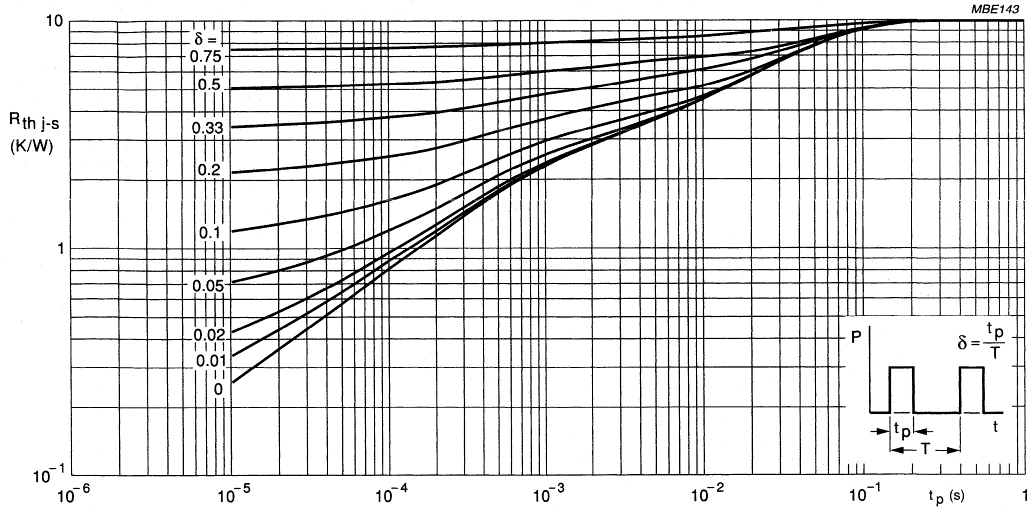


Fig.12 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

N-channel enhancement mode vertical D-MOS transistor

BSP106

FEATURES

- Very low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage	–	60	V
I_D	drain current	DC value	425	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 200 mA V_{GS} = 10 V	4	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA $V_{GS} = V_{DS}$	3	V

PIN CONFIGURATION

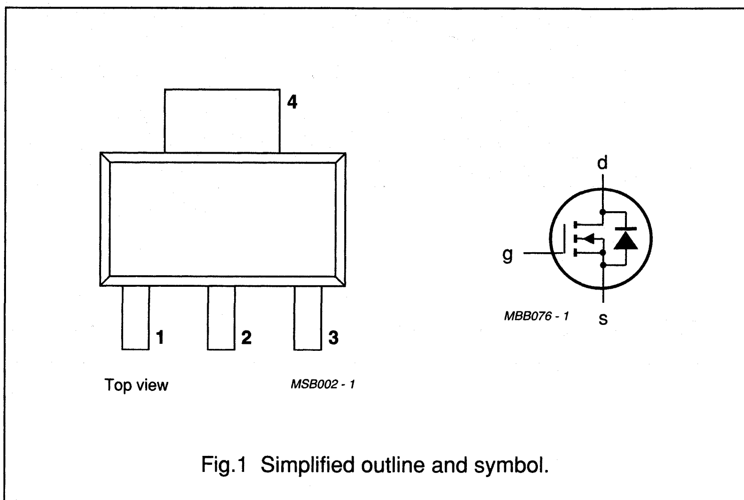


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	60	V
V_{DG}	drain-gate voltage		–	60	V
$\pm V_{GSO}$	gate-source voltage		–	20	V
I_D	drain current	DC value	–	425	mA
I_{DM}	drain current	peak value	–	850	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–55	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board 40 x 40 x 1.5 mm; mounting pad for the drain lead minimum 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	60	90	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 48 V V_{GS} = 0	–	–	1	μA
		V_{DS} = 25 V V_{GS} = 0	–	–	0.5	μA
$\pm I_{GSS}$	gate-source leakage current	V_{DS} = 0 $\pm V_{GS}$ = 15 V	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	0.8	–	3	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 200 mA V_{GS} = 10 V	–	2.5	4	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 200 mA V_{DS} = 10 V	100	200	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	25	40	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	22	30	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	6	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	2	5	ns
t_{off}	turn-off time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10	–	10	15	ns

N-channel enhancement mode vertical D-MOS transistor

BSP106

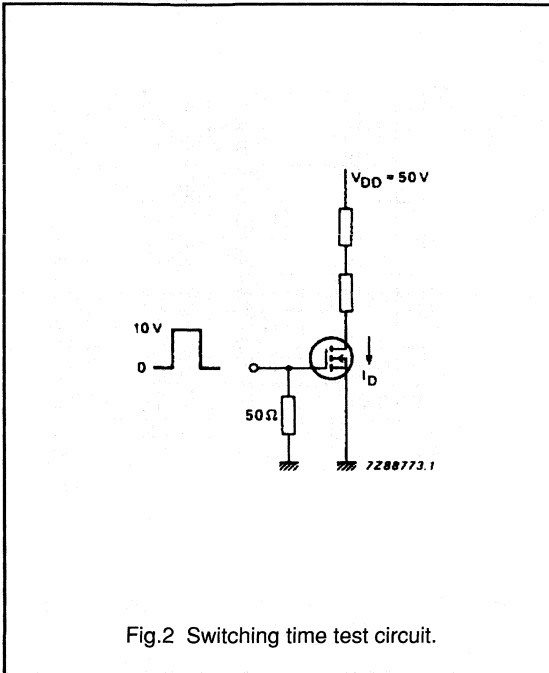


Fig.2 Switching time test circuit.

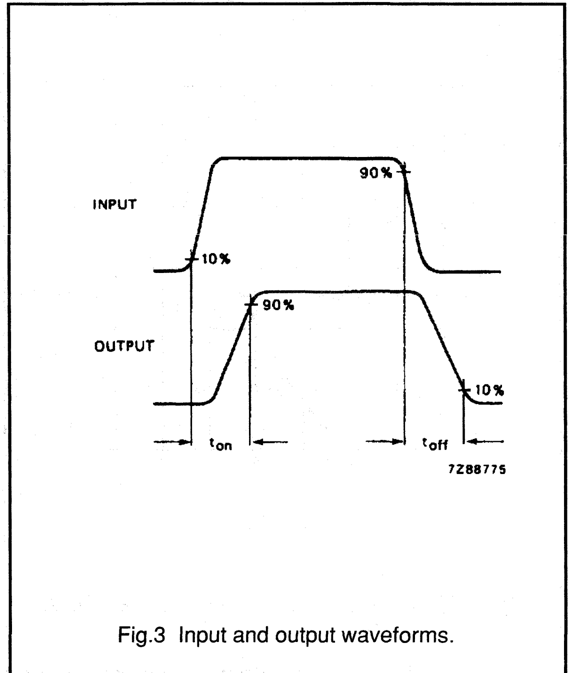


Fig.3 Input and output waveforms.

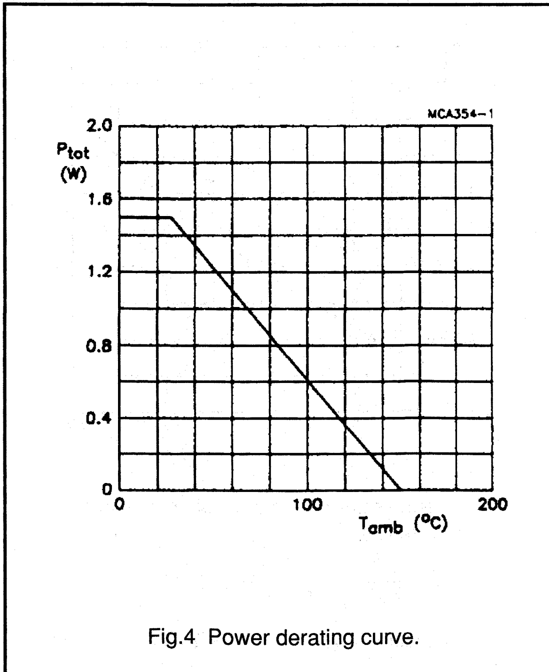


Fig.4 Power derating curve.

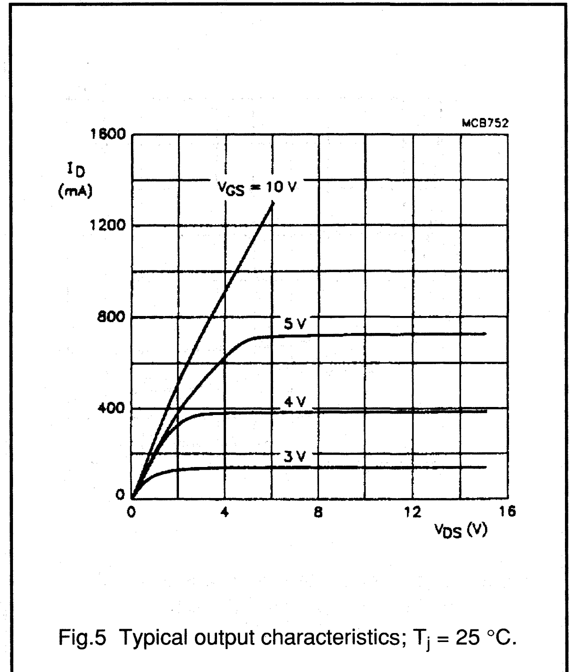


Fig.5 Typical output characteristics; T_j = 25 °C.

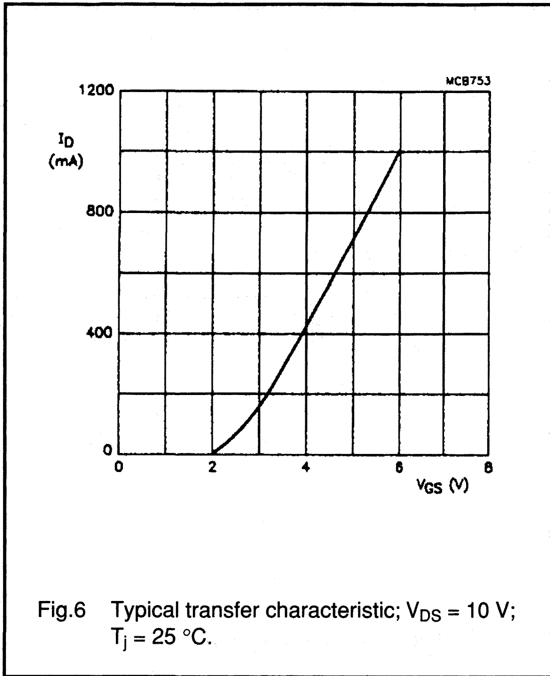


Fig.6 Typical transfer characteristic; V_{DS} = 10 V; T_j = 25 °C.

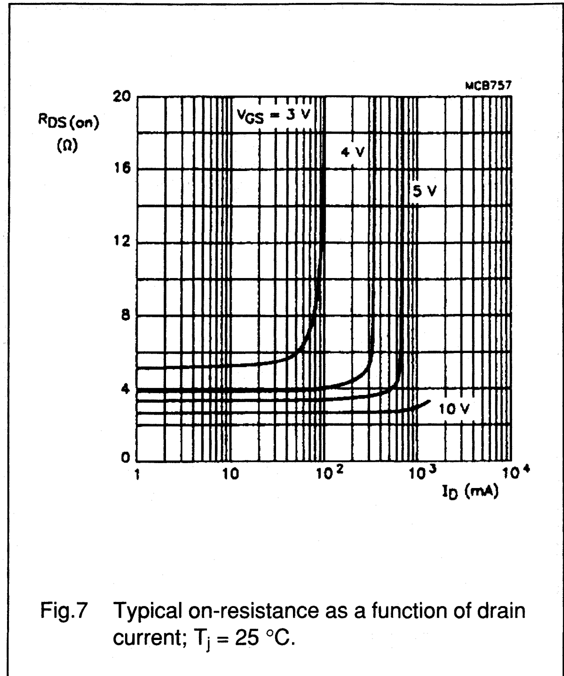


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

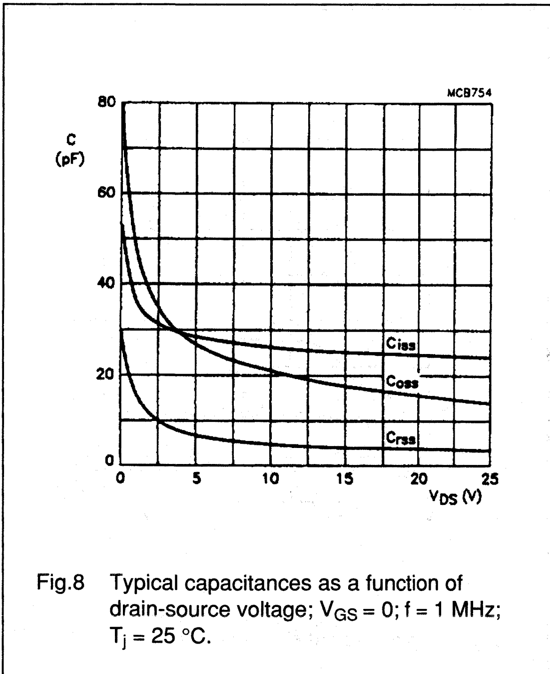


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

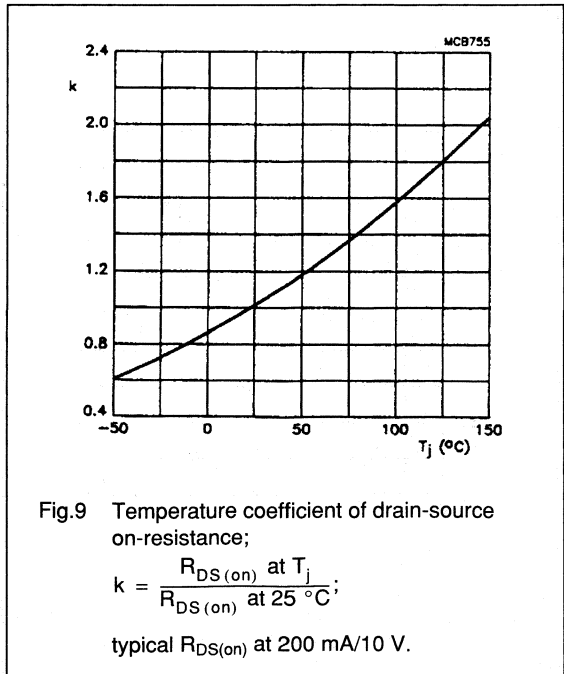


Fig.9 Temperature coefficient of drain-source on-resistance;

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C};$$

typical $R_{DS(on)}$ at 200 mA/10 V.

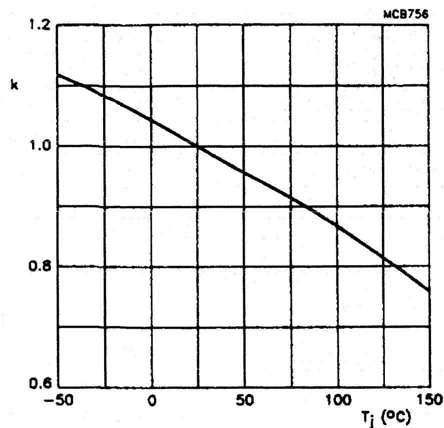


Fig.10 Temperature coefficient of gate-source threshold voltage;

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C};$$

$V_{GS(th)}$ at 1 mA.

N-channel enhancement mode vertical D-MOS transistor

BSP107

FEATURES

- Direct interface to C-MOS, TTL, etc. due to low threshold voltage
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope. Intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer driver switching.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage (DC)	200	V
$V_{GS(th)}$	gate-source threshold voltage	2.4	V
I_D	drain current (DC)	200	mA
$R_{DS(on)}$	drain-source on-state resistance	28	Ω

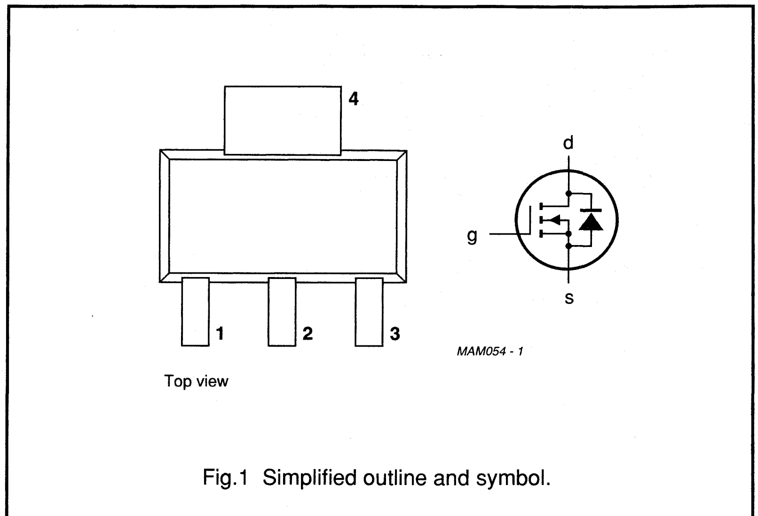


Fig.1 Simplified outline and symbol.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	drain current	DC	–	200	mA
I_{DM}	drain current	peak	–	350	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	operating junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	from junction to ambient (note 1)	83.3	K/W

Note

1. Device mounted on an epoxy printed circuit board, 40 mm × 40 mm × 1.5 mm. Mounting pad for the drain lead minimum 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 I_D = 10 μA	200	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 130 V V_{GS} = 0	–	–	30	nA
I_{DSX}	drain-source leakage current	V_{DS} = 70 V V_{GS} = 0.2 V	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	± V_{GS} = 15 V V_{DS} = 0	–	–	10	nA
$V_{GS(th)}$	gate threshold voltage	I_D =1 mA V_{DS} = V_{GS}	0.8	–	2.4	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA V_{GS} = 2.6 V	–	20	28	Ω
$R_{DS(on)}$	drain-source on-resistance	I_D = 150 mA V_{GS} = 10 V	–	14	–	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA V_{DS} = 15 V	90	180	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	50	65	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	16	25	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	4	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	switching-on time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 – 10 V	–	2	10	ns
t_{off}	switching-off time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 – 10 V	–	5	20	ns

N-channel enhancement mode vertical D-MOS transistor

BSP107

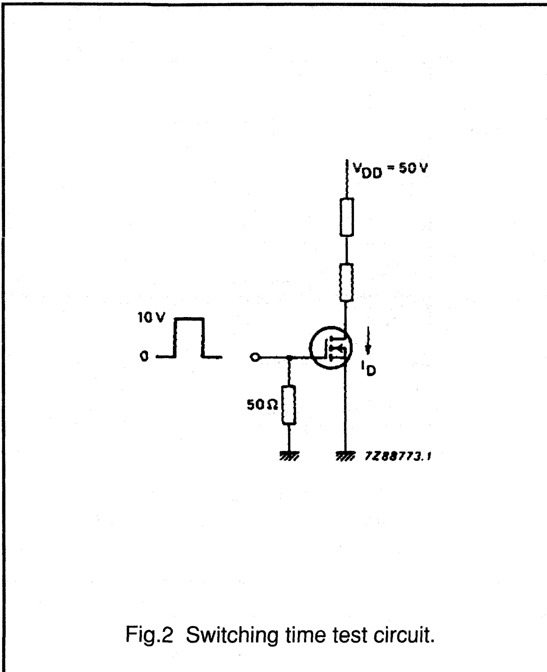


Fig.2 Switching time test circuit.

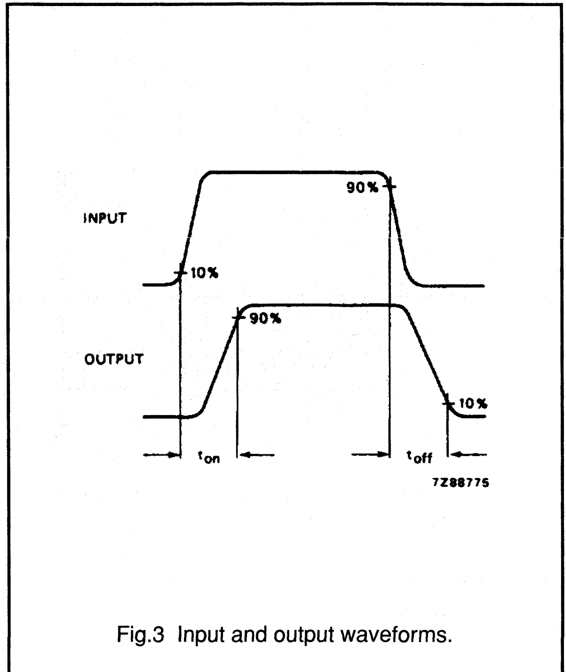


Fig.3 Input and output waveforms.

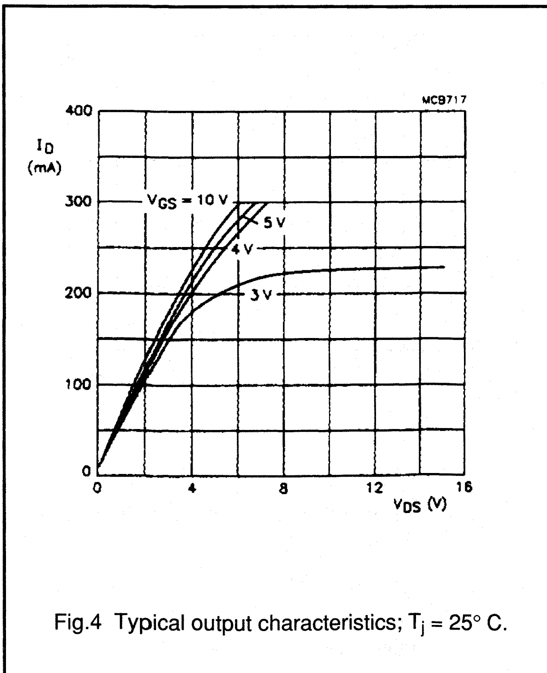


Fig.4 Typical output characteristics; T_j = 25° C.

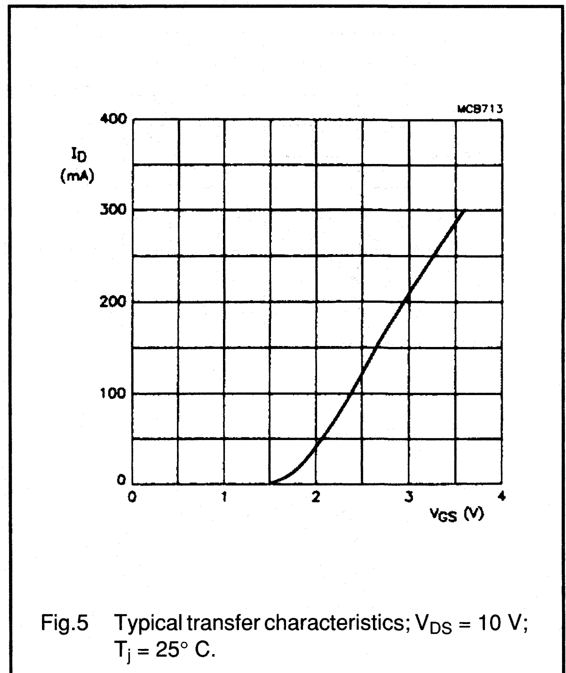


Fig.5 Typical transfer characteristics; V_{DS} = 10 V; T_j = 25° C.

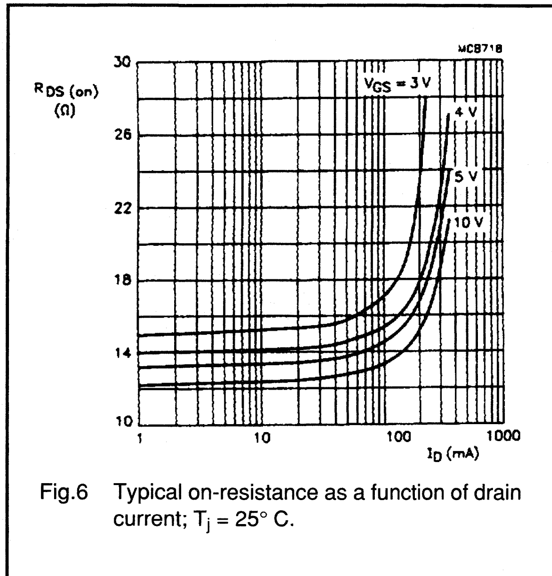


Fig.6 Typical on-resistance as a function of drain current; T_j = 25° C.

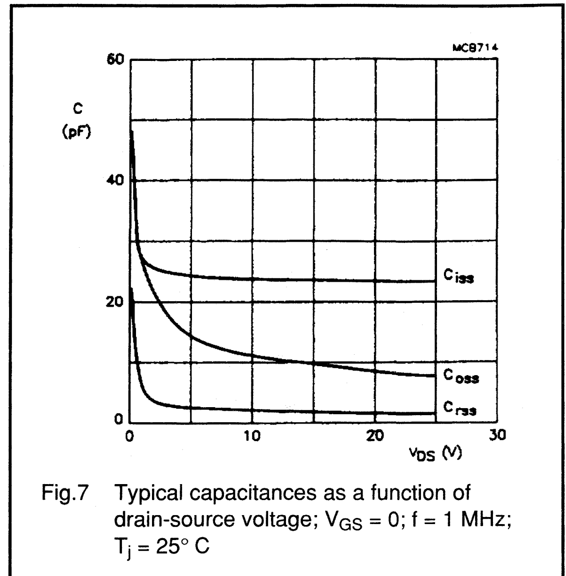
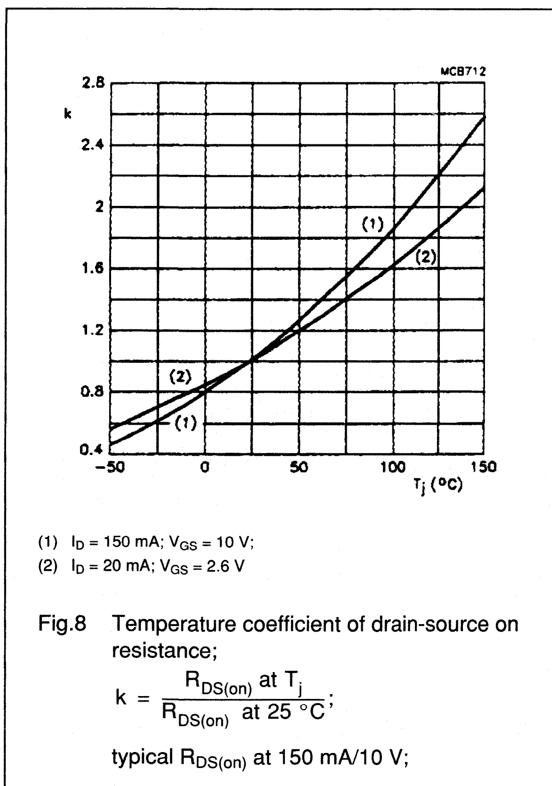


Fig.7 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25° C



(1) I_D = 150 mA; V_{GS} = 10 V;
(2) I_D = 20 mA; V_{GS} = 2.6 V

Fig.8 Temperature coefficient of drain-source on resistance;

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ ^\circ C};$$

typical $R_{DS(on)}$ at 150 mA/10 V;

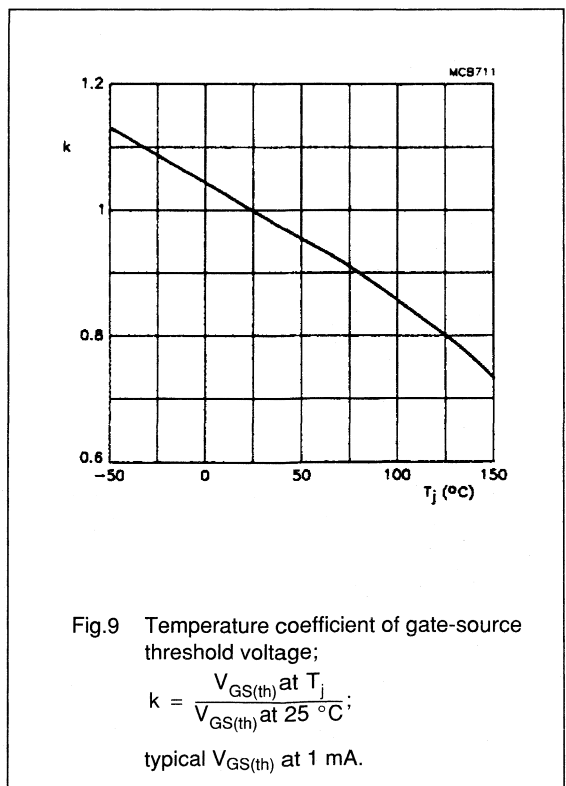


Fig.9 Temperature coefficient of gate-source threshold voltage;

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ ^\circ C};$$

typical $V_{GS(th)}$ at 1 mA.

N-channel enhancement mode vertical D-MOS transistor

BSP107

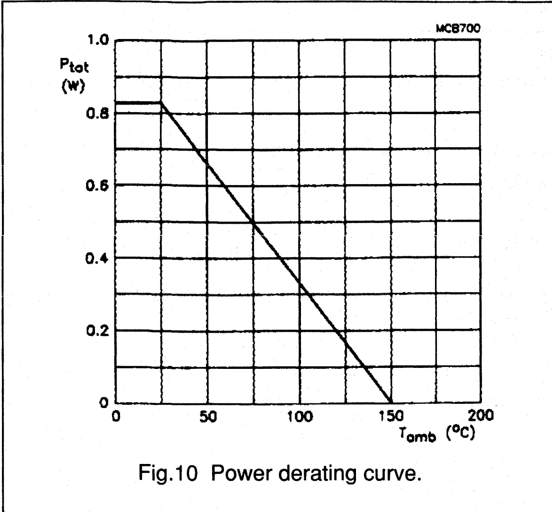


Fig.10 Power derating curve.

N-channel enhancement mode vertical D-MOS transistor

BSP108

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line-transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

PINNING - SOT223

1	= gate
2	= drain
3	= source
4	= drain

Marking code

BSP108

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	500	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1.5	W
Drain-source ON-resistance				
		typ.	2.0	Ω
I_D = 500 mA; V_{GS} = 10 V	$R_{DS(on)}$	max.	3.0	Ω
Transfer admittance				
I_D = 500 mA; V_{DS} = 15 V	$\lvert Y_{fs} \rvert$	min.	150	mS
		typ.	300	mS

PIN CONFIGURATION

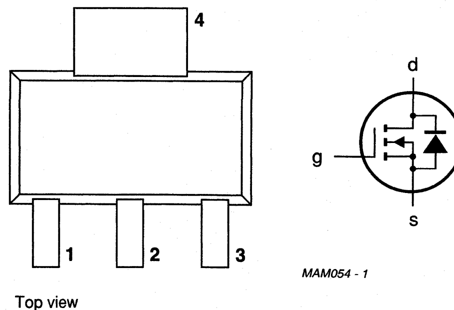


Fig.1 Simplified outline and symbol.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	500	mA
Drain current (peak)	I_{DM}	max.	1.0	A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}	−65 to + 150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board 40 mm × 40 mm × 1.5 mm; mounting pad for the collector lead min. 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)\ DSS}$	min.	80	V
Gate threshold voltage I_D = 1 mA; V_{GS} = V_{DS}	$V_{GS\ (th)}$	min.	1.5	V
		max.	3.5	V
Gate-source leakage current $\pm V_{GS}$ = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1.0	μA
Drain-source ON-resistance I_D = 500 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	2.0	Ω
		max.	3.0	Ω
Transfer admittance I_D = 500 mA; V_{DS} = 15 V	$\lvert Y_{fs} \rvert$	min.	150	mS
		typ.	300	mS
Input capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ.	45	pF
		max.	60	pF
Output capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ.	30	pF
		max.	45	pF

Feedback capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ.	8	pF
		max.	12	pF
Switching times (see Figs 2 and 3) I_D = 500 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	4	ns
		max.	8	ns
	t_{off}	typ.	10	ns
		max.	15	ns

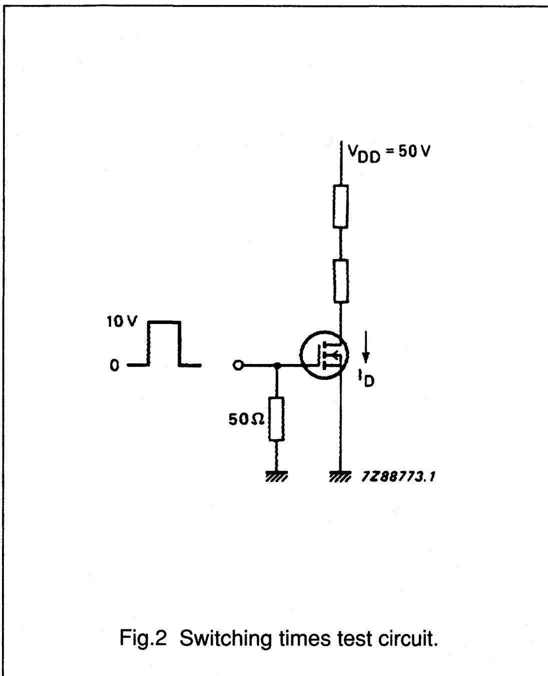


Fig.2 Switching times test circuit.

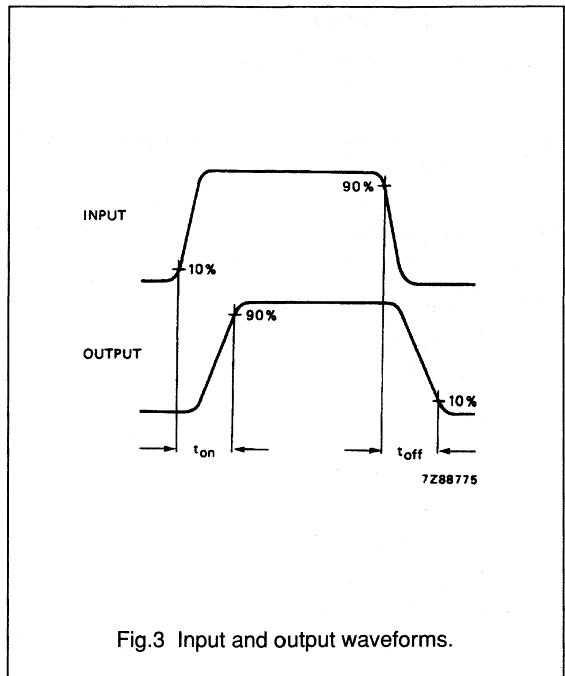


Fig.3 Input and output waveforms.

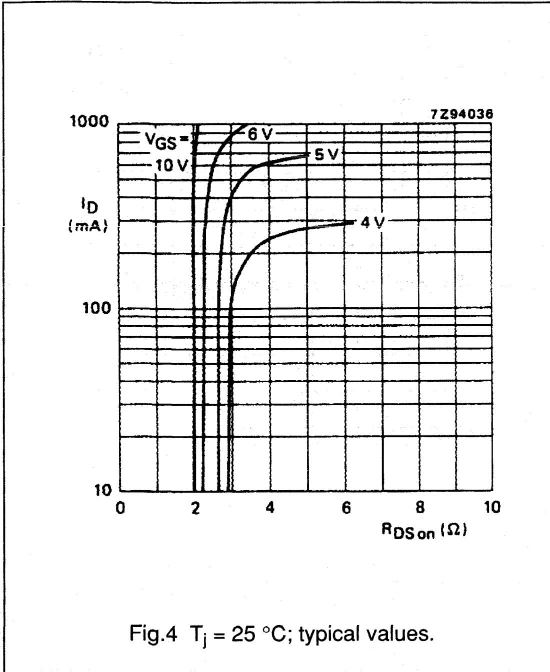


Fig.4 T_j = 25 °C; typical values.

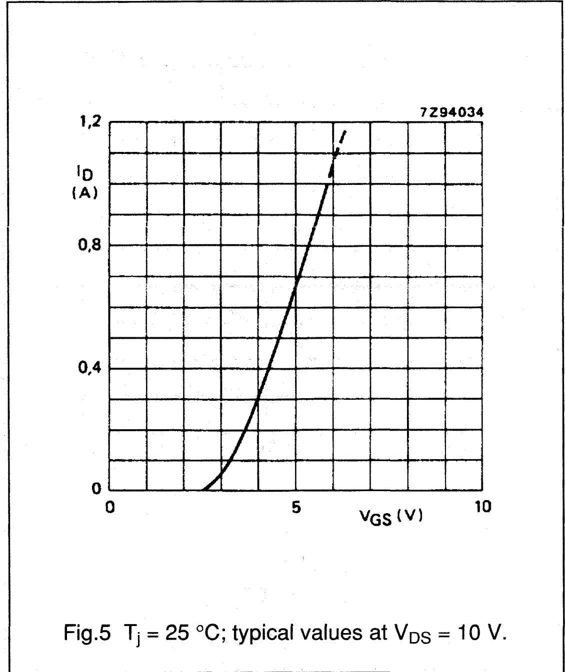


Fig.5 T_j = 25 °C; typical values at V_{DS} = 10 V.

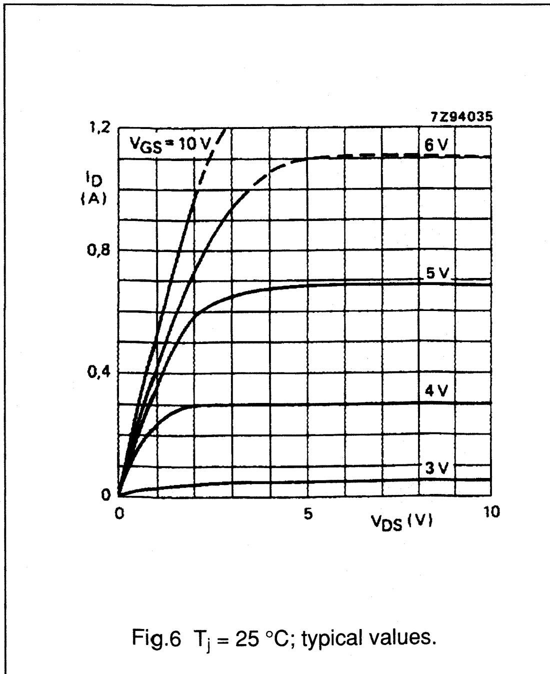


Fig.6 T_j = 25 °C; typical values.

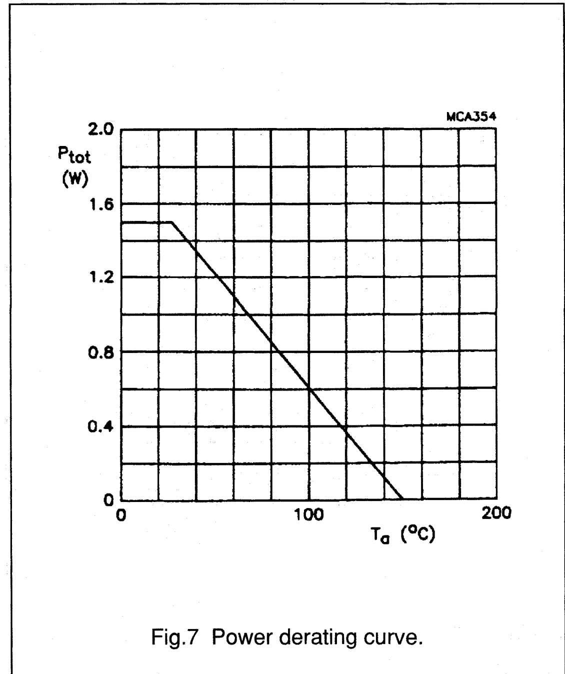


Fig.7 Power derating curve.

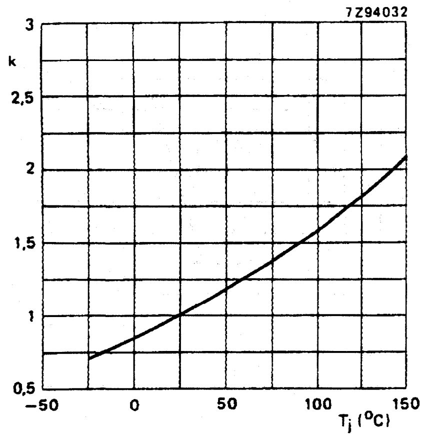


Fig.8

$$k = \frac{R_{DS\,on}\ \text{at}\ T_j}{R_{DS\,on}\ \text{at}\ 25\ °C};$$

typical values at 500 mA/10 V.

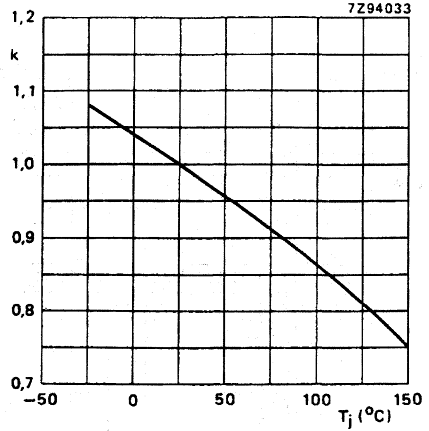


Fig.9

$$k = \frac{V_{GS\,(th)}\ \text{at}\ T_j}{V_{GS\,(th)}\ \text{at}\ 25\ °C};$$

$V_{GS(th)}$ at 1 mA; typical values.

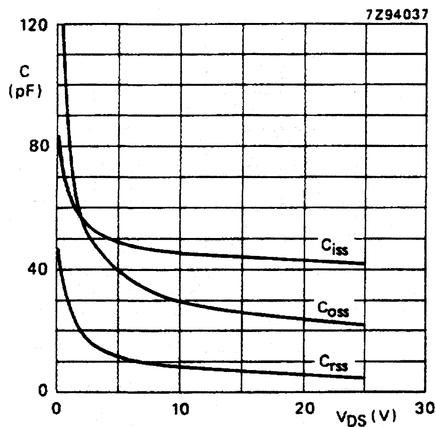


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-channel enhancement mode vertical D-MOS transistor

BSP110

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and designed for use in telephone ringer circuits and for application in relay, high-speed and line transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

PINNING - SOT223

1 = gate
2 = drain
3 = source
4 = drain

MARKING CODE

BSP110

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80	V
Drain source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	325	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1.5	W
Drain-source ON-resistance I_D = 200 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	4.5	Ω
		max.	7	Ω
Transfer admittance I_D = 200 mA; V_{DS} = 15 V	$\lvert Y_{fs} \rvert$	min.	75	mS
		typ.	150	mS

PIN CONFIGURATION

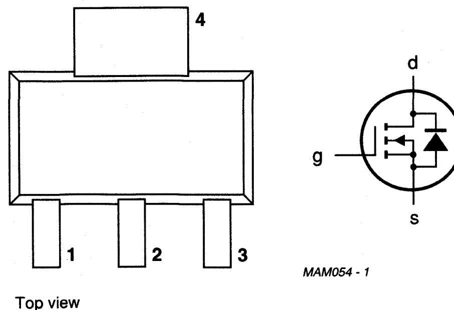


Fig.1 Simplfied outline and symbol.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Parameter	Symbol		Value	Unit
Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	325	mA
Drain current (peak)	I_{DM}	max.	650	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

Parameter	Symbol		Value	Unit
From junction to ambient (note 1)	$R_{th\ j-a}$	=	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board 40 mm × 40 mm × 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value	Unit
Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)\ DSS}$	min.	80	V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1.0	μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$I_{GS(th)}$	min.	0.8	V
		max.	2.8	V
Drain-source ON-resistance (see Fig.4) I_D = 150 mA; V_{GS} = 5 V	$R_{DS(on)}$	typ.	7	Ω
		max.	10	Ω
I_D = 200 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	4.5	Ω
		max.	7	Ω
Transfer admittance I_D = 200 mA; V_{DS} = 5 V	$\lvert Y_{fs} \rvert$	min.	75	mS
		typ.	150	mS
Input capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ.	15	pF
		max.	30	pF

Output capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ.	13	pF
		max.	20	pF
Feedback capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ.	3	pF
		max.	6	pF
Switching times (see Figs 2 and 3) I_D = 200 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	2	ns
		max.	5	ns
	t_{off}	typ.	5	ns
		max.	10	ns

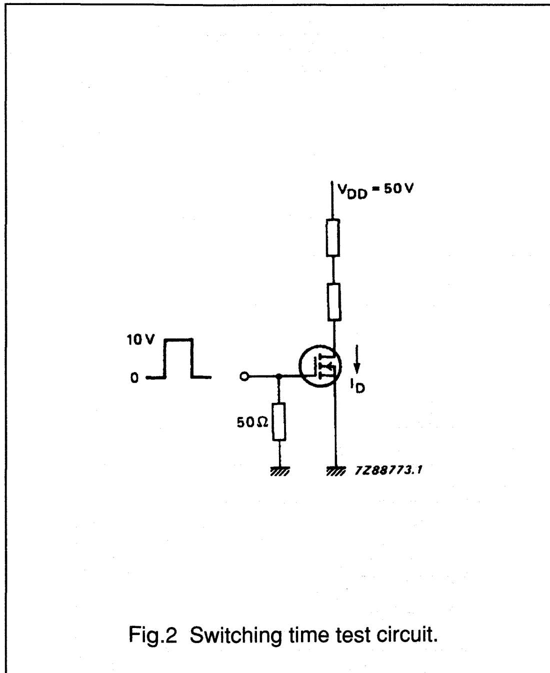


Fig.2 Switching time test circuit.

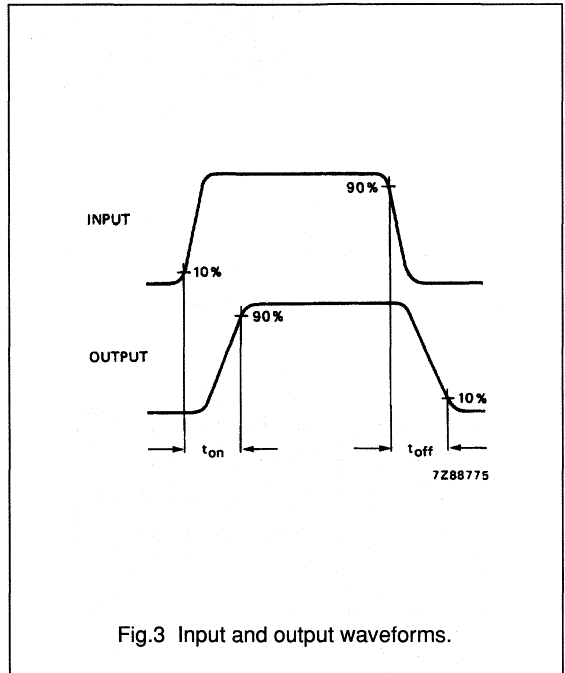


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BSP110

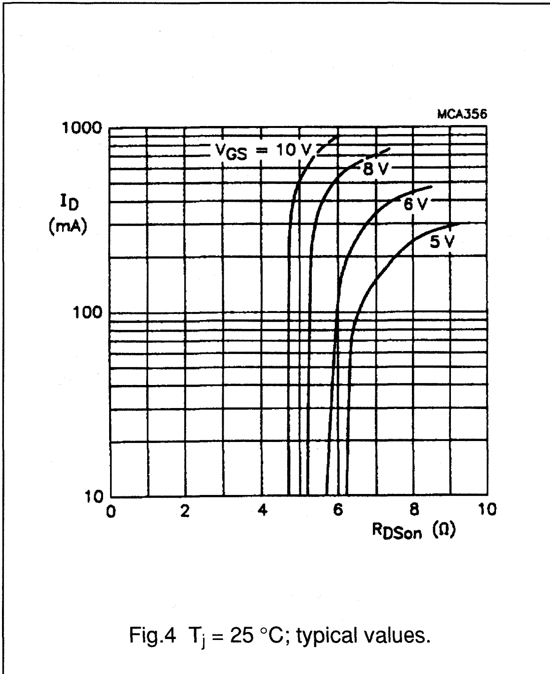


Fig.4 T_j = 25 °C; typical values.

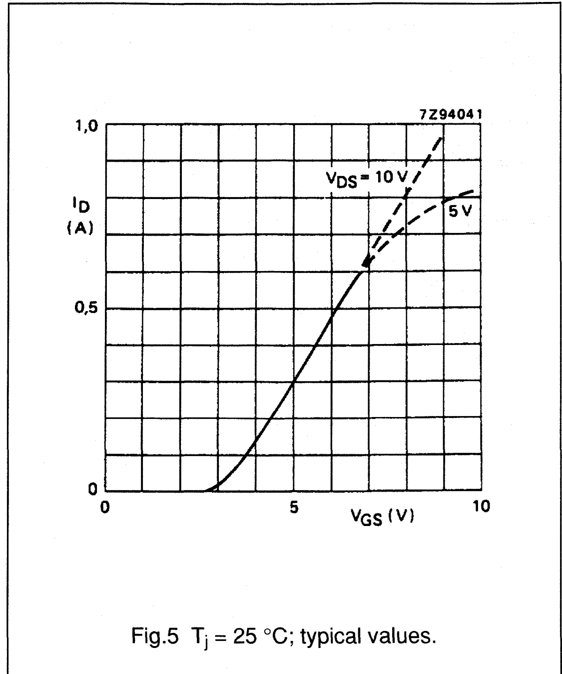


Fig.5 T_j = 25 °C; typical values.

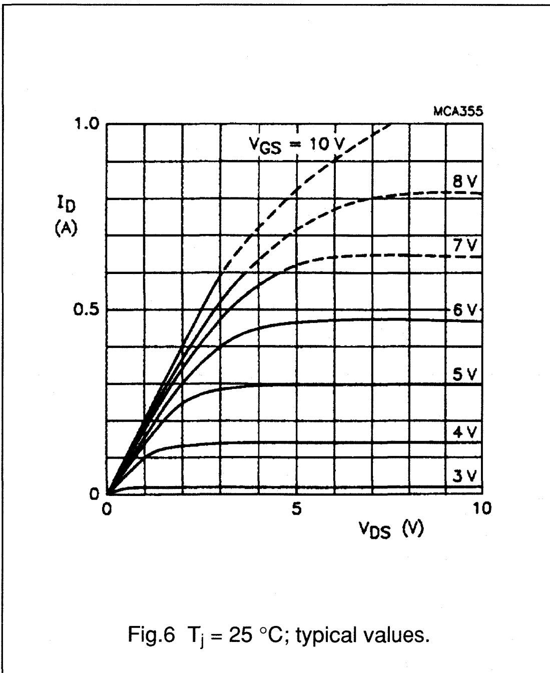


Fig.6 T_j = 25 °C; typical values.

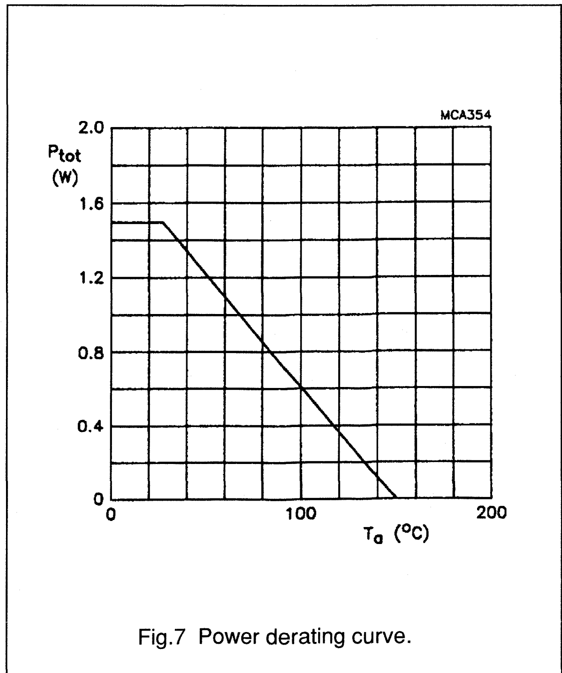


Fig.7 Power derating curve.

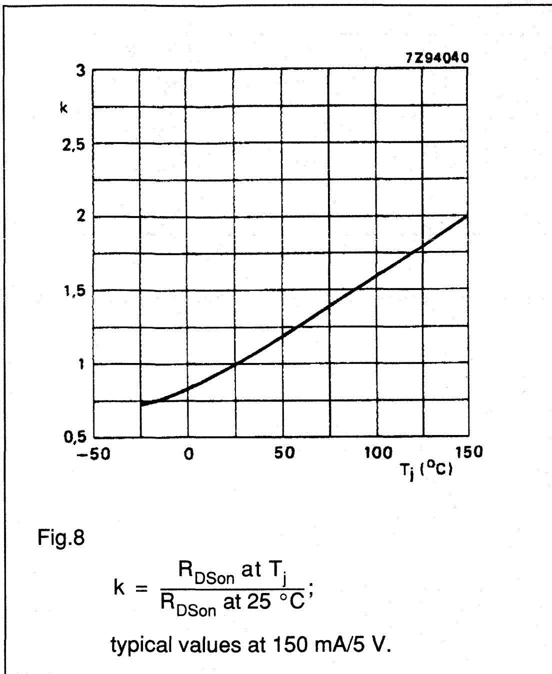


Fig.8

$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C};$$

typical values at 150 mA/5 V.

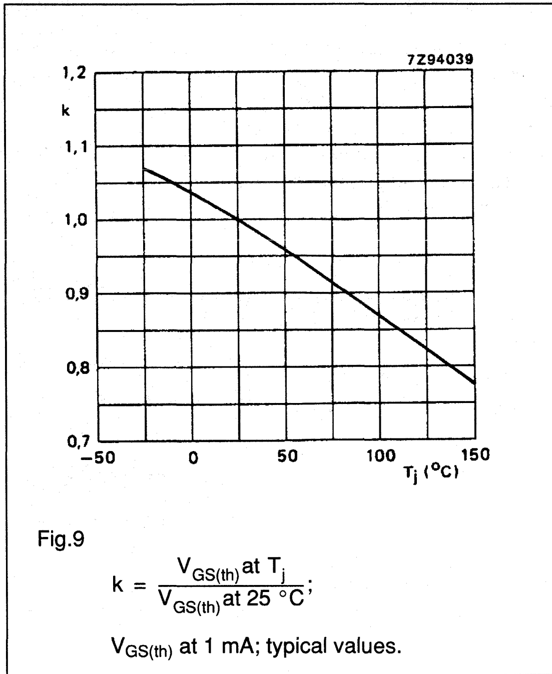


Fig.9

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C};$$

$V_{GS(th)}$ at 1 mA; typical values.

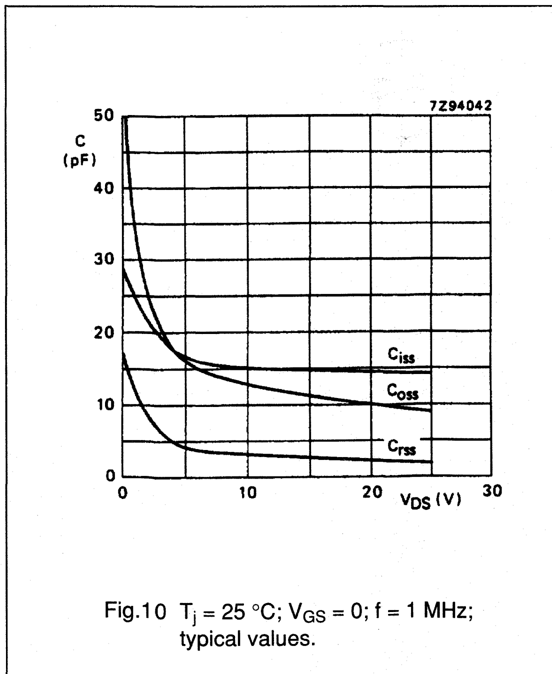


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-channel enhancement mode vertical D-MOS transistor

BSP120

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and designed for use as a line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200	V
Drain-current (DC)	I_D	max.	250	mA
Drain-source ON-resistance				
I_D = 250 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	7	Ω
		max.	12	Ω
Gate threshold voltage	$V_{GS(th)}$	max.	2.8	V

PINNING - SOT223

1 = gate
2 = drain
3 = source
4 = drain

Marking code

BSP120

PIN CONFIGURATION

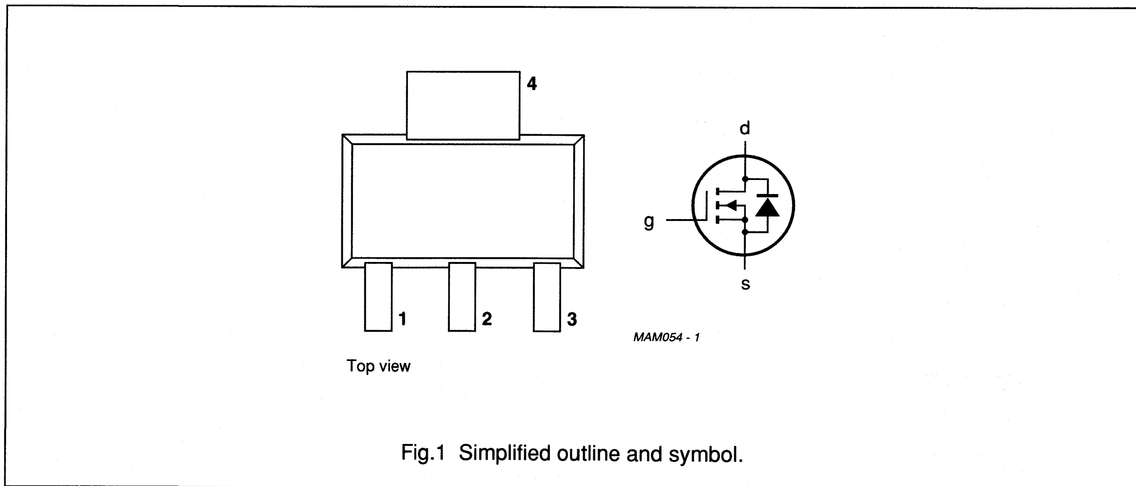


Fig.1 Simplified outline and symbol.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Drain current (peak)	I_{DM}	max.	800	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board 40 mm × 40 mm × 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage I_D = 10 µA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200	V
Drain-source leakage current V_{DS} =160 V; V_{GS} = 0	I_{DSS}	max.	1.0	µA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Drain-source ON-resistance (see Fig.4) I_D = 250 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	7 12	Ω Ω
Gate threshold voltage I_D = 1 mA; V_{GS} = V_{DS}	$V_{GS(th)}$	min. max.	0.8 2.8	V V
Transfer admittance I_D = 250 mA; V_{DS} = 15 V	$\lvert Y_{fs} \rvert$	min. typ.	125 250	mS mS
Input capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	45 65	pF pF
Output capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	20 30	pF pF

Feedback capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	5 pF 10 pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ. max.	3 ns 6 ns
	t_{off}	typ. max.	15 ns 20 ns

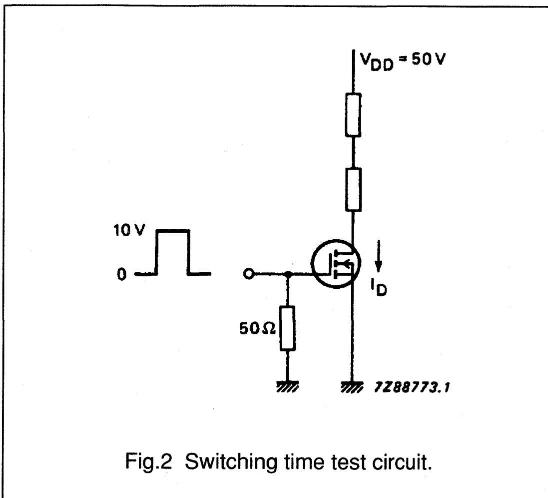


Fig.2 Switching time test circuit.

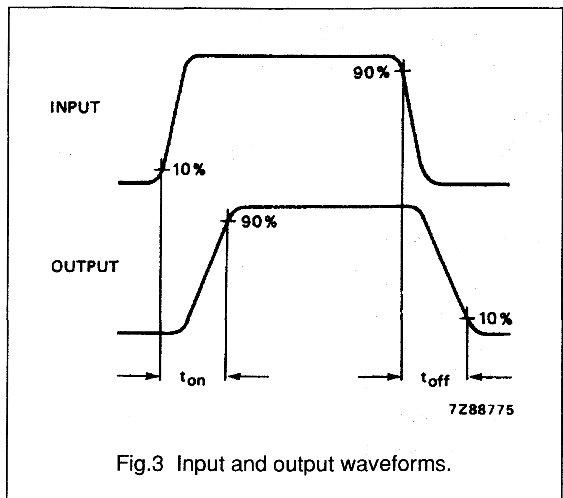


Fig.3 Input and output waveforms.

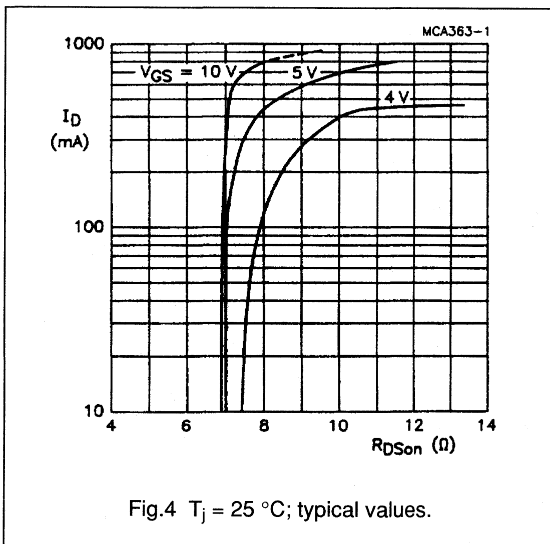


Fig.4 T_j = 25 °C; typical values.

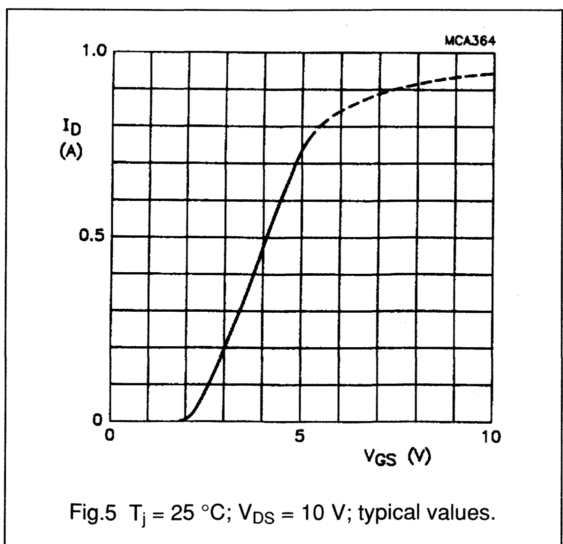


Fig.5 T_j = 25 °C; V_{DS} = 10 V; typical values.

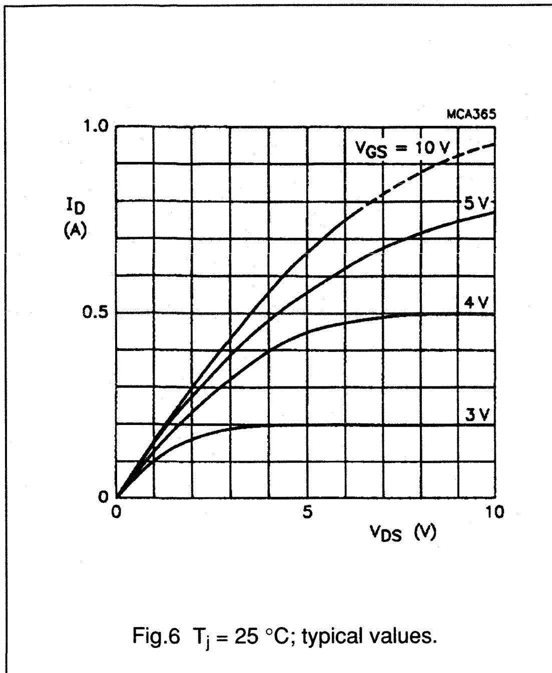


Fig.6 T_j = 25 °C; typical values.

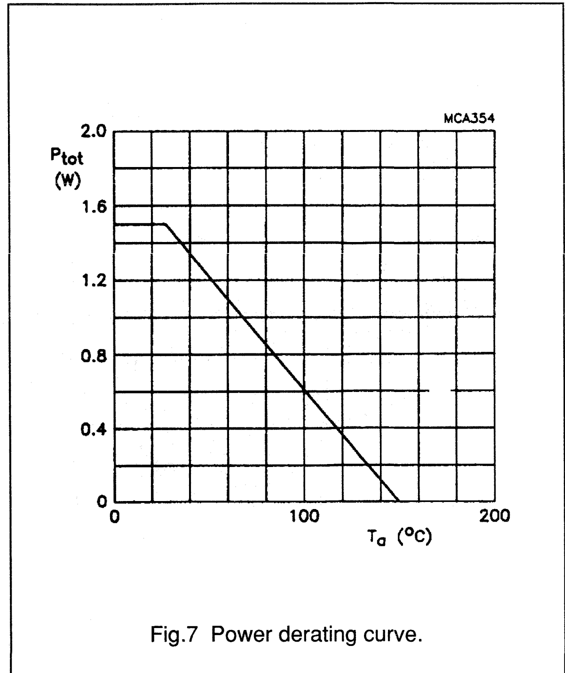


Fig.7 Power derating curve.

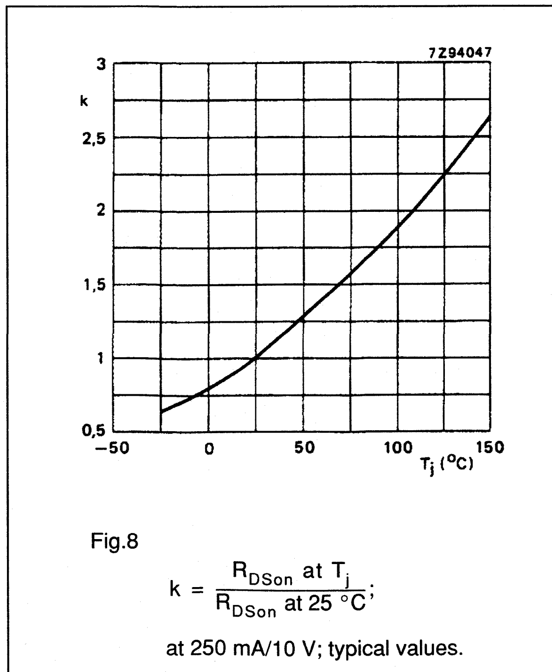


Fig.8

$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C};$$

at 250 mA/10 V; typical values.

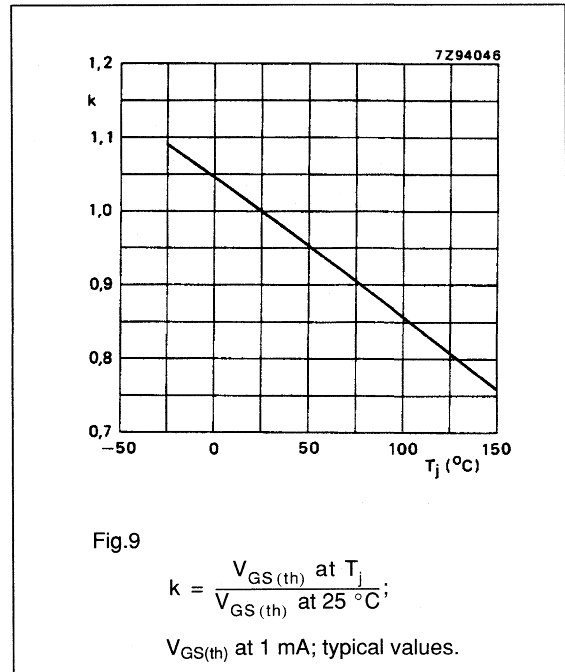


Fig.9

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C};$$

$V_{GS(th)}$ at 1 mA; typical values.

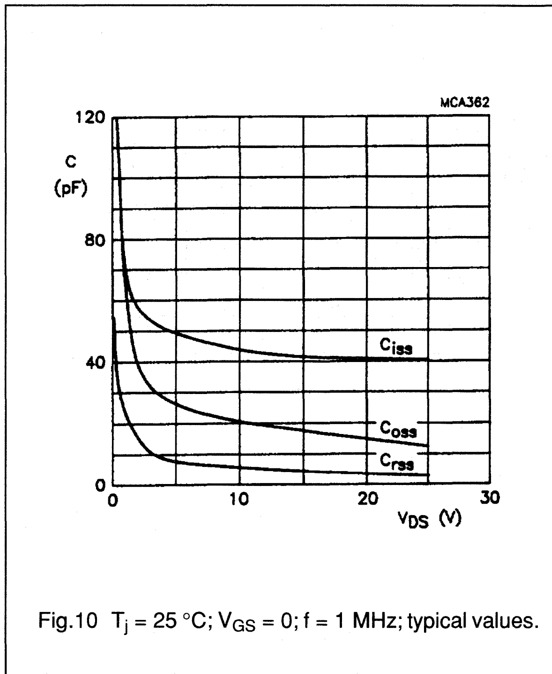


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-channel enhancement mode vertical D-MOS transistor

BSP121

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and designed for use as a line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	350	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1.5	W
Drain-source on-resistance I_D = 400 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	4.5	Ω
		max.	6.0	Ω
Transfer admittance I_D = 400 mA; V_{DS} = 25 V	$\lvert Y_{fs} \rvert$	min.	200	mS
		typ.	350	mS

PINNING - SOT223

1 = gate
2 = drain
3 = source
4 = drain

Marking code

BSP121

PIN CONFIGURATION

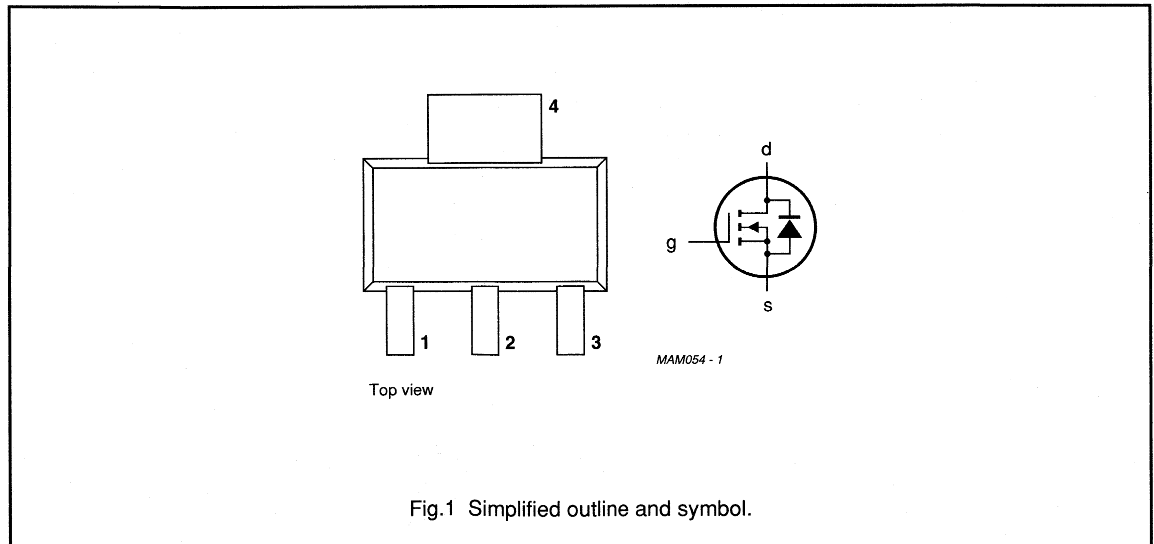


Fig.1 Simplified outline and symbol.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	350	mA
Drain current (peak)	I_{DM}	max.	1.2	A
Total power dissipation up to $T_{amb} = 25$ °C (note 1)	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{thj\text{-}a}$	=	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board 40 mm × 40 mm × 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value	Unit
Drain-source breakdown voltage				
I_D = 10 µA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200	V
Drain-source leakage current				
V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	max.	1.0	µA
V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	200	nA
Gate-source leakage current				
± V_{GS} = 20 V; V_{DS} = 0	$\pm I_{GSS}$	max.	100	nA
Gate threshold voltage				
I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.0	V
		max.	2.8	V
Drain-source on-resistance				
I_D = 400 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	4.5	Ω
		max.	6.0	Ω
Transfer admittance				
I_D = 400 mA; V_{DS} = 25 V	$\|Y_{fs}\|$	min.	200	mS
		typ.	350	mS
Input capacitance at f = 1 MHz				
V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ.	45	pF
		max.	60	pF
Output capacitance at f = 1 MHz				
V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ.	15	pF
		max.	25	pF
Feedback capacitance at f = 1 MHz				
V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ.	3.5	pF
		max.	10	pF
Switching times (see Figs 2 and 3)				
I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	5	pF
		max.	10	pF
	t_{off}	typ.	15	ns
		max.	20	ns

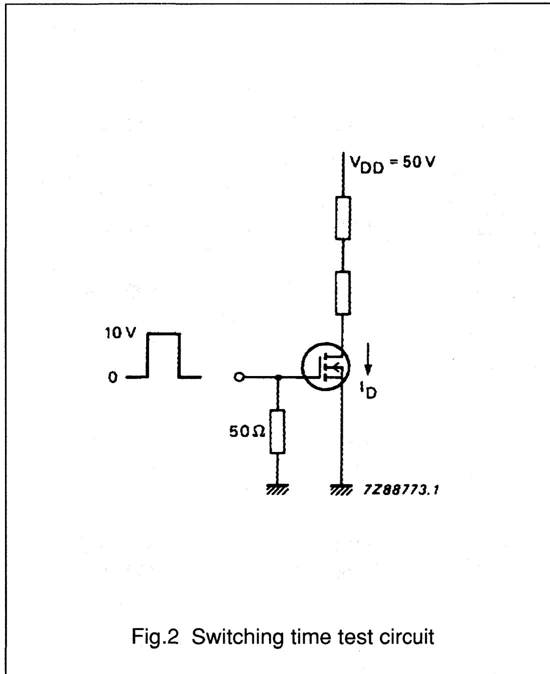


Fig.2 Switching time test circuit

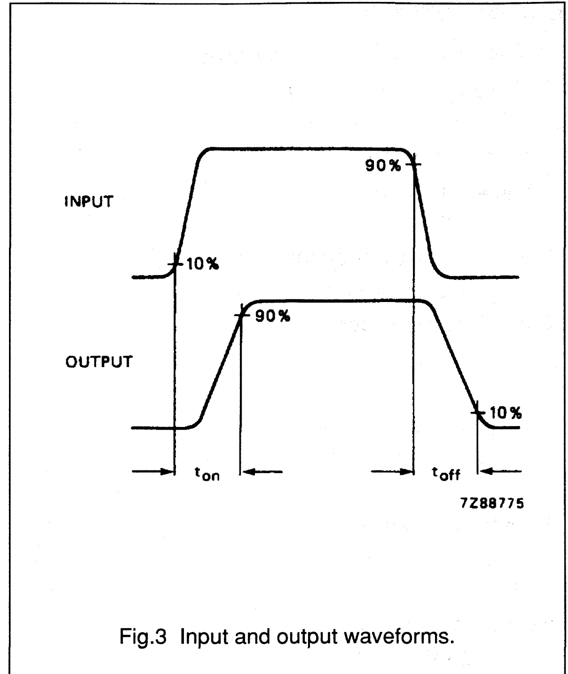


Fig.3 Input and output waveforms.

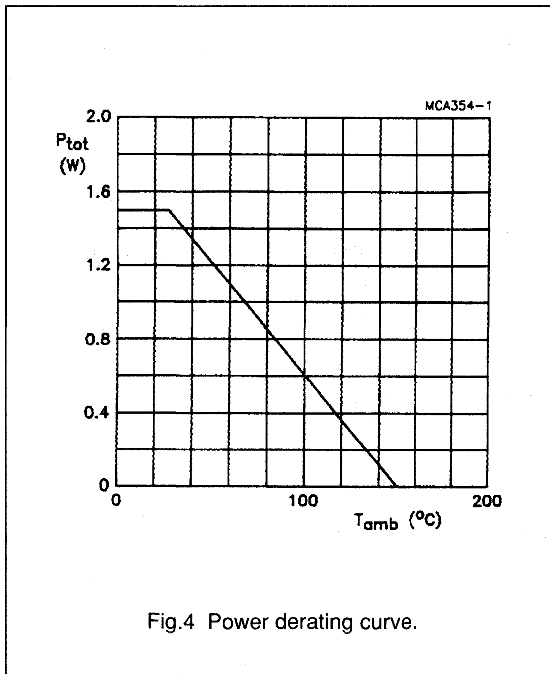


Fig.4 Power derating curve.

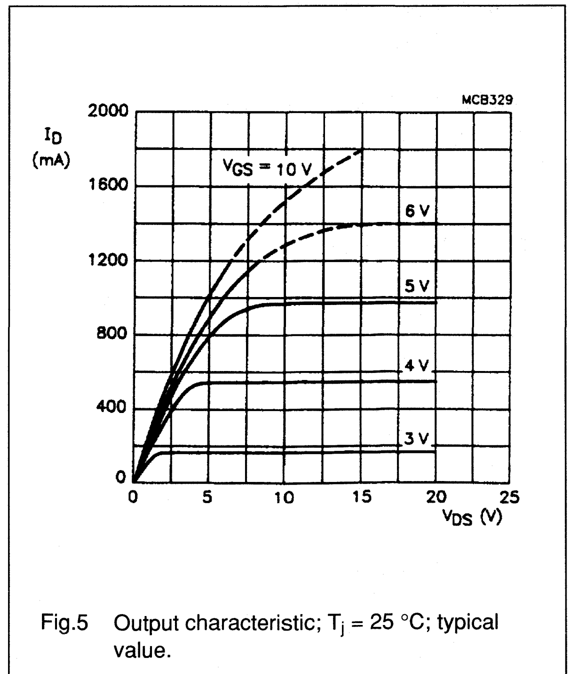


Fig.5 Output characteristic; T_j = 25 °C; typical value.

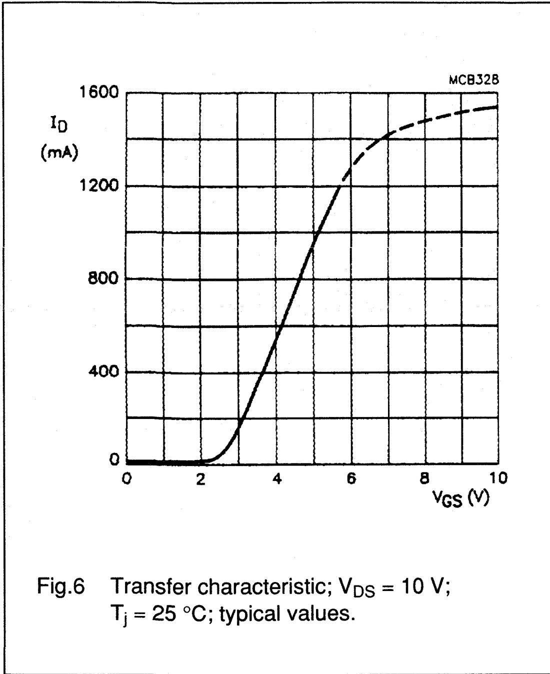


Fig.6 Transfer characteristic; V_{DS} = 10 V; T_j = 25 °C; typical values.

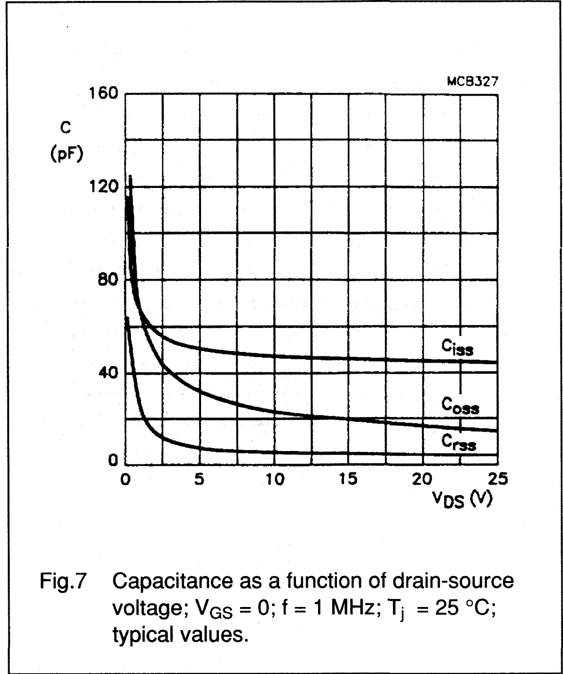


Fig.7 Capacitance as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C; typical values.

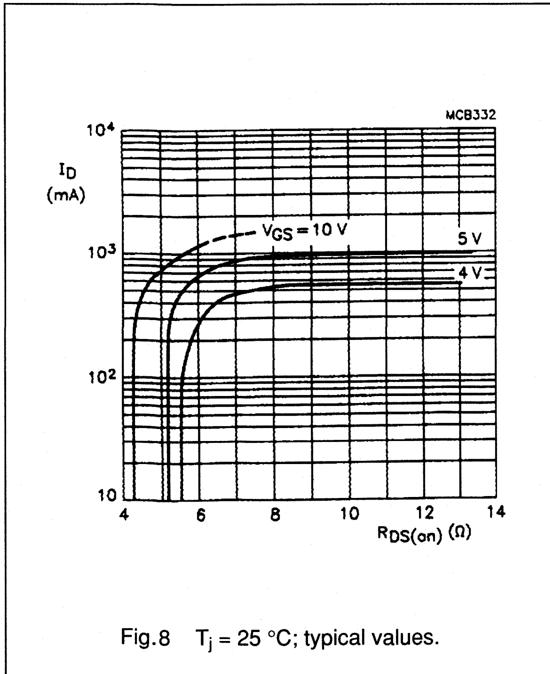


Fig.8 T_j = 25 °C; typical values.

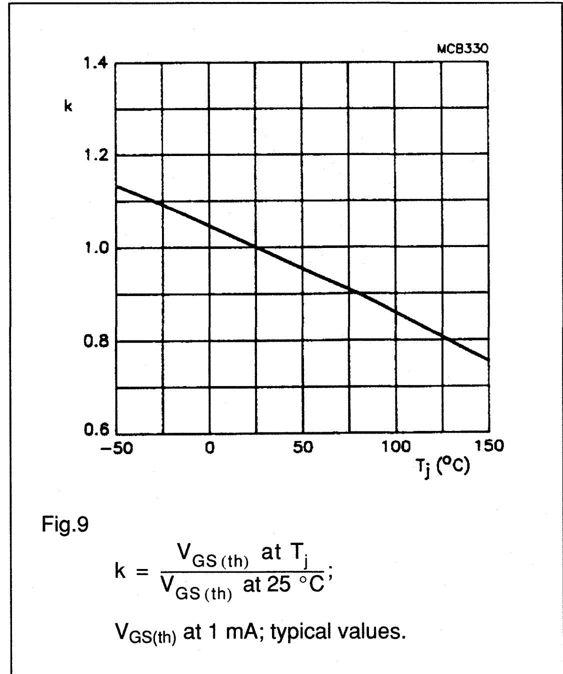


Fig.9

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C};$$

$V_{GS(th)}$ at 1 mA; typical values.

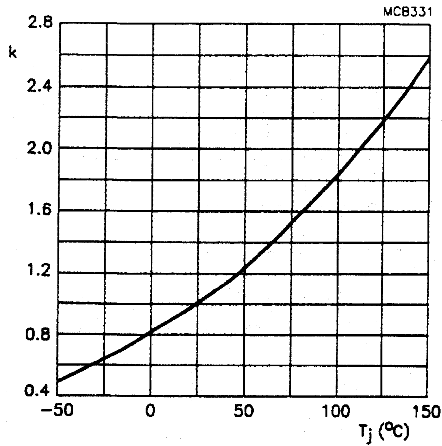


Fig.10

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C};$$

at 400 mA/10 V; typical values.

N-channel enhancement mode vertical D-MOS transistor

BSP122

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	200	V
I_D	DC drain current	550	mA
$R_{DS(on)}$	drain-source on-resistance	2.5	Ω
$V_{GS(th)}$	gate-source threshold voltage	2	V

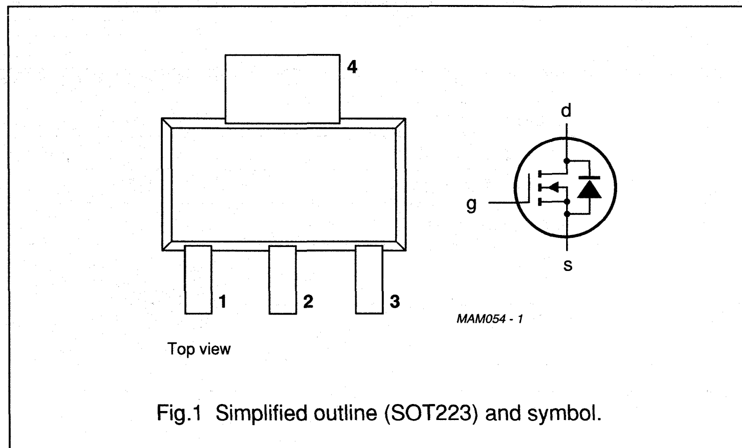


Fig.1 Simplified outline (SOT223) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	550	mA
I_{DM}	peak drain current		–	3	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3 K/W

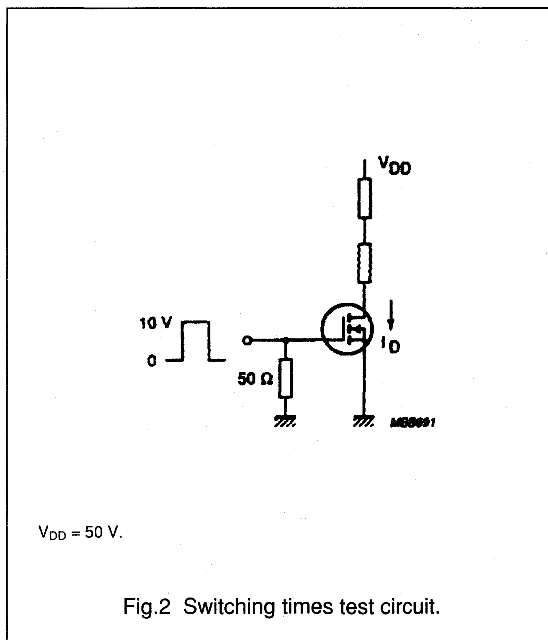
Note

1. Device mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 µA; V_{GS} = 0	200	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 160 V; V_{GS} = 0	–	–	1	µA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.4	–	2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 750 mA; V_{GS} = 10 V	–	1.6	2.5	Ω
		I_D = 20 mA; V_{GS} = 2.4 V	–	2.5	–	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 750 mA; V_{DS} = 25 V	400	800	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	165	–	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	40	–	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	9	–	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 750 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	–	35	ns
t_{off}	turn-off time	I_D = 750 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	–	50	ns



V_{DD} = 50 V.

Fig.2 Switching times test circuit.

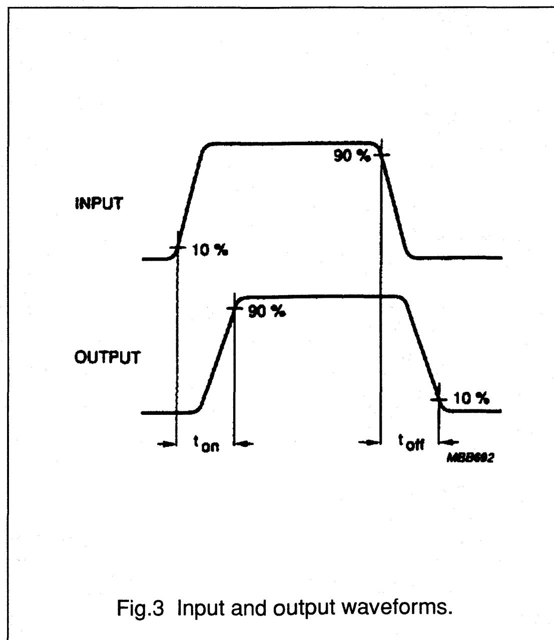


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BSP126

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and designed for use as a line interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching.
- No secondary breakdown.

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	250	V
Drain current (DC)	I_D	max.	350	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1.5	W
Drain-source on-resistance				
I_D = 300 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	5.0	Ω
		max.	7.0	Ω
Gate-source threshold voltage	$V_{GS(th)}$	max.	2	V

PINNING - SOT223

1 = gate
2 = drain
3 = source
4 = drain

Marking code

BSP126

PIN CONFIGURATION

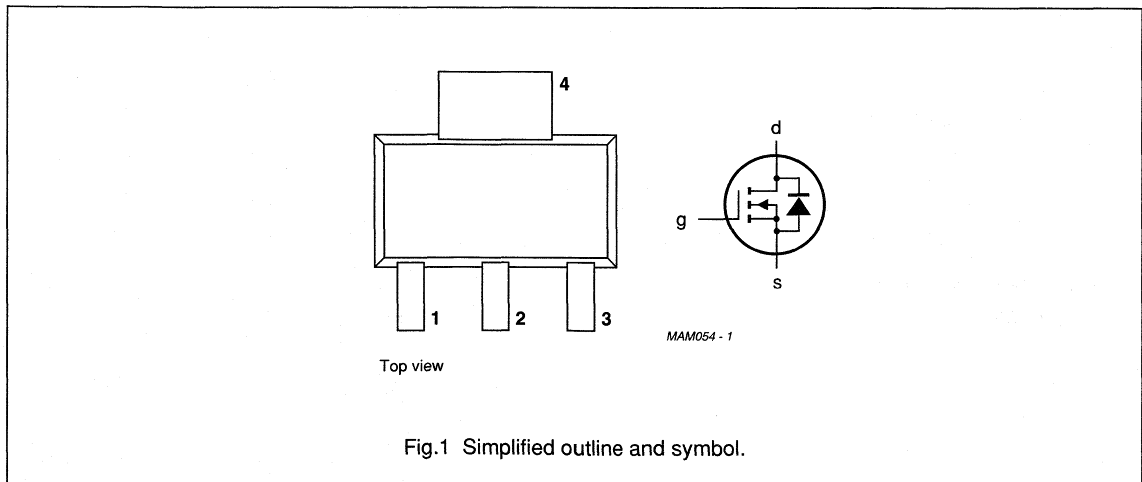


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BSP126

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	250	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	350	mA
Drain current (peak)	I_{DM}	max.	1.2	A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board 40 mm × 40 mm × 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage				
I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	250	V
Drain-source leakage current				
V_{DS} = 200 V; V_{GS} = 0	I_{DSS}	max.	1.0	μA
Gate-source leakage current				
± V_{GS} = 20 V; V_{DS} = 0	$\pm I_{GSS}$	max.	100	nA
Gate threshold voltage				
I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.8	V
		max.	2.0	V
Drain-source on-resistance				
I_D = 300 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	5.0	Ω
		max.	7.0	Ω
I_D = 20 mA; V_{GS} = 2.4 V	$R_{DS(on)}$	max.	10	Ω
Transfer admittance				
I_D = 300 mA; V_{DS} = 25 V	$\lvert Y_{fs} \rvert$	min.	200	mS
		typ.	400	mS
Input capacitance at f = 1 MHz;				
V_{DS} = 25 V; V_{GS} = 0	C_{iss}	typ.	65	pF
		max.	90	pF
Output capacitance at f = 1 MHz;				
V_{DS} = 25 V; V_{GS} = 0	C_{oss}	typ.	20	pF
		max.	30	pF

Feedback capacitance at f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{rss}	typ.	5 pF
		max.	15 pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	5 ns
		max.	10 ns
	t_{off}	typ.	20 ns
		max.	30 ns

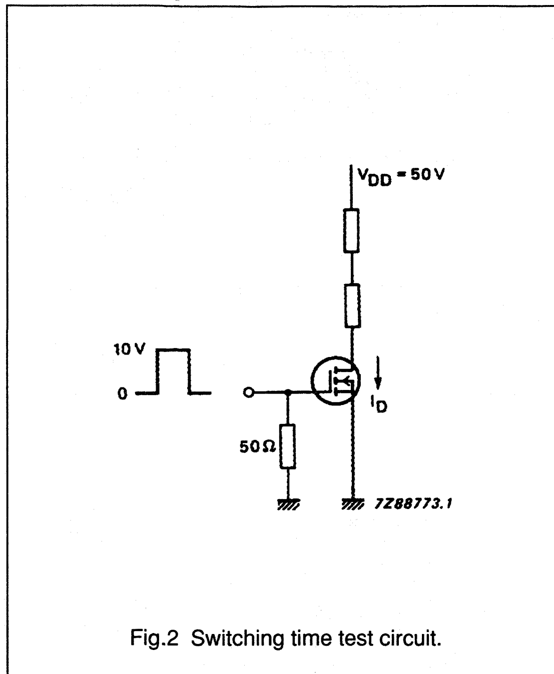


Fig.2 Switching time test circuit.

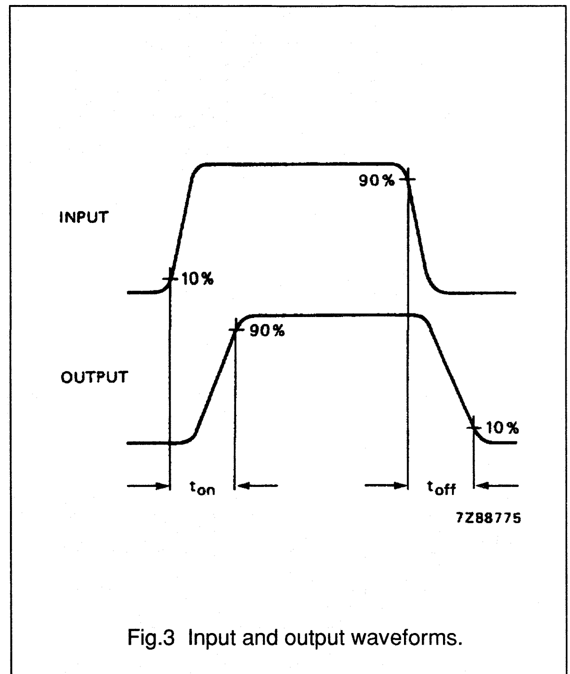


Fig.3 Input and output waveforms.

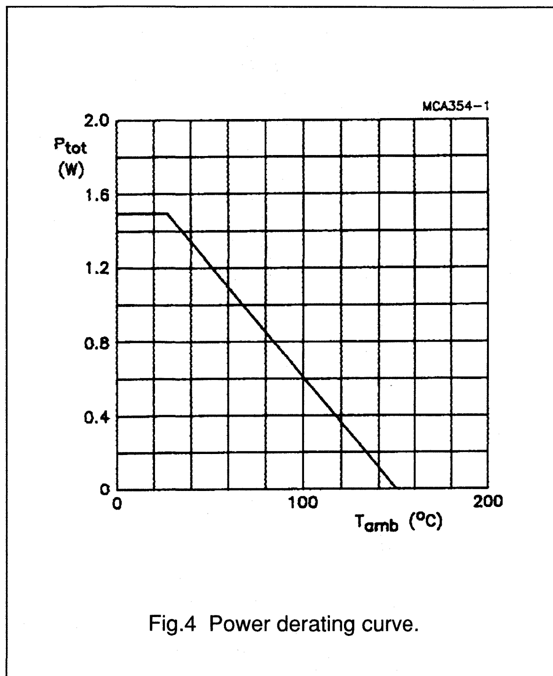


Fig.4 Power derating curve.

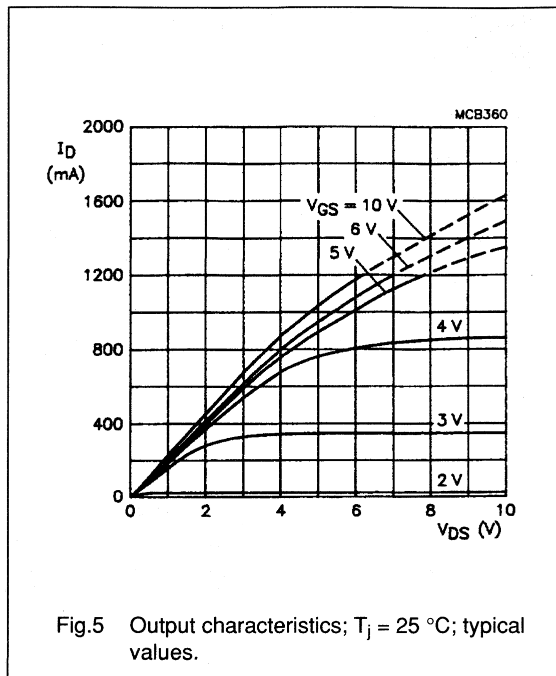


Fig.5 Output characteristics; T_j = 25 °C; typical values.

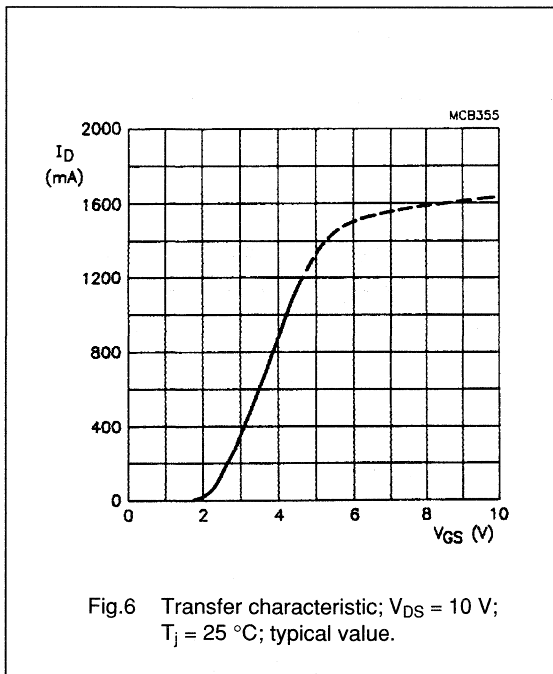


Fig.6 Transfer characteristic; V_{DS} = 10 V; T_j = 25 °C; typical value.

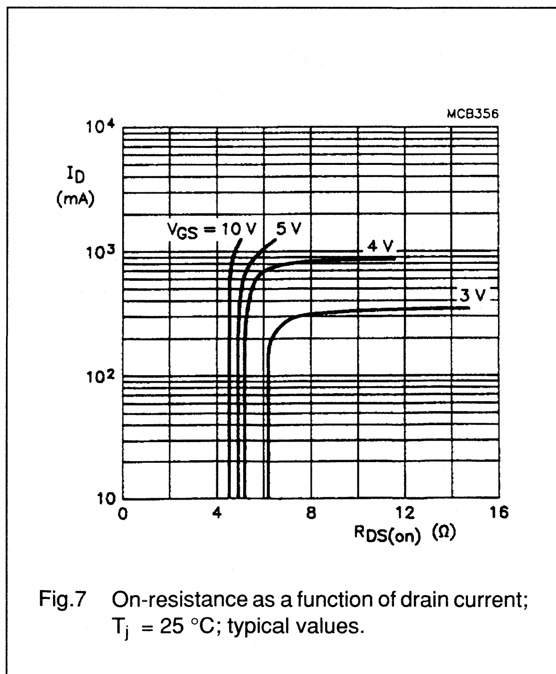


Fig.7 On-resistance as a function of drain current; T_j = 25 °C; typical values.

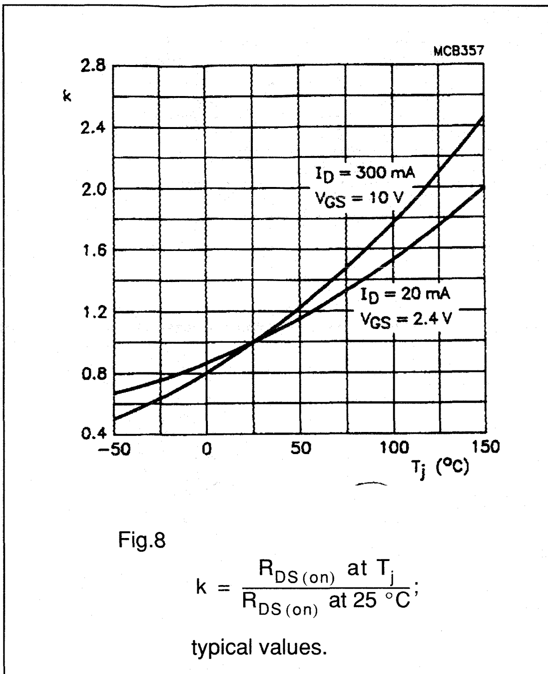


Fig.8

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C};$$

typical values.

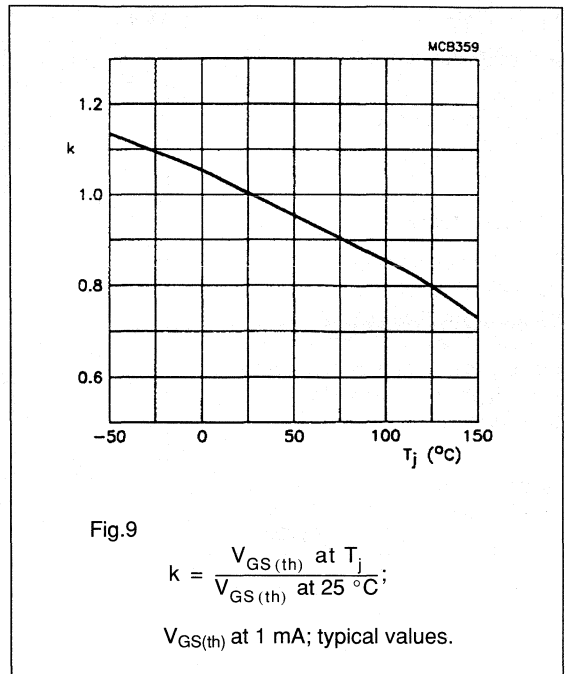


Fig.9

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C};$$

$V_{GS(th)}$ at 1 mA; typical values.

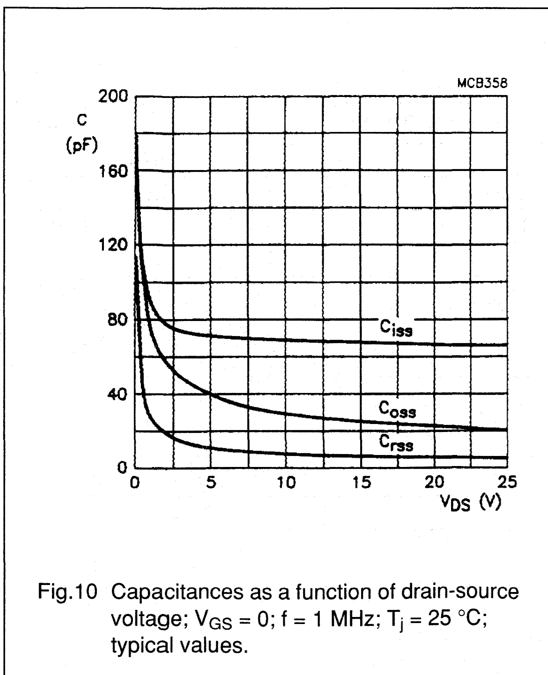


Fig.10 Capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C; typical values.

N-channel enhancement mode vertical D-MOS transistor

BSP127

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
Code: BSP127	
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	270	V
I_D	DC drain current	350	mA
$R_{DS(on)}$	drain-source on-resistance	8	Ω
$V_{GS(th)}$	gate-source threshold voltage	2	V

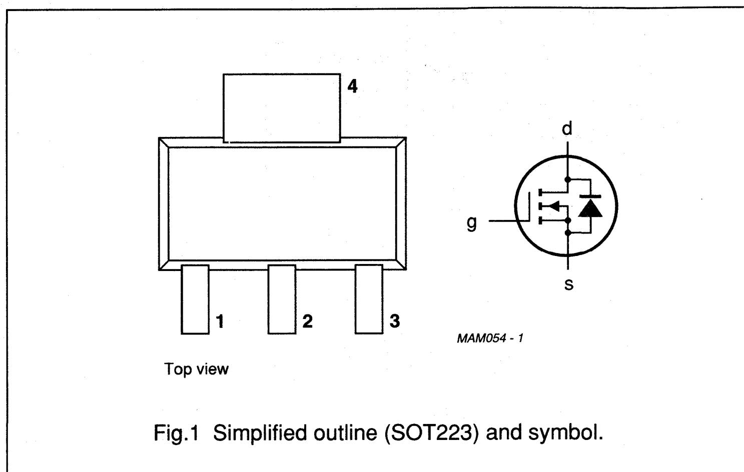


Fig.1 Simplified outline (SOT223) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	270	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	350	mA
I_{DM}	peak drain current		–	1.4	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3 K/W

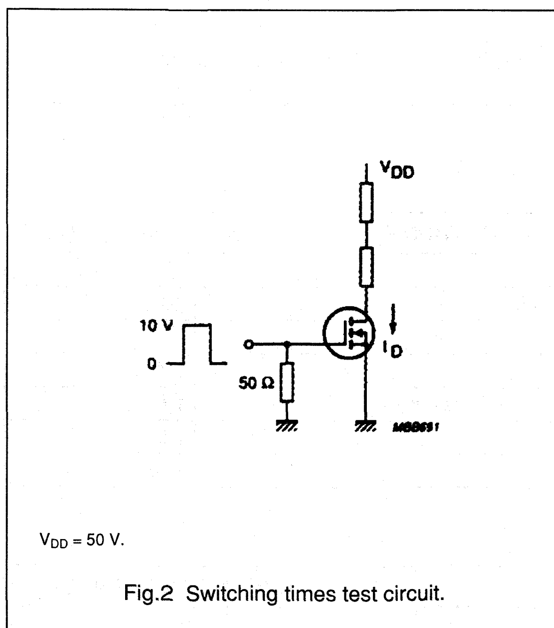
Note

1. Device mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	270	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 220 V; V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.8	–	2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 250 mA; V_{GS} = 10 V	–	6.5	8	Ω
		I_D = 20 mA; V_{GS} = 2.4 V	–	9	14	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA; V_{DS} = 25 V	200	400	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	55	80	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	5	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	20	30	ns



V_{DD} = 50 V.

Fig.2 Switching times test circuit.

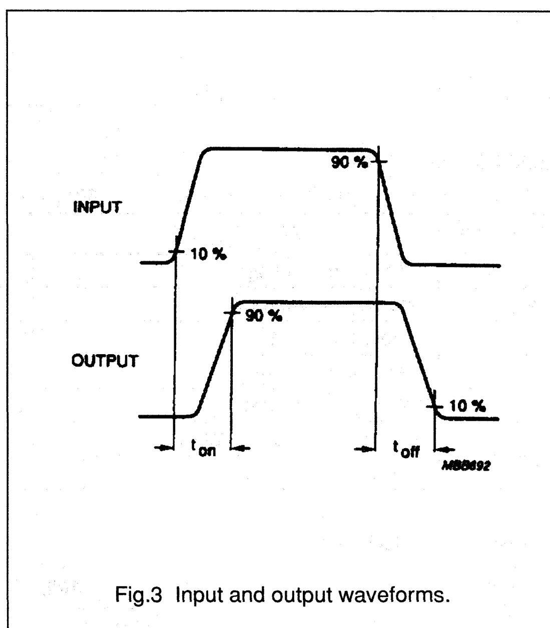


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BSP128

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
Code: BSP128	
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	drain-source voltage	200	V
I_D	DC drain current	350	mA
$R_{DS(on)}$	drain-source on-resistance	8	Ω
$V_{GS(th)}$	gate-source threshold voltage	1.8	V

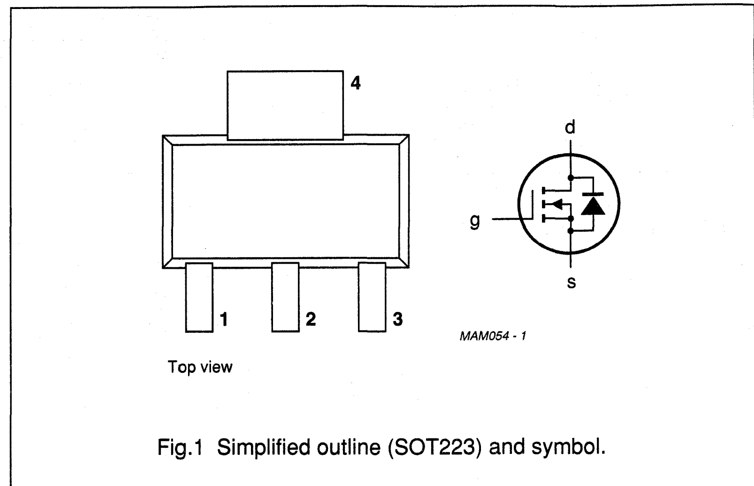


Fig.1 Simplified outline (SOT223) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	350	mA
I_{DM}	peak drain current		–	1.4	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3 K/W

Note

1. Device mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm^2.

N-channel enhancement mode vertical D-MOS transistor

BSP128

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	200	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 160 V; V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{GS} = V_{DS}	0.4	–	1.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 100 mA; V_{GS} = 2.8 V	–	5	8	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 300 mA; V_{DS} = 25 V	200	400	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	50	80	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	5	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	20	30	ns

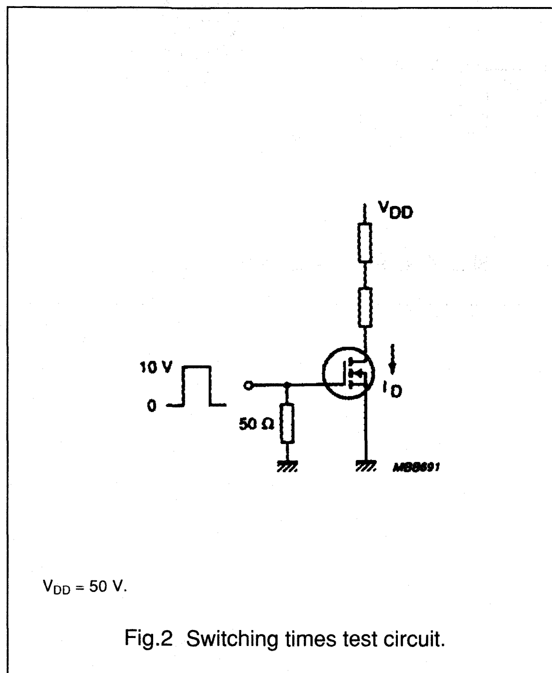


Fig.2 Switching times test circuit.

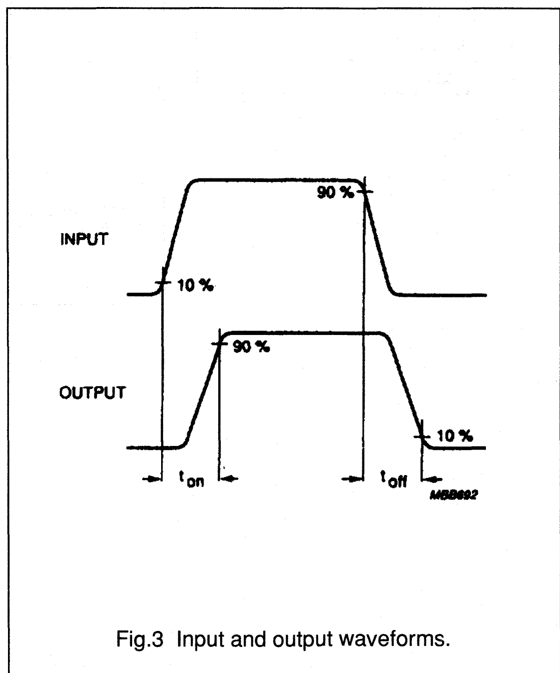


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BSP130

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

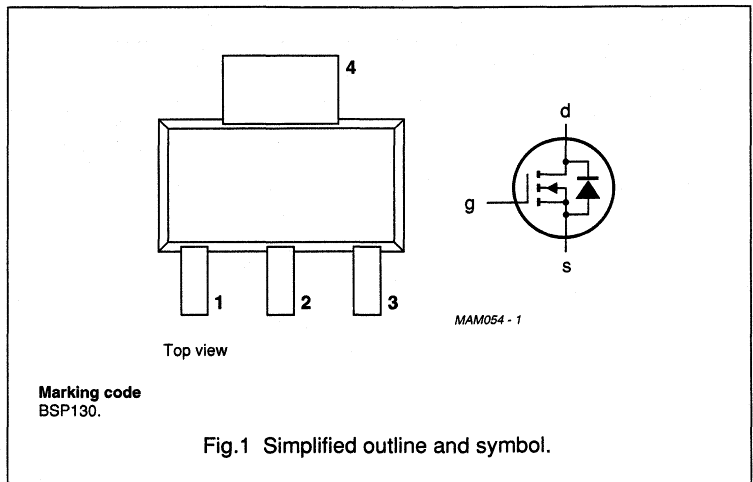
N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	300	V
I_D	DC drain current		–	300	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	1.5	W
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 250 mA; V_{GS} = 10 V	–	8	Ω
$V_{GS(off)}$	gate-source cut-off voltage	I_D = 1 mA; V_{DS} = V_{GS}	0.8	2	V



Marking code
BSP130.

Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	300	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	300	mA
I_{DM}	peak drain current		–	1.4	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	1.5	W
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient; note 1	83.3 K/W

Note

1. Device mounted on an epoxy printed-circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm^2.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA; V_{GS} = 0	300	–	–	V
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}	0.8	–	2	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA; V_{GS} = 2.4 V	–	7.9	14	Ω
		I_D = 250 mA; V_{GS} = 10 V	–	6.7	8	Ω
I_{DSS}	drain-source leakage current	V_{DS} = 240 V; V_{GS} = 0	–	–	100	nA
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA; V_{DS} = 25 V	200	380	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	57	90	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	15	30	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	2.6	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	2.5	10	ns
t_{off}	turn-off time	I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 10 to 0 V	–	17	30	ns

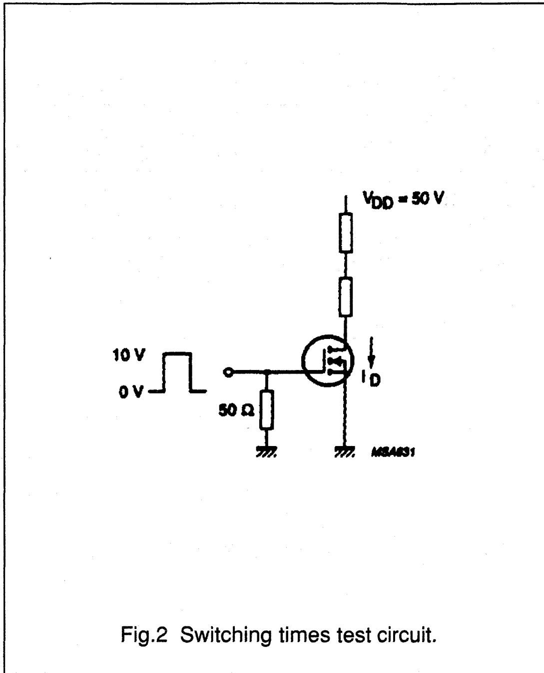


Fig.2 Switching times test circuit.

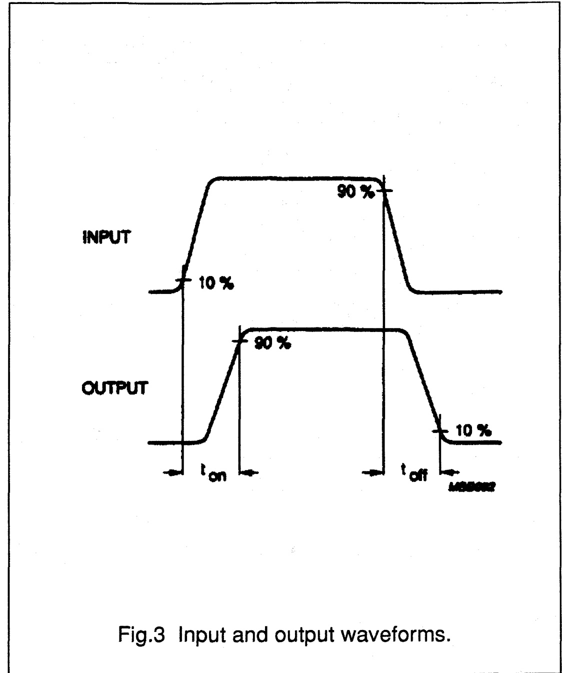


Fig.3 Input and output waveforms.

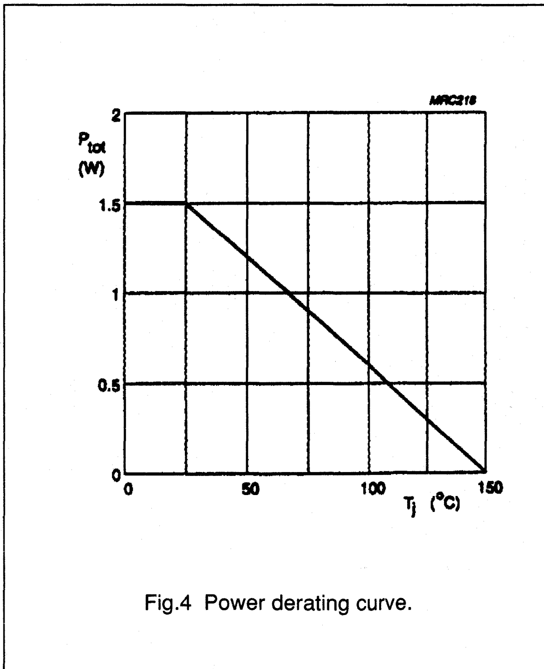
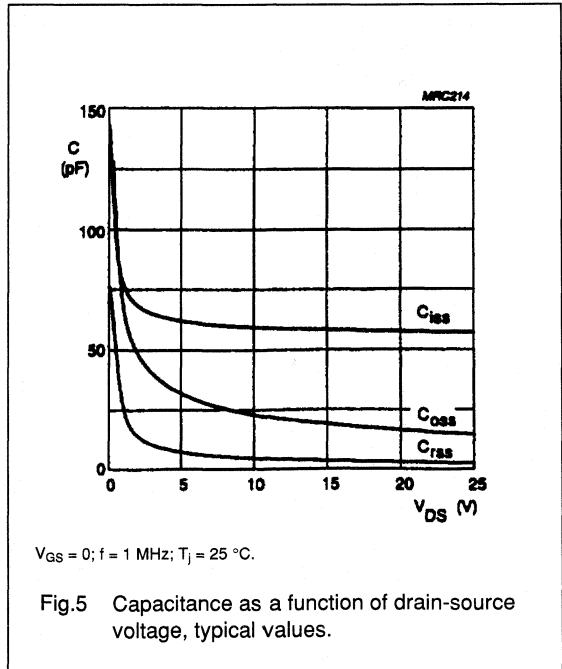
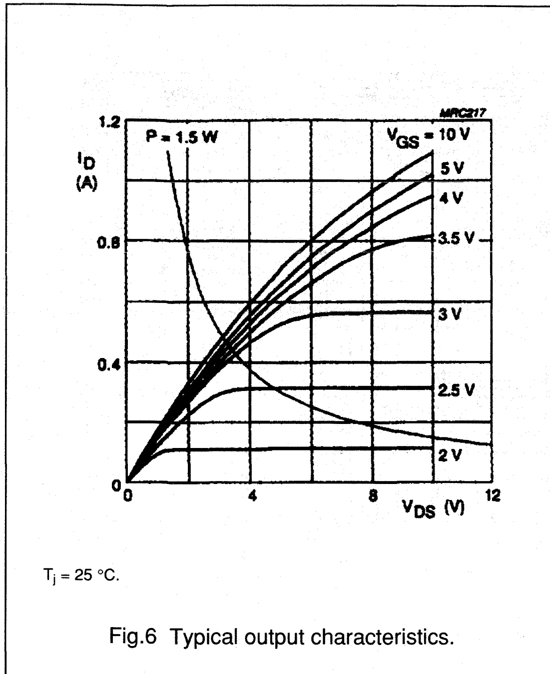


Fig.4 Power derating curve.



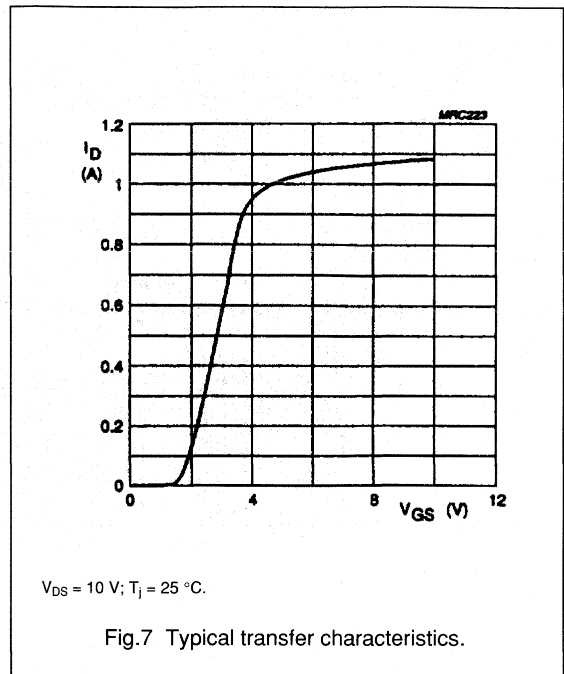
$V_{GS} = 0$; f = 1 MHz; $T_j = 25$ °C.

Fig.5 Capacitance as a function of drain-source voltage, typical values.



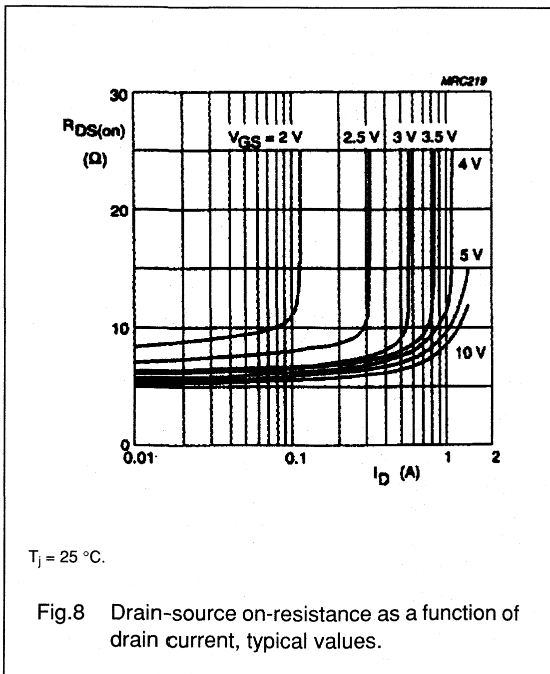
T_j = 25 °C.

Fig.6 Typical output characteristics.



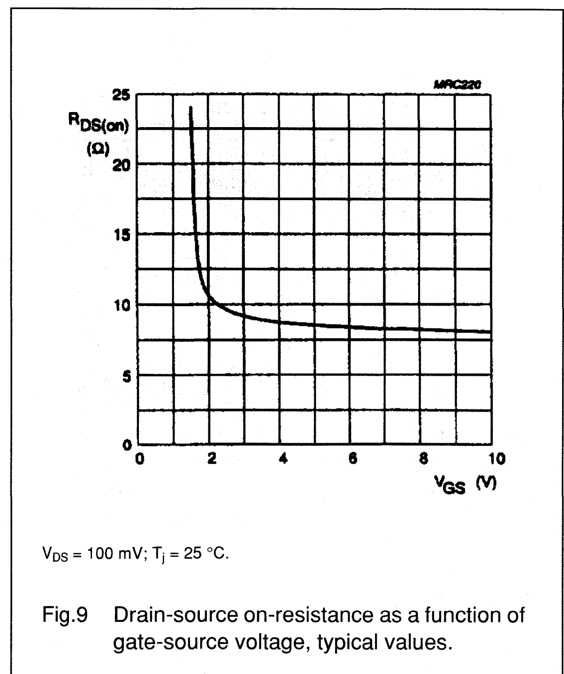
V_{DS} = 10 V; T_j = 25 °C.

Fig.7 Typical transfer characteristics.



T_j = 25 °C.

Fig.8 Drain-source on-resistance as a function of drain current, typical values.



V_{DS} = 100 mV; T_j = 25 °C.

Fig.9 Drain-source on-resistance as a function of gate-source voltage, typical values.

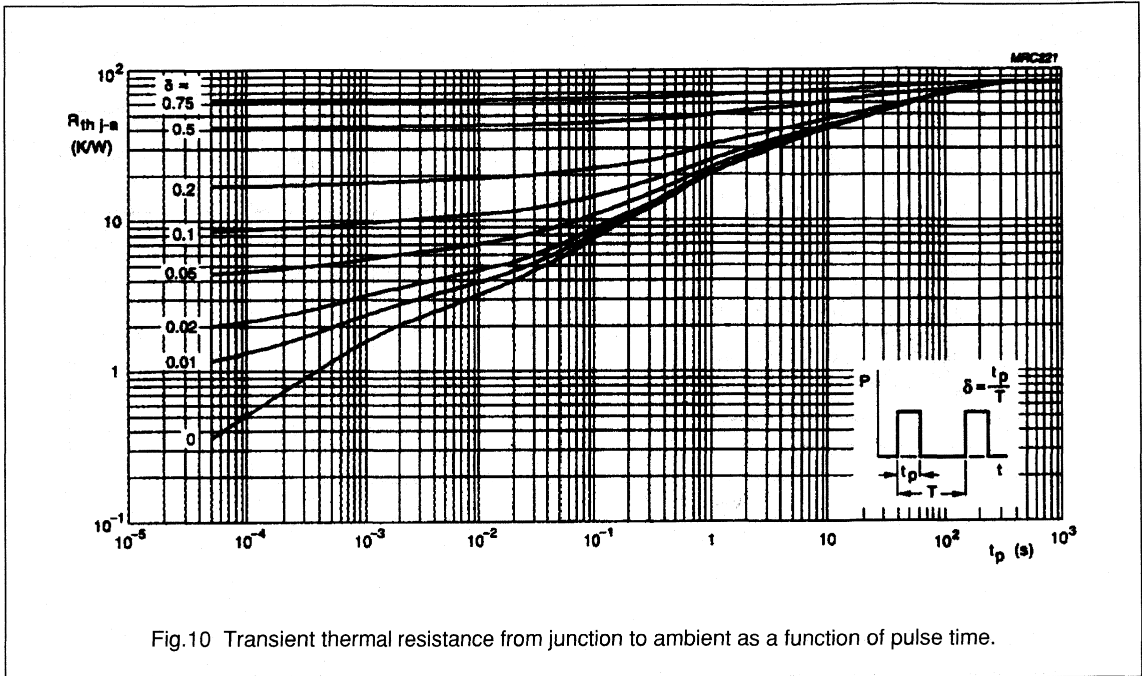
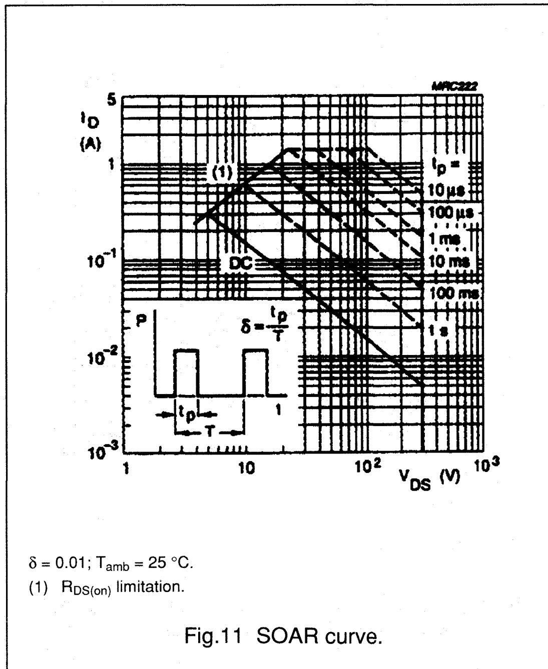


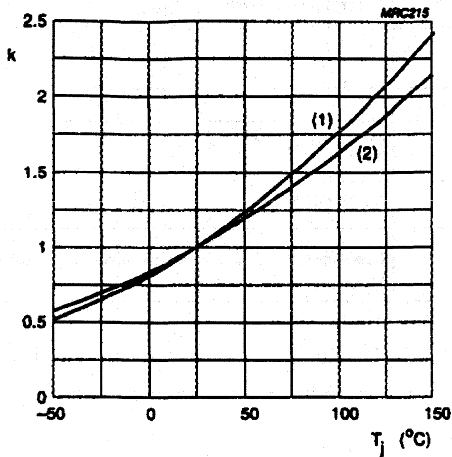
Fig.10 Transient thermal resistance from junction to ambient as a function of pulse time.



$\delta = 0.01$; $T_{amb} = 25$ °C.

(1) $R_{DS(on)}$ limitation.

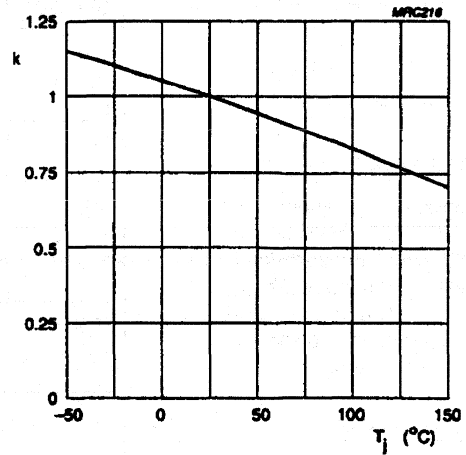
Fig.11 SOAR curve.



$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$

Typical $R_{DS(on)}$;
(1) I_D = 250 mA; V_{GS} = 10 V.
(2) I_D = 20 mA; V_{GS} = 2.4 V.

Fig.12 Temperature coefficient of drain-source on-resistance.



$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C}$.

Typical $V_{GS(th)}$ at 1 mA.

Fig.13 Temperature coefficient of gate-source threshold voltage.

N-channel enhancement mode vertical D-MOS transistor

BSP152

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
I_D	DC drain current		–	550	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	1.5	W
$\pm V_{GSO}$	gate-source voltage	open drain	–	40	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 750 mA; V_{GS} = 10 V	–	2.5	Ω
$V_{GS(off)}$	gate-source cut-off voltage	I_D = 1 mA; $V_{DS} = V_{GS}$	1.5	3.5	V

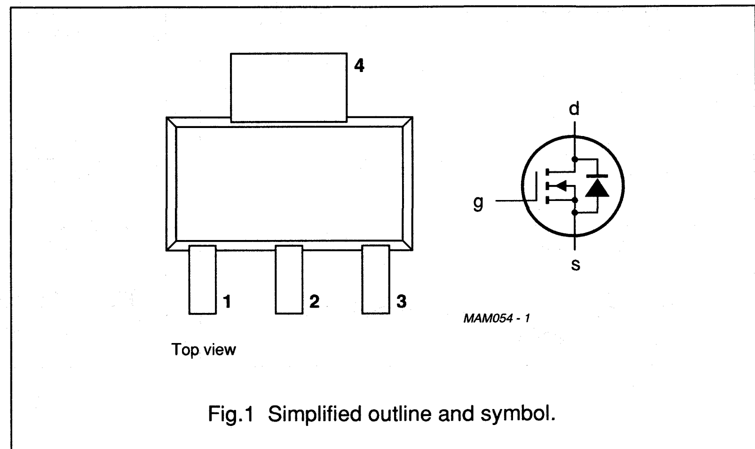


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	40	V
I_D	DC drain current		–	550	mA
I_{DM}	peak drain current		–	3	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	1.5	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient; note 1	83.3 K/W

Note

1. Device mounted on an epoxy printed-circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 mm^2.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 µA; V_{GS} = 0	200	–	–	V
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 40 V; V_{DS} = 0	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}	1.5	–	3.5	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 750 mA; V_{GS} = 10 V	–	–	2.5	Ω
I_{DSS}	drain-source leakage current	V_{DS} = 160 V; V_{GS} = 0	–	–	100	nA
$\mid Y_{fs}\mid$	transfer admittance	I_D = 750 mA; V_{DS} = 25 V	400	–	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	100	–	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	42	–	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	8	–	pF
Switching times (see Figs 2 and 33)						
t_{on}	turn-on time	I_D = 750 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	–	–	15	ns
t_{off}	turn-off time	I_D = 750 mA; V_{DD} = 50 V; V_{GS} = 10 to 0 V	–	–	30	ns

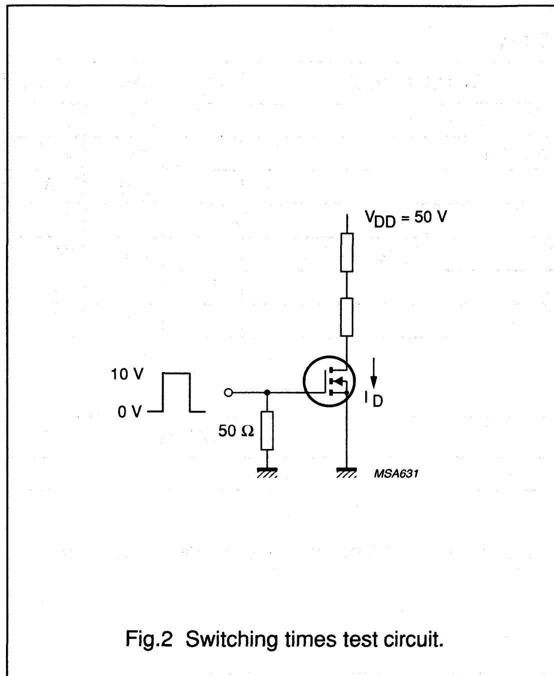


Fig.2 Switching times test circuit.

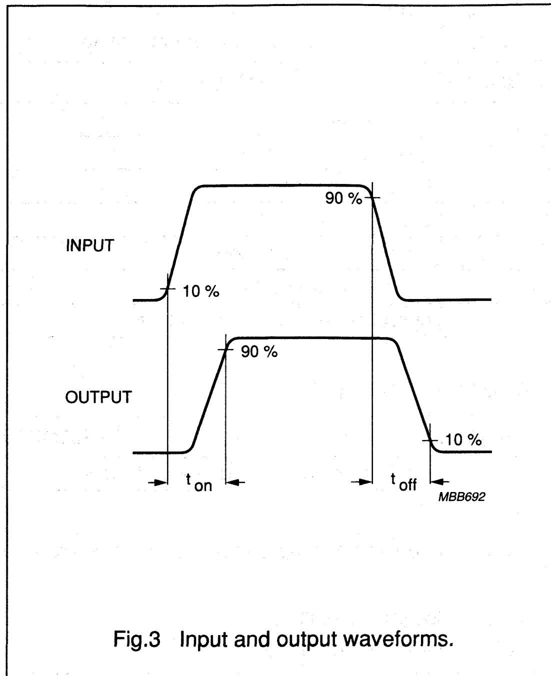


Fig.3 Input and output waveforms.

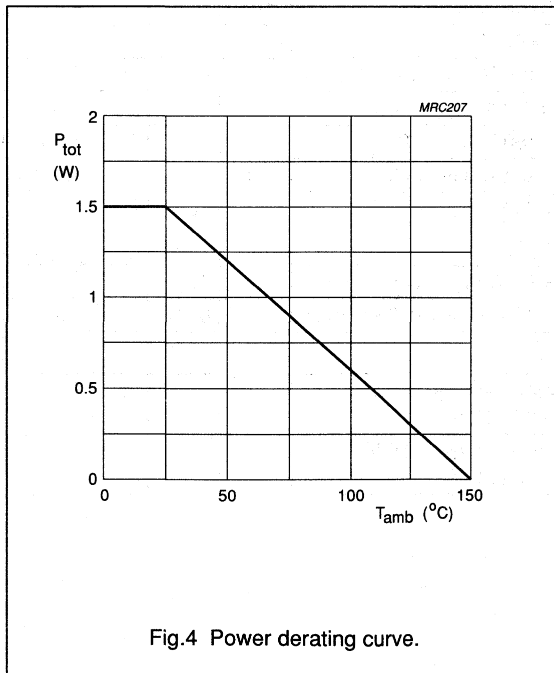
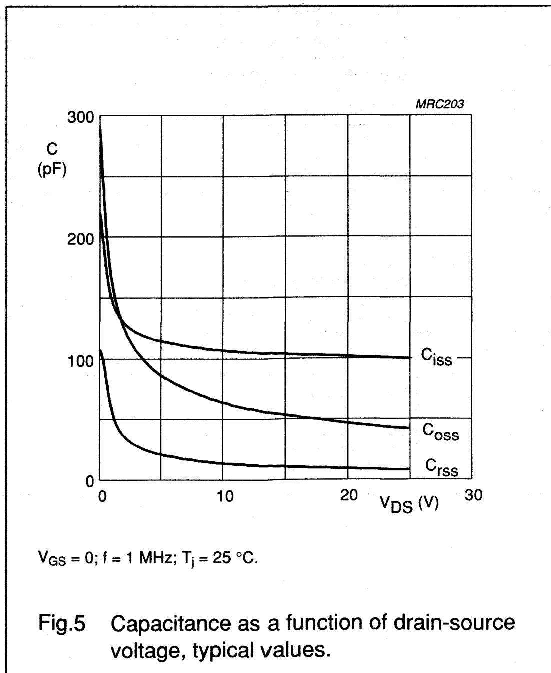
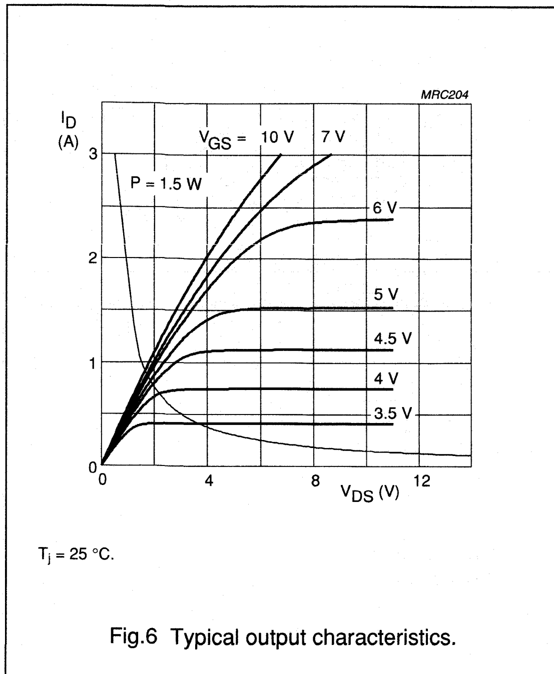


Fig.4 Power derating curve.



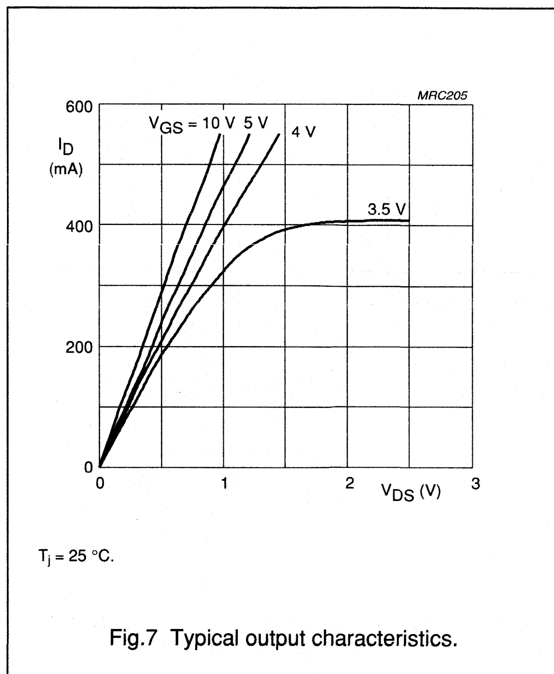
$V_{GS} = 0$; f = 1 MHz; $T_j = 25$ °C.

Fig.5 Capacitance as a function of drain-source voltage, typical values.



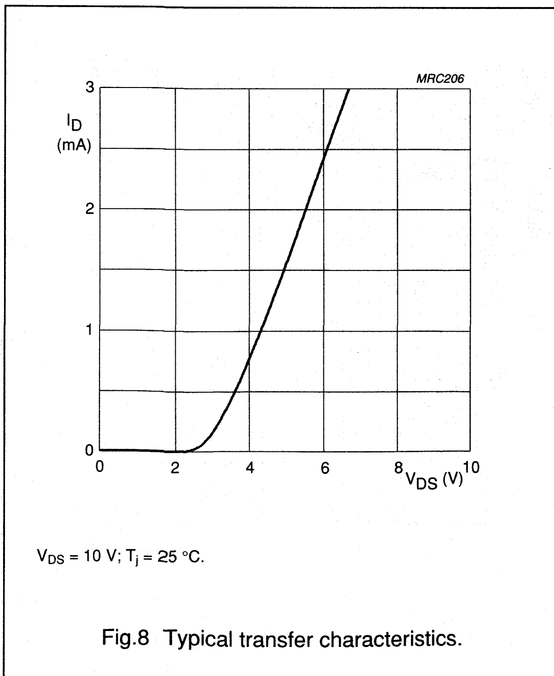
T_j = 25 °C.

Fig.6 Typical output characteristics.



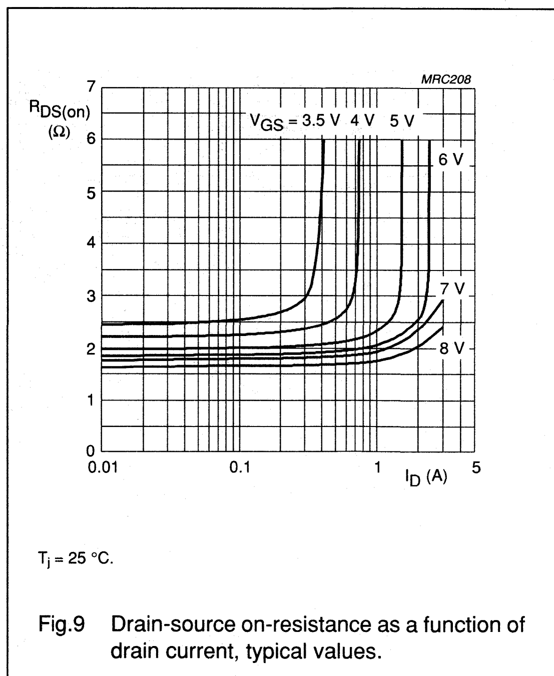
T_j = 25 °C.

Fig.7 Typical output characteristics.



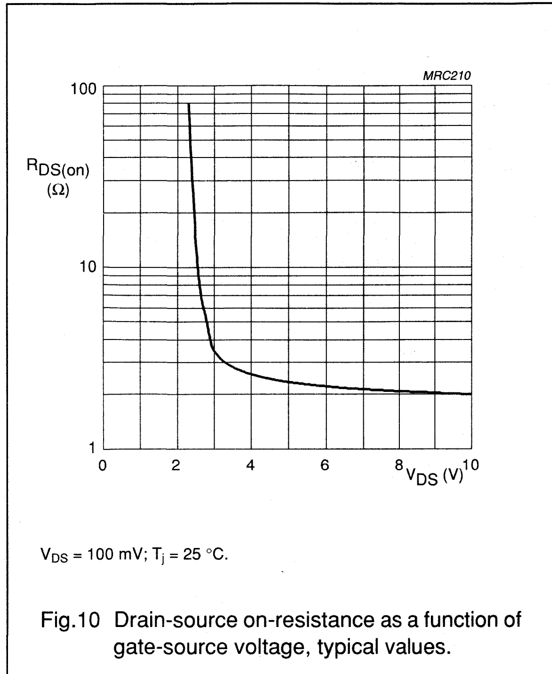
V_{DS} = 10 V; T_j = 25 °C.

Fig.8 Typical transfer characteristics.



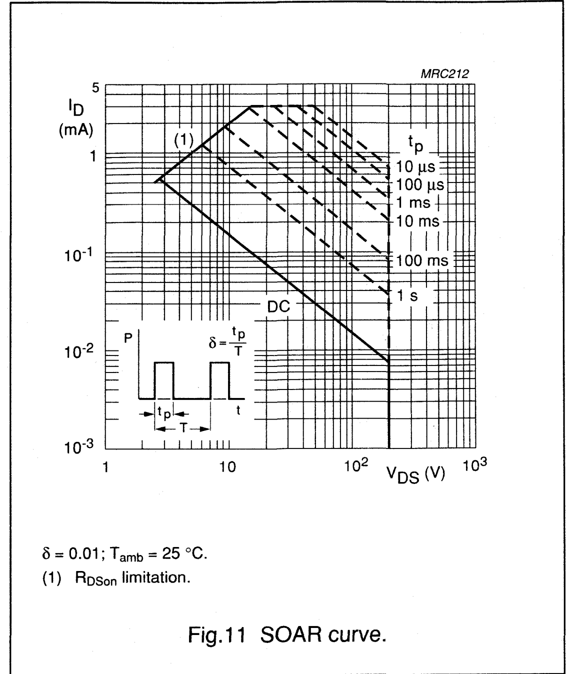
T_j = 25 °C.

Fig.9 Drain-source on-resistance as a function of drain current, typical values.



V_{DS} = 100 mV; T_j = 25 °C.

Fig.10 Drain-source on-resistance as a function of gate-source voltage, typical values.



δ = 0.01; T_{amb} = 25 °C.

(1) R_{DSon} limitation.

Fig.11 SOAR curve.

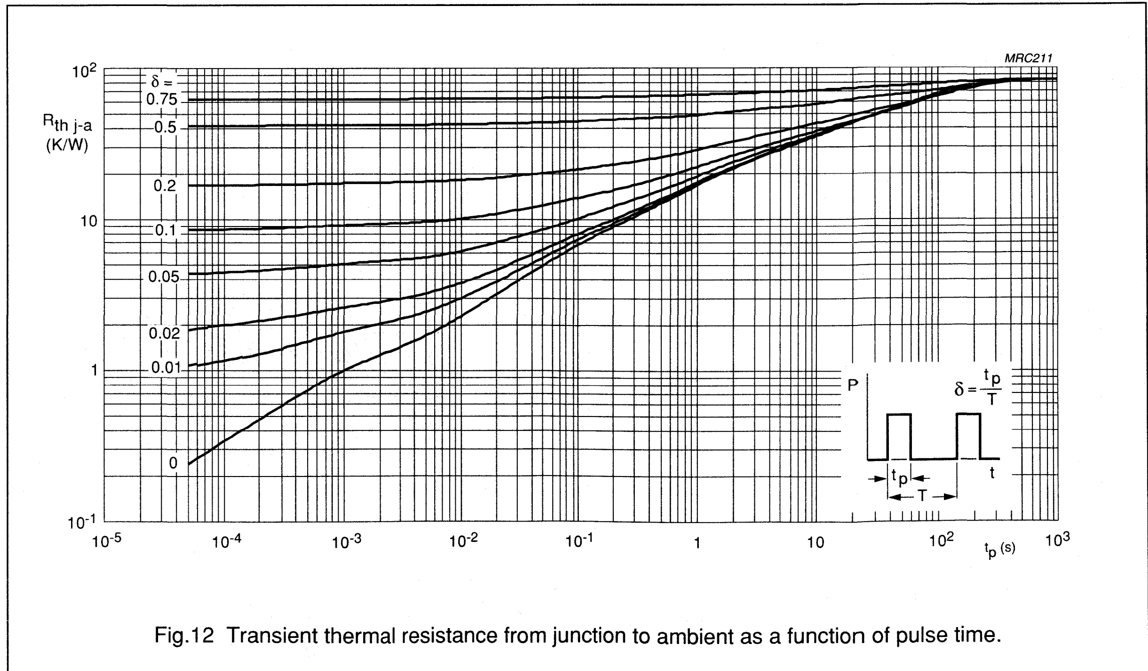
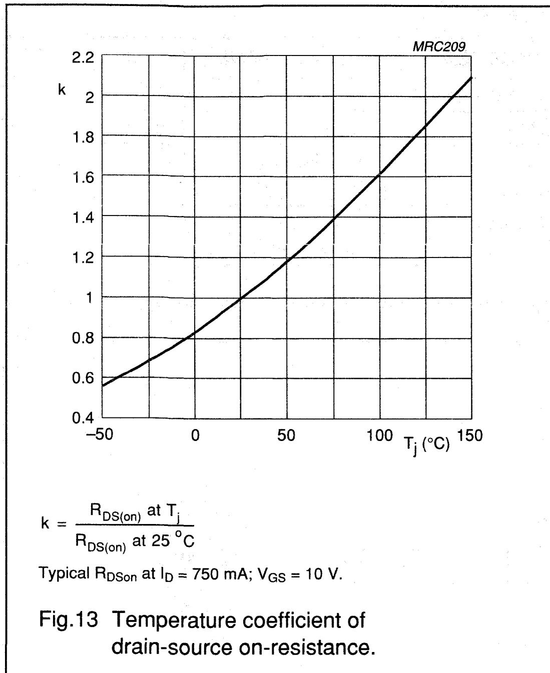


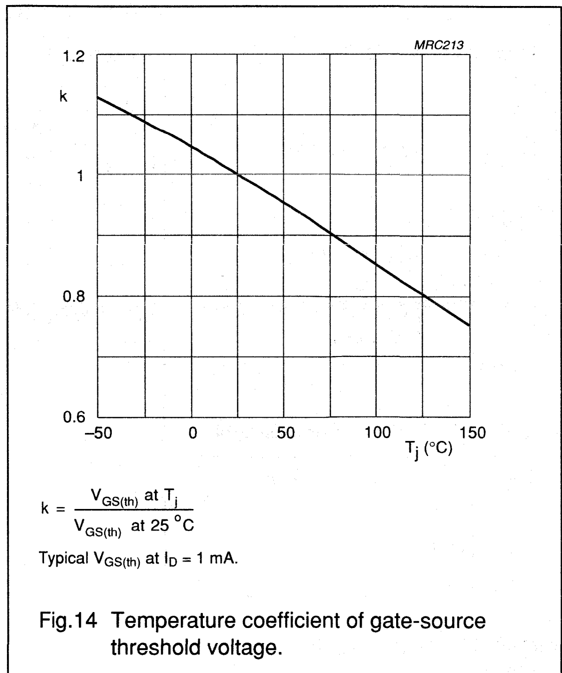
Fig.12 Transient thermal resistance from junction to ambient as a function of pulse time.



$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\,^{\circ}C}$$

Typical R_{DSon} at I_D = 750 mA; V_{GS} = 10 V.

Fig.13 Temperature coefficient of drain-source on-resistance.



$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\,^{\circ}C}$$

Typical $V_{GS(th)}$ at I_D = 1 mA.

Fig.14 Temperature coefficient of gate-source threshold voltage.

P-channel enhancement mode vertical D-MOS transistor

BSP204; BSP204A

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a TO-92 variant envelope, intended for use in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant (BSP204)

PIN	DESCRIPTION
1	gate
2	drain
3	source

PINNING - TO-92 variant (BSP204A)

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$-V_{DS}$	drain-source voltage		200	V
$-I_D$	drain current	DC value	250	mA
$R_{DS(on)}$	drain-source on-resistance	$-I_D = 200$ mA $-V_{GS} = 10$ V	15	Ω
$V_{GS(th)}$	gate-source threshold voltage	$-I_D = 1$ mA $V_{GS} = V_{DS}$	2.8	V

PIN CONFIGURATION

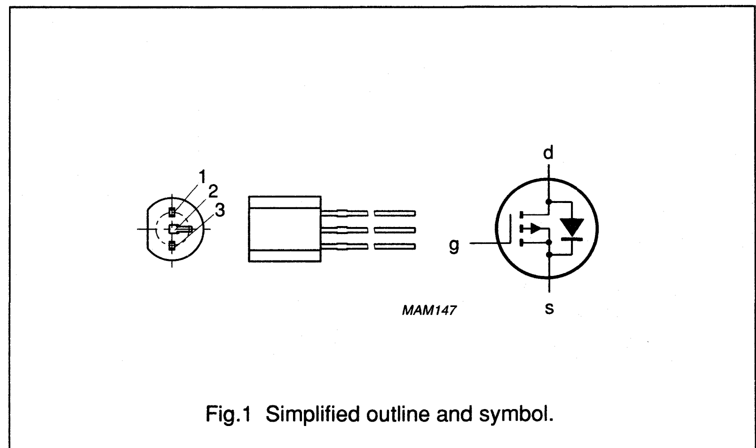


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage		–	20	V
$-I_D$	drain current	DC value	–	250	mA
$-I_{DM}$	drain current	peak value	–	600	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1	W
T_{stg}	storage temperature range		−65	150	°C
T_j	junction temperature		–	150	°C

Note

1. Device mounted on an epoxy printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm x 10 mm.

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	from junction to ambient (note 1)	125	K/W

Note

1. Device mounted on an epoxy printed-circuit board, maximum lead length 4 mm; mounting pad for the drain lead minimum 10 mm x 10 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-I_D$ = 10 μA V_{GS} = 0	200	–	–	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 160 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA $V_{GS} = V_{DS}$	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 200 mA $-V_{GS}$ = 10 V	–	10	15	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	$-I_D$ = 200 mA $-V_{DS}$ = 25 V	100	200	–	mS
C_{iss}	input capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	65	90	pF
C_{oss}	output capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	6	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	20	30	ns

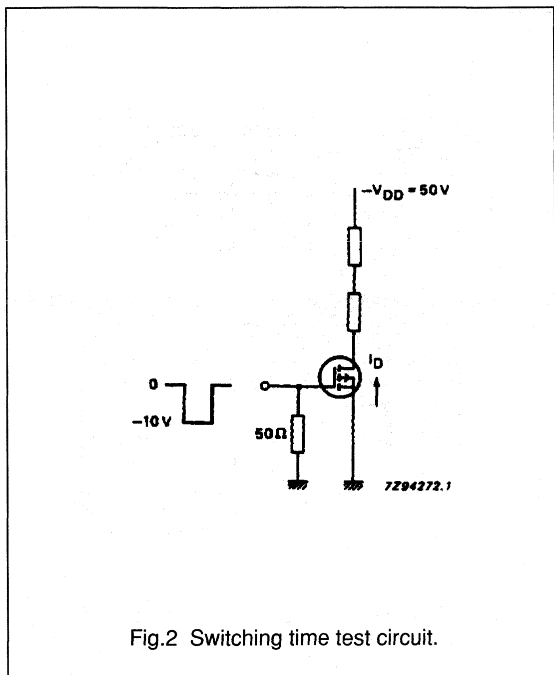


Fig.2 Switching time test circuit.

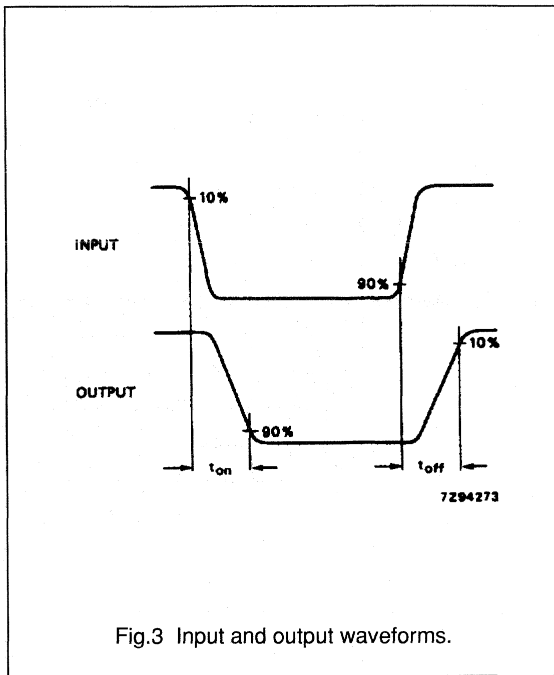


Fig.3 Input and output waveforms.

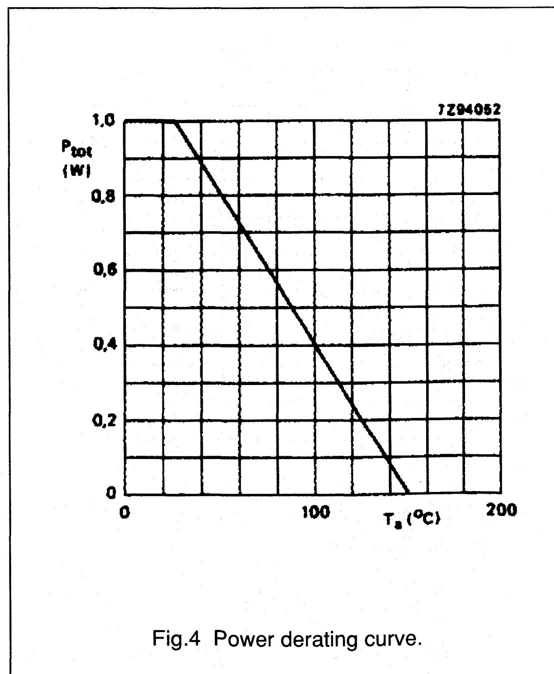


Fig.4 Power derating curve.

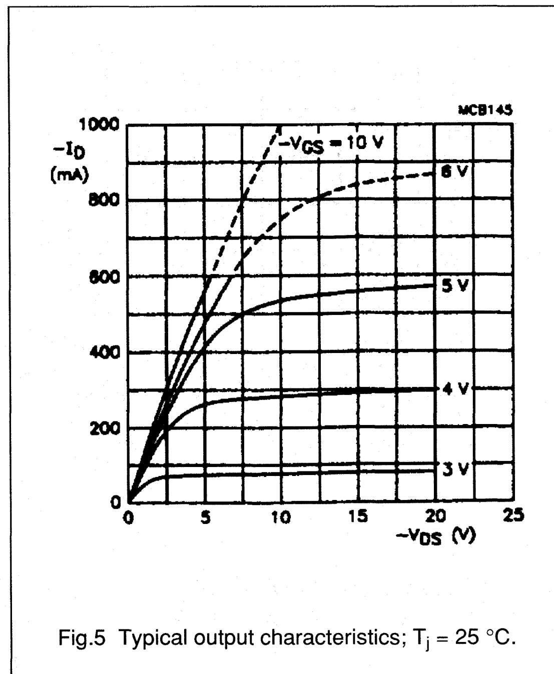


Fig.5 Typical output characteristics; T_j = 25 °C.

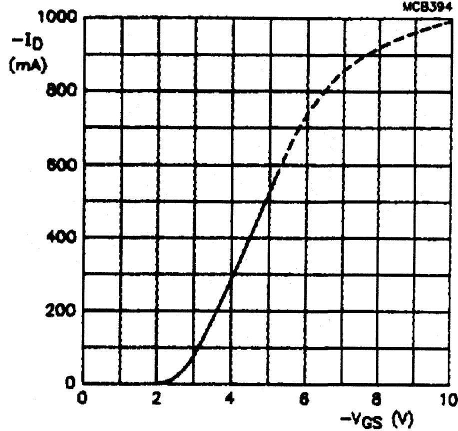


Fig.6 Typical transfer characteristic; $-V_{DS}$ = 10 V; T_j = 25 °C.

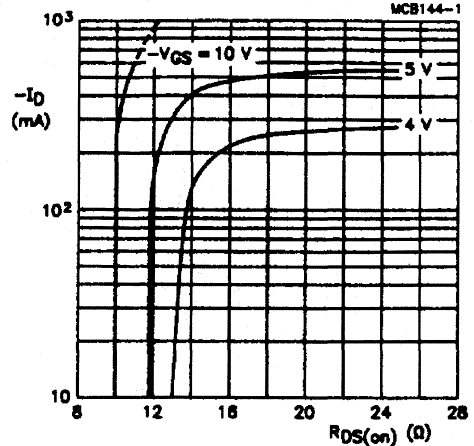


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

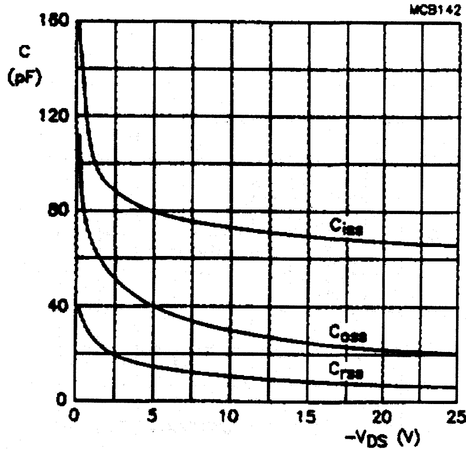


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

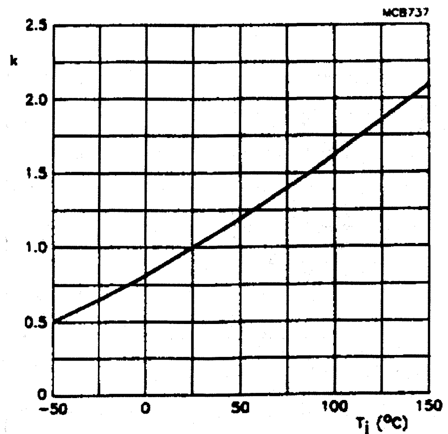


Fig.9 Temperature coefficient of drain-source on-resistance;

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C};$$

typical $R_{DS(on)}$ at –200 mA/–10 V.

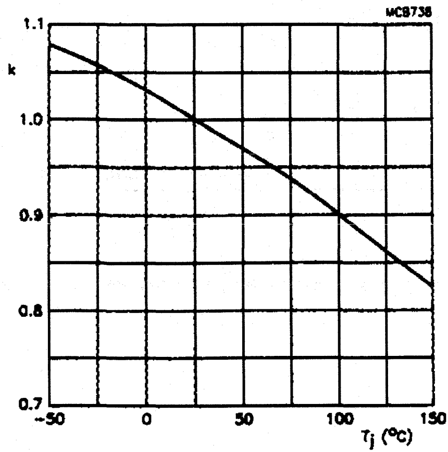


Fig.10 Temperature coefficient of gate-source threshold voltage;

$$k = \frac{-V_{GS(th)} \text{ at } T_j}{-V_{GS(th)} \text{ at } 25\ °C};$$

typical $-V_{GS(th)}$ at −1 mA.

P-channel enhancement mode vertical D-MOS transistor

BSP205

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line-transformer drivers.

FEATURES

- Very low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

PINNING - SOT223

1 = gate
2 = drain
3 = source
4 = drain

PIN CONFIGURATION

Marking code

BSP205

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60	V
Drain current (DC)	$-I_D$	max.	275	mA
Drain-source ON-resistance				
$-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$R_{DS(on)}$	max.	10	Ω
Gate threshold voltage	$-V_{GS(th)}$	max.	3.5	V

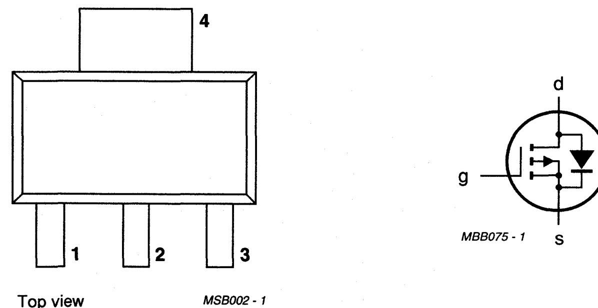


Fig.1 Simplified outline and symbol.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	275	mA
Drain current (peak)	$-I_{DM}$	max.	550	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}		−65 to 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j-a}$	=	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board 40 mm × 40 mm × 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value	Unit
Drain-source breakdown voltage $-I_D$ = 10 μA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	60	V
Drain-source leakage current $-V_{DS}$ = 48 V; V_{GS} = 0	$-I_{DSS}$	max.	1.0	μA
Gate-source leakage current ± V_{GS} = 20 V; V_{DS} = 0	$\pm I_{GSS}$	max.	100	nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	1.5 3.5	V V
Drain-source ON-resistance $-I_D$ = 200 mA ; $-V_{GS}$ = 10 V	$R_{DS(on)}$	typ. max.	7.5 10	Ω Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert Y_{fs} \rvert$	min. typ.	60 125	mS mS
Input capacitance at f = 1 MHz; $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max.	30 45	pF pF
Output capacitance at f = 1 MHz; $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max.	20 30	pF pF
Feedback capacitance at f = 1 MHz; $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max.	5 10	pF pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on}	typ. max.	3 6	ns ns
	t_{off}	typ. max.	10 15	ns ns

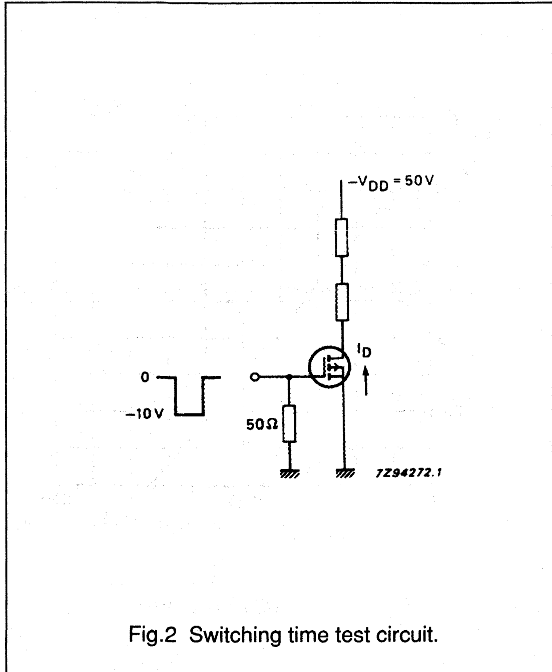


Fig.2 Switching time test circuit.

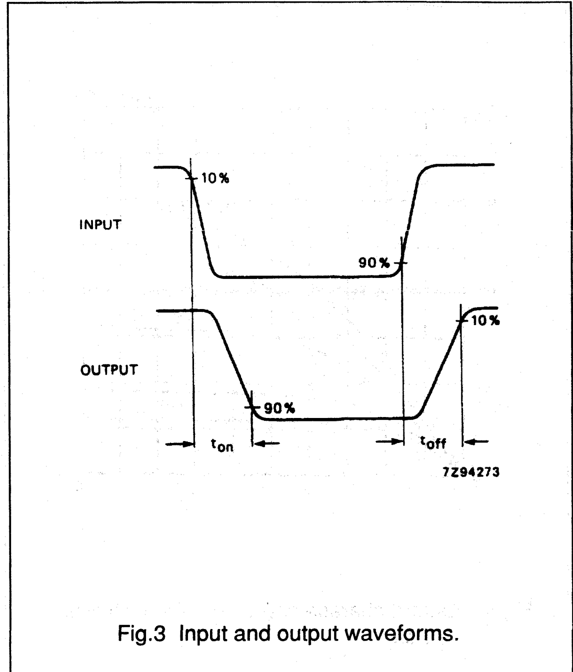


Fig.3 Input and output waveforms.

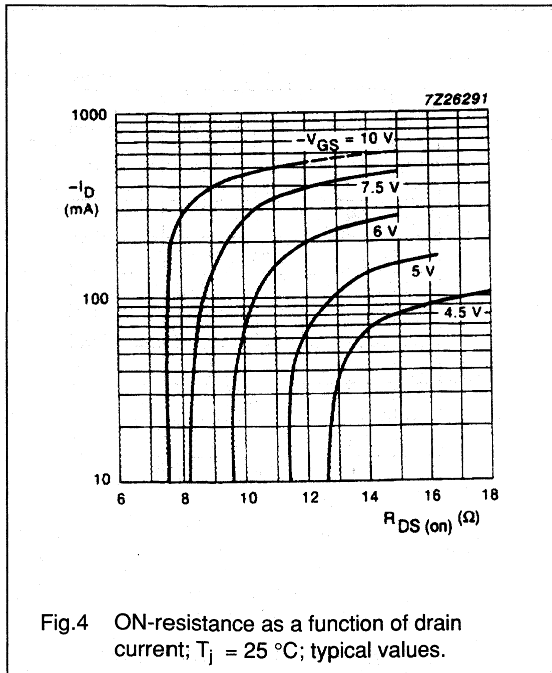


Fig.4 ON-resistance as a function of drain current; T_j = 25 °C; typical values.

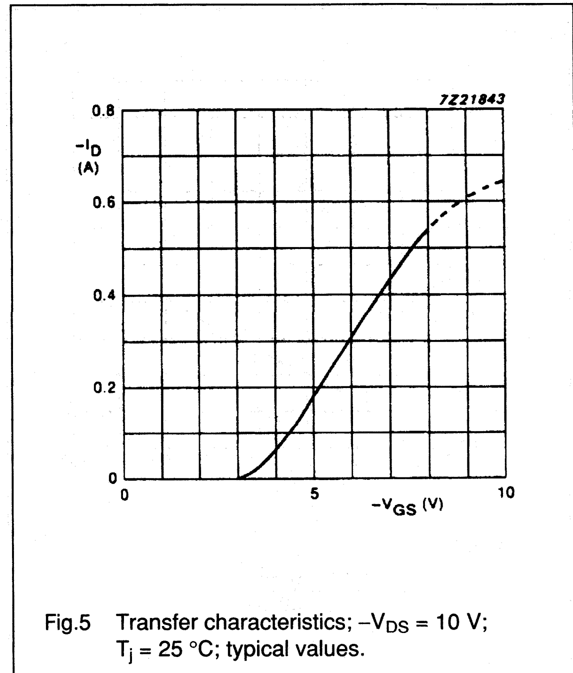


Fig.5 Transfer characteristics; $-V_{DS}$ = 10 V; T_j = 25 °C; typical values.

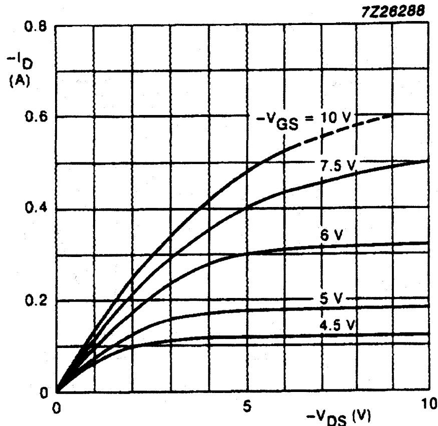


Fig.6 Output characteristics; $T_j = 25$ °C; typical values.

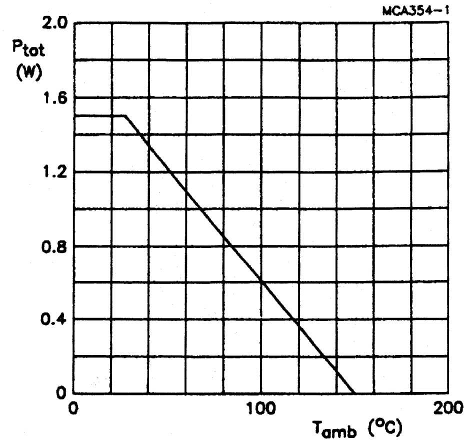


Fig.7 Power derating curve.

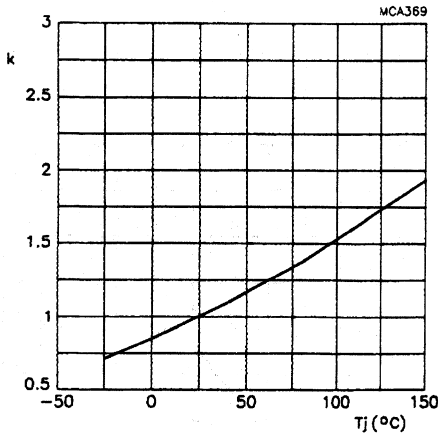


Fig.8

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C};$$

at −200 mA/−10 V; typical values.

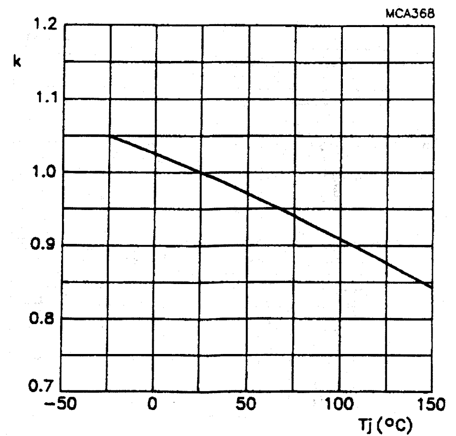


Fig.9

$$k = \frac{-V_{GS(th)} \text{ at } T_j}{-V_{GS(th)} \text{ at } 25\ °C};$$

$-V_{GS(th)}$ at −1 mA; typical values.

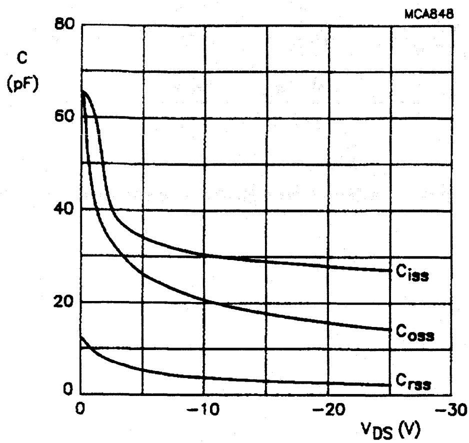


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

P-channel enhancement mode vertical D-MOS transistor

BSP206

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line-transformer drivers.

FEATURES

- Very low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60	V
Drain current (DC)	$-I_D$	max.	350	mA
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$R_{DS(on)}$	max.	6	Ω
Gate threshold voltage	$-V_{GS(th)}$	max.	3.5	V

PINNING - SOT223

1 = gate
2 = drain
3 = source
4 = drain

Marking code

BSP206

PIN CONFIGURATION

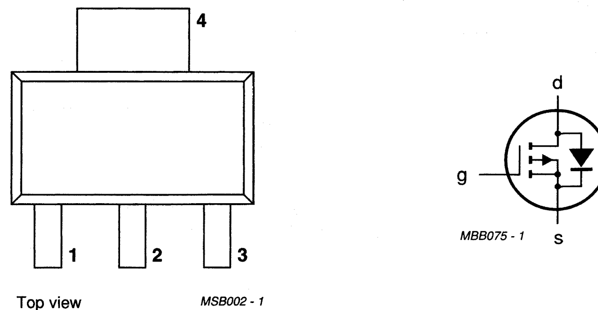


Fig.1 Simplfied outline and symbol.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Parameter	Symbol		Value	Unit
Drain-source voltage	$-V_{DS}$	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	350	mA
Drain current (peak)	$-I_{DM}$	max.	700	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1.5	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

Parameter	Symbol		Value	Unit
From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board 40 mm × 40 mm × 1.5 mm; mounting pad for the drain lead min. 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value	Unit
Drain-source breakdown voltage $-I_D$ = 10 µA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	60	V
Drain-source leakage current $-V_{DS}$ = 48 V; V_{GS} = 0	$-I_{DSS}$	max.	1.0	µA
Gate-source leakage current $\pm V_{GS}$ = 20 V; V_{DS} = 0	$\pm I_{GSS}$	max.	100	nA
Gate threshold voltage $-I_D$ = 1 mA; $V_{DS} = V_{GS}$	$-V_{GS(th)}$	min. max.	1.5 3.5	V V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$R_{DS(on)}$	typ. max.	4.5 6	Ω Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert Y_{fs} \rvert$	min. typ.	100 200	mS mS
Input capacitance at f = 1 MHz; $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max.	55 70	pF pF
Output capacitance at f = 1 MHz; $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max.	30 45	pF pF
Feedback capacitance at f = 1 MHz; $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max.	8 12	pF pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on}	typ. max.	4 8	ns ns
	t_{off}	typ. max.	15 25	ns ns

P-channel enhancement mode vertical D-MOS transistor

BSP206

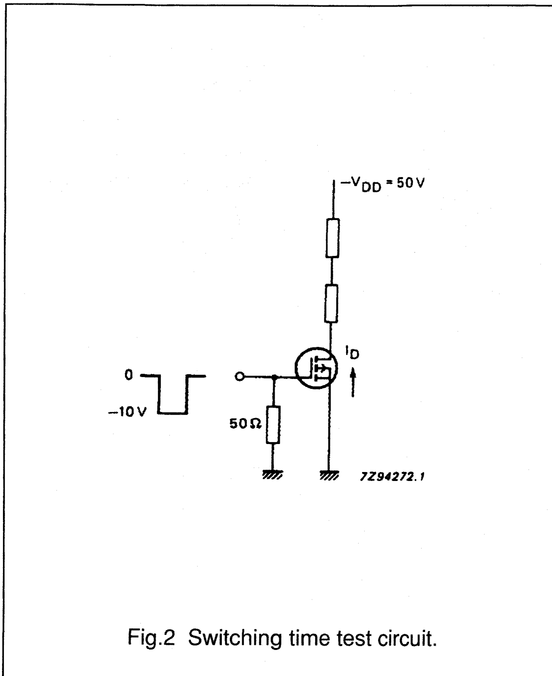


Fig.2 Switching time test circuit.

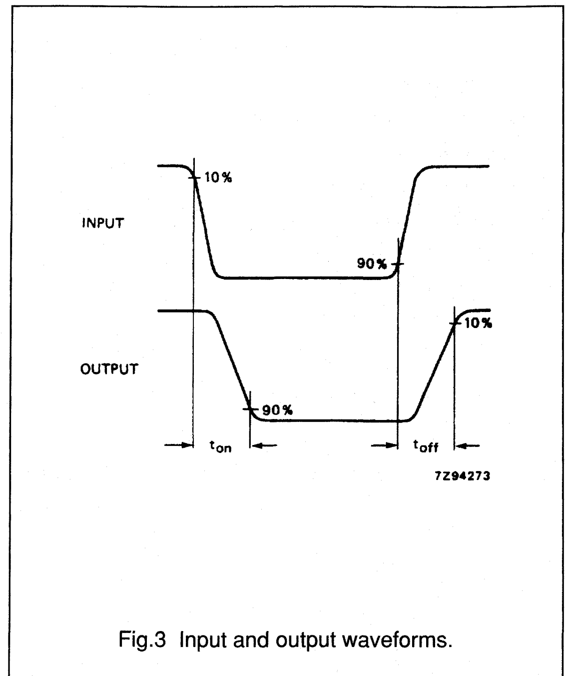


Fig.3 Input and output waveforms.

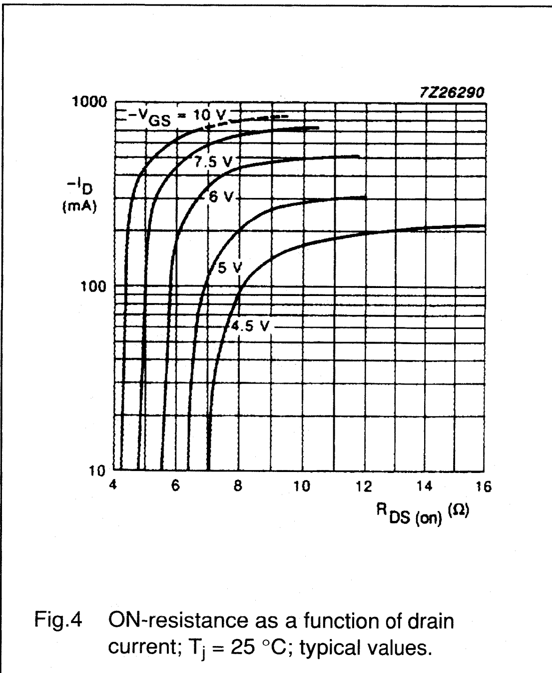


Fig.4 ON-resistance as a function of drain current; T_j = 25 °C; typical values.

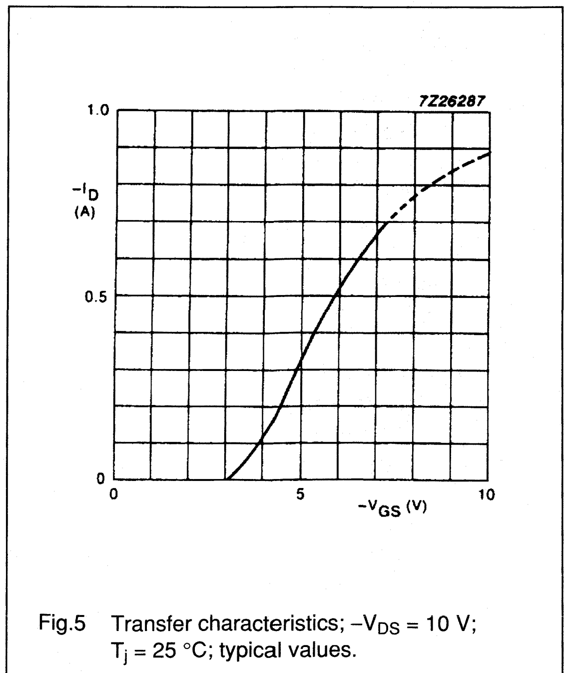


Fig.5 Transfer characteristics; $-V_{DS}$ = 10 V; T_j = 25 °C; typical values.

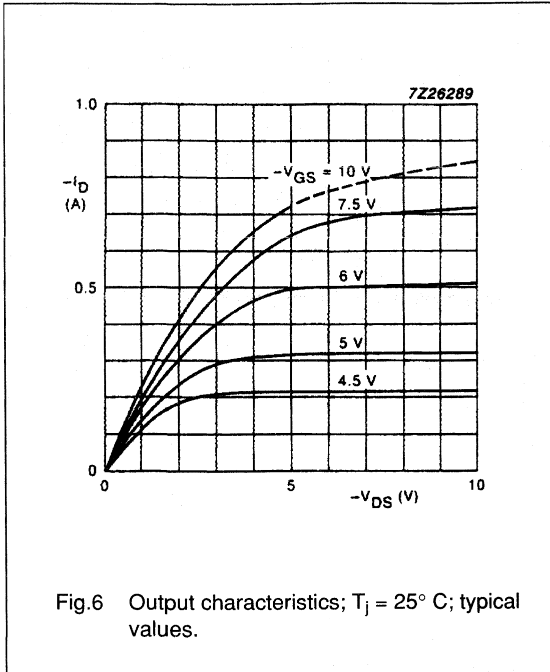


Fig.6 Output characteristics; T_j = 25° C; typical values.

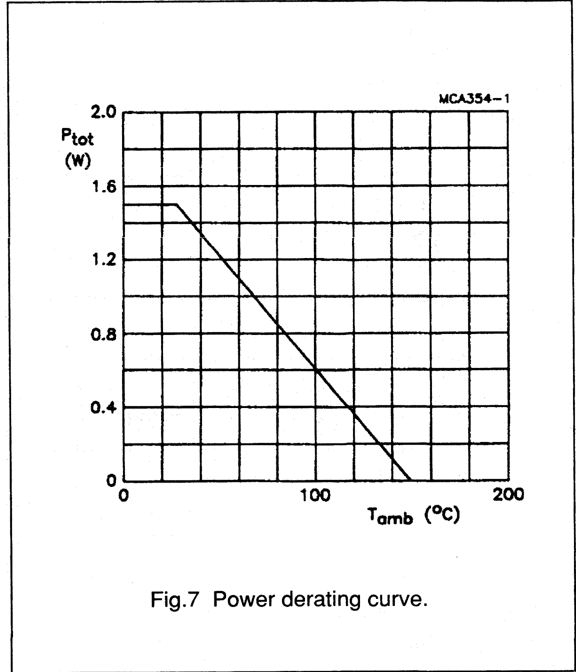


Fig.7 Power derating curve.

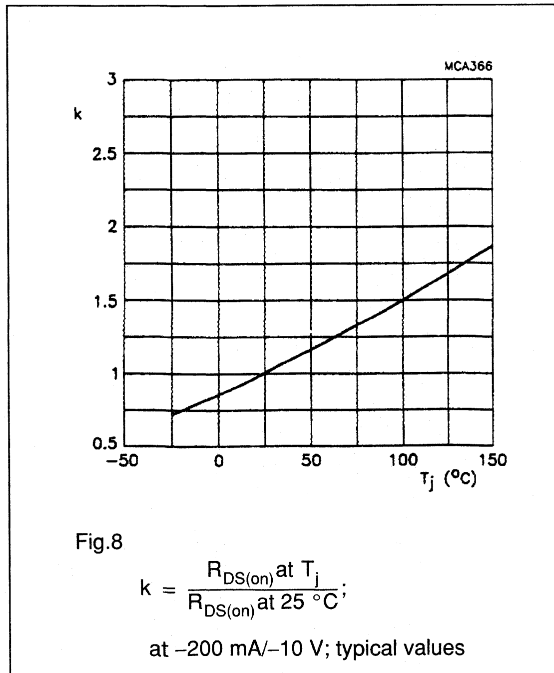


Fig.8

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C};$$

at −200 mA/−10 V; typical values

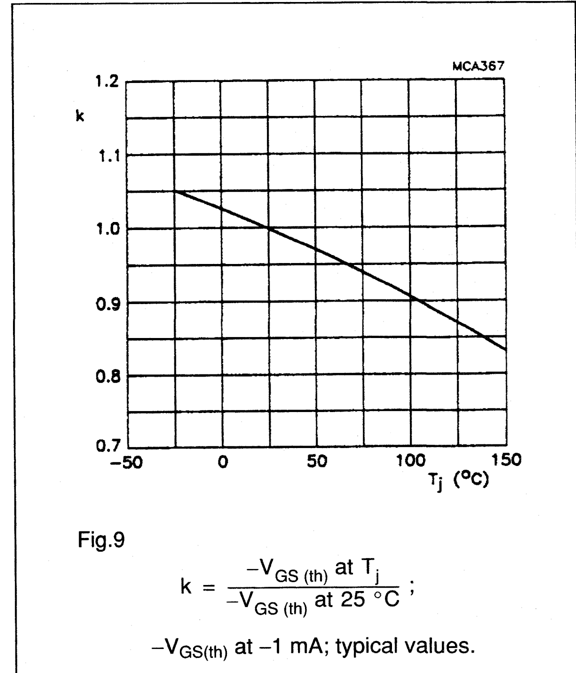


Fig.9

$$k = \frac{-V_{GS\,(th)} \text{ at } T_j}{-V_{GS\,(th)} \text{ at } 25\ °C};$$

$-V_{GS(th)}$ at −1 mA; typical values.

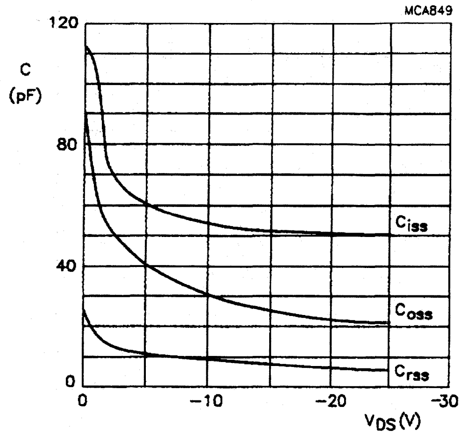


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

P-channel enhancement mode vertical D-MOS transistor

BSP220

FEATURES

- Low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and intended for use in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$-V_{DS}$	drain-source voltage		200	V
$-I_D$	drain current	DC value	225	mA
$R_{DS(on)}$	drain-source on-resistance	$-I_D = 200$ mA $-V_{GS} = 10$ V	12	Ω
$-V_{GS(th)}$	gate-source threshold voltage		2.8	V

PIN CONFIGURATION

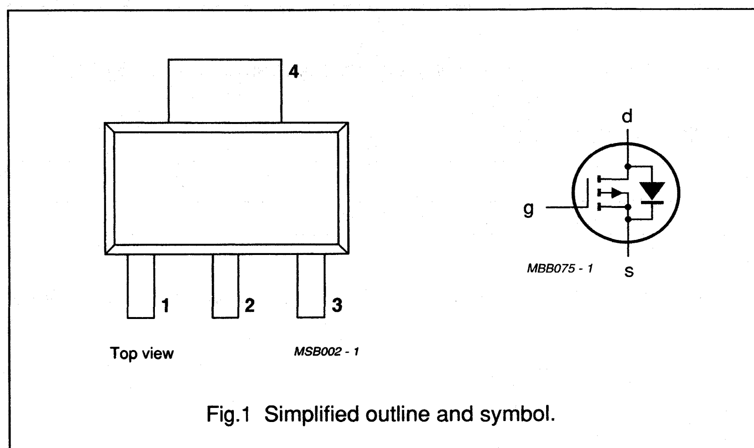


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$-I_D$	drain current	DC value	–	225	mA
$-I_{DM}$	drain current	peak value	–	600	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Note

1. Device mounted on an epoxy printed-circuit board 40 x 40 x 1.5 mm; mounting pad for the drain lead minimum 6 cm^2.

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board 40 x 40 x 1.5 mm; mounting pad for the drain lead minimum 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-I_D$ = 10 μA V_{GS} = 0	200	–	–	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 160 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA V_{GS} = V_{DS}	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 200 mA $-V_{GS}$ = 10 V	–	10	12	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	$-I_D$ = 200 mA $-V_{DS}$ = 25 V	100	200	–	mS
C_{iss}	input capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	–	65	90	pF
C_{oss}	output capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	$-V_{DS}$ = 25 V V_{GS} = 0 f = 1 MHz	–	6	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	5	20	ns
t_{off}	turn-off time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	20	30	ns

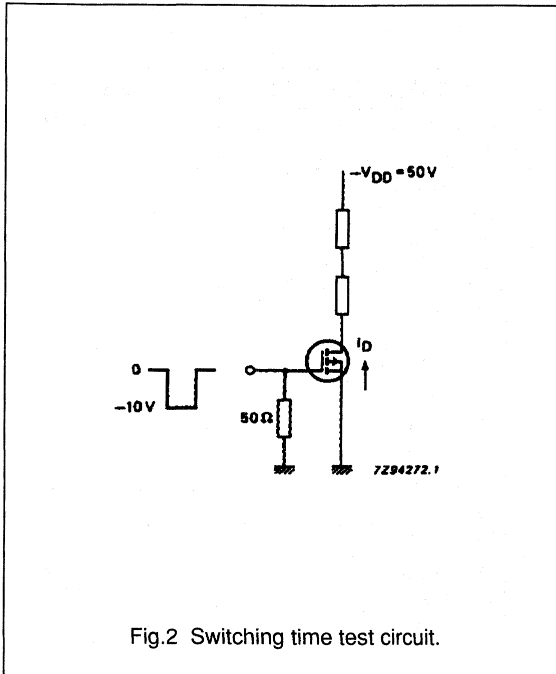


Fig.2 Switching time test circuit.

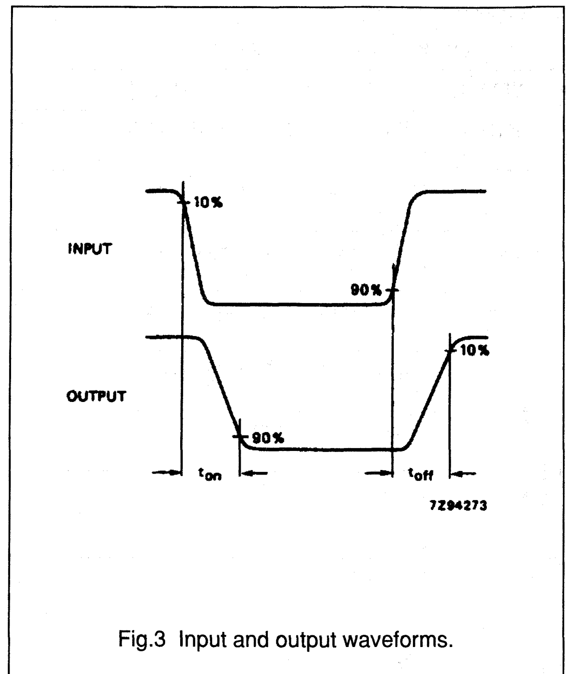


Fig.3 Input and output waveforms.

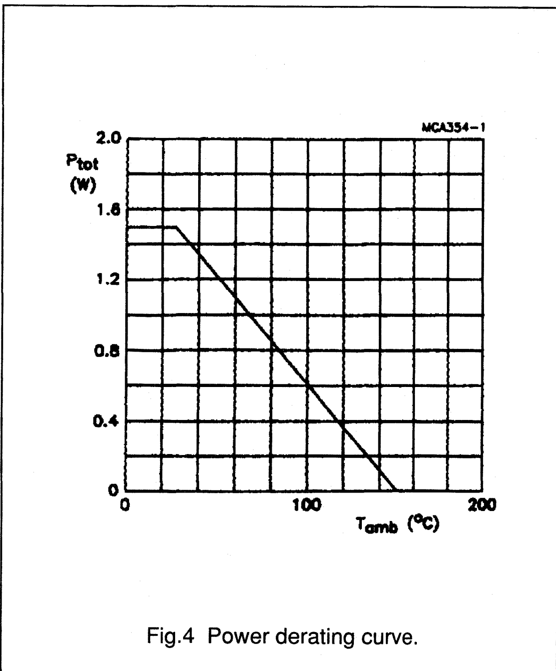


Fig.4 Power derating curve.

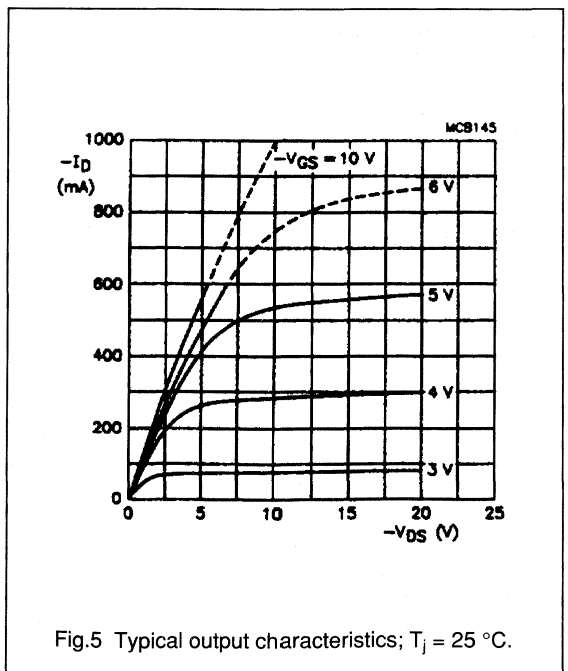


Fig.5 Typical output characteristics; T_j = 25 °C.

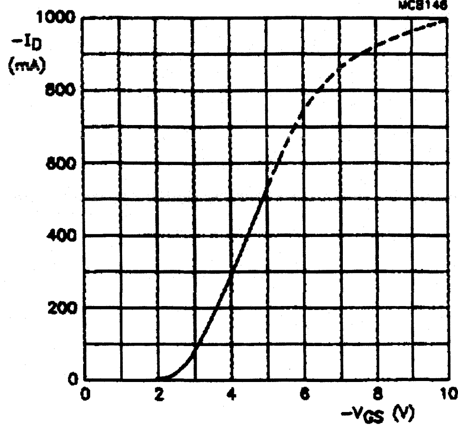


Fig.6 Typical transfer characteristic; $-V_{DS}$ = 10 V; T_j = 25 °C.

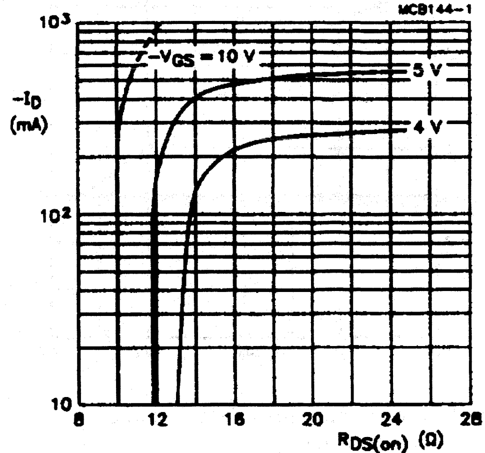


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

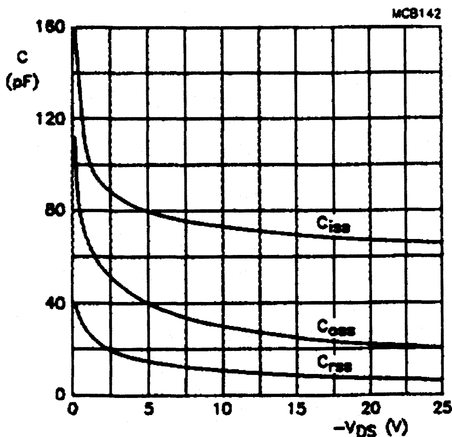


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

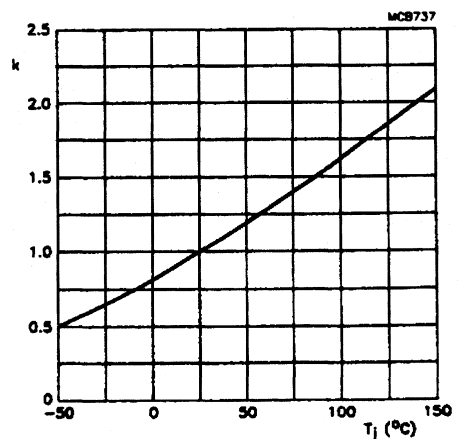


Fig.9 Temperature coefficient of drain-source on-resistance;

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C};$$

typical $R_{DS(on)}$ at −200 mA/−10 V.

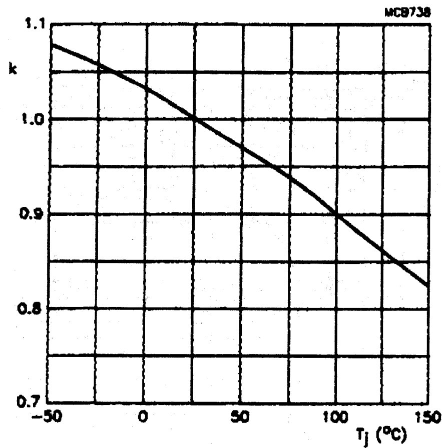


Fig.10 Temperature coefficient of gate-source threshold voltage;

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C};$$

typical $-V_{GS(th)}$ at -1 mA.

P-channel enhancement mode vertical D-MOS transistor

BSP225

FEATURES

- Low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope, intended for use in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$-V_{DS}$	drain-source voltage		250	V
$-I_D$	drain current	DC value	225	mA
$R_{DS(on)}$	drain-source on-resistance	$-I_D = 200$ mA $-V_{GS} = 10$ V	15	Ω
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D = 1$ mA $V_{GS} = V_{DS}$	2.8	V

PIN CONFIGURATION

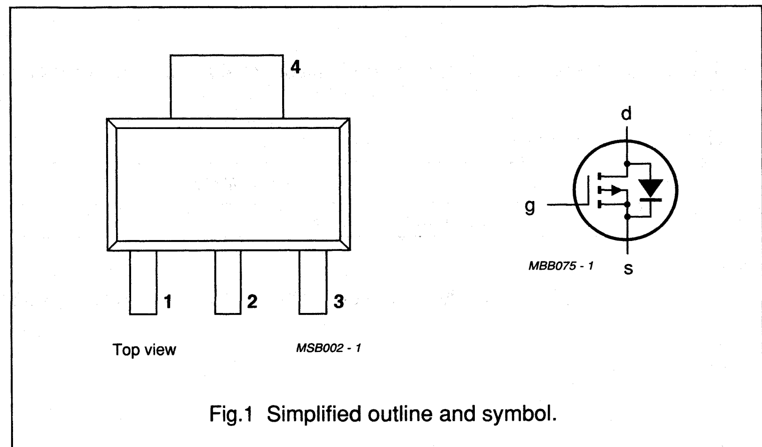


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	250	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$-I_D$	drain current	DC value	–	225	mA
$-I_{DM}$	drain current	peak value	–	600	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Note

1. Device mounted on an epoxy printed-circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain lead minimum 6 cm^2.

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	83.3	K/W

Note

1. Device mounted on an epoxy printed-circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain lead minimum 6 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-I_D$ = 10 μA V_{GS} = 0	250	–	–	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 200 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	V_{DS} = 0 $\pm V_{GS}$ = 20 V	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D$ = 1 mA $V_{GS} = V_{DS}$	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-I_D$ = 200 mA $-V_{GS}$ = 10 V	–	10	15	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	$-I_D$ = 200 mA $-V_{DS}$ = 25 V	100	200	–	mS
C_{iss}	input capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	65	90	pF
C_{oss}	output capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	20	30	pF
C_{rss}	feedback capacitance	$-V_{DS}$ = 25 V $-V_{GS}$ = 0 f = 1 MHz	–	6	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	5	10	ns
t_{off}	turn-off time	$-I_D$ = 250 mA $-V_{DD}$ = 50 V $-V_{GS}$ = 0 to 10 V	–	20	30	ns

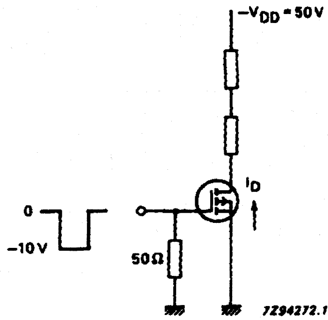


Fig.2 Switching time test circuit.

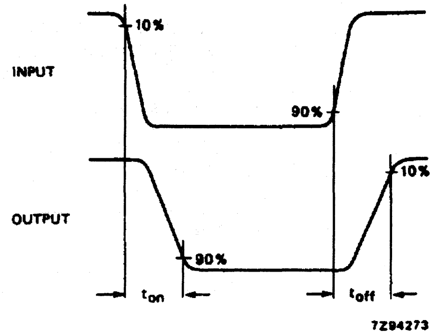


Fig.3 Input and output waveforms.

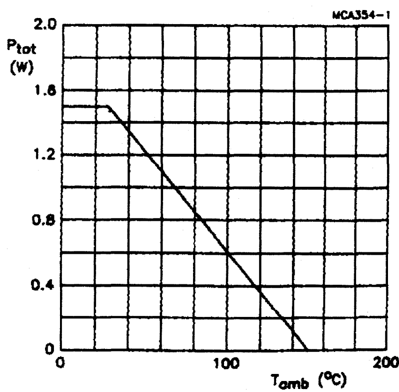


Fig.4 Power derating curve.

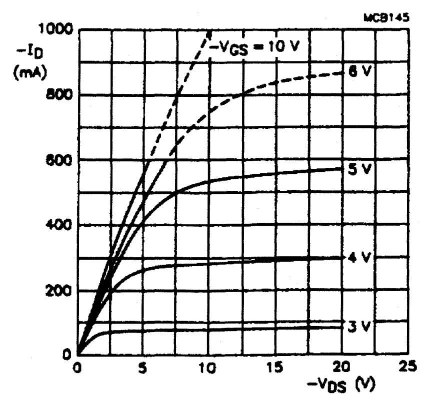


Fig.5 Typical output characteristics; T_j = 25 °C.

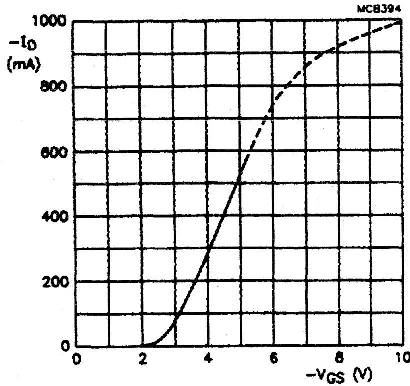


Fig.6 Typical transfer characteristic; $-V_{DS}$ = 10 V; T_j = 25 °C.

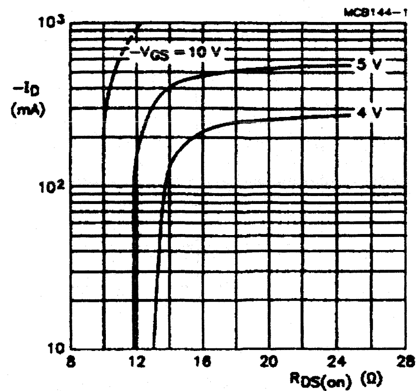


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C; $R_{DS(on)} = f(I_D)$.

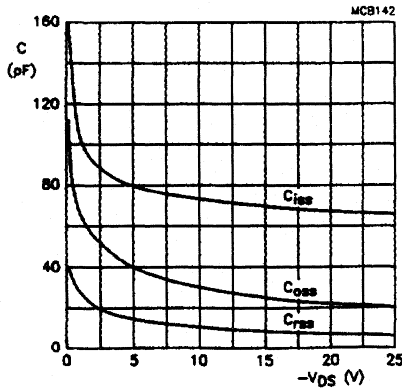


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

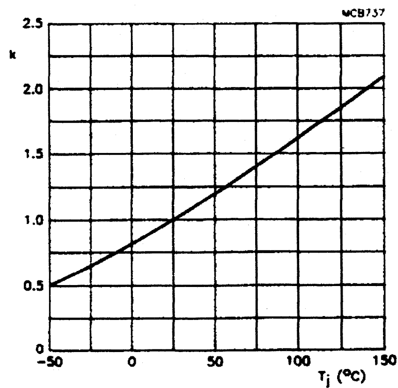


Fig.9 Temperature coefficient of drain-source on-resistance;

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C};$$

typical $R_{DS(on)}$ at −200 mA/−10 V.

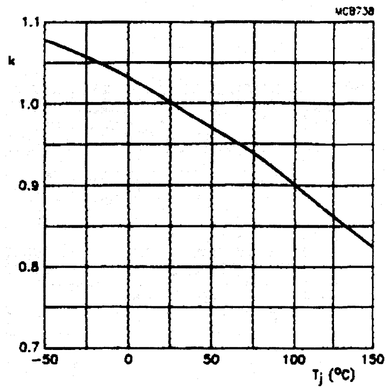


Fig.10 Temperature coefficient of gate-source threshold voltage;

$$k = \frac{-V_{GS(th)} \text{ at } T_j}{-V_{GS(th)} \text{ at } 25\ ^\circ C};$$

typical $V_{GS(th)}$ at −1 mA.

P-channel enhancement mode vertical D-MOS transistor

BSP230

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Line current interruptor in telephone sets
- Relay, high speed and line transformer drivers.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a SOT223 plastic SMD package.

PINNING - SOT223

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source
4	d	drain

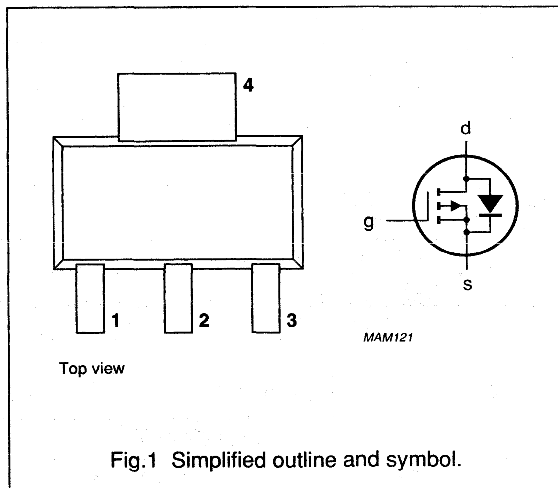


Fig.1 Simplified outline and symbol.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–300	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	$I_D = -1$ mA; $V_{DS} = V_{GS}$	–1.7	–2.55	V
I_D	drain current (DC)		–	–210	mA
R_{DSon}	drain-source on-state resistance	$I_D = -170$ mA; $V_{GS} = -10$ V	–	17	Ω
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	1.5	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–300	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	–210	mA
I_{DM}	peak drain current		–	–0.75	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	1.5	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	83.3	K/W

Note to the Limiting values and Thermal characteristics

1. Device mounted on an epoxy printed-circuit board, 40 × 40 × 1.5 mm; mounting pad for drain lead minimum 6 cm^2.

CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = -10$ μA	–300	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = V_{GS}$; $I_D = -1$ mA	–1.7	–	–2.55	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = -240$ V	–	–	–100	nA
I_{GSS}	gate leakage current	$V_{GS} = \pm 20$ V; $V_{DS} = 0$	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -10$ V; $I_D = -170$ mA	–	–	17	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	$V_{DS} = -25$ V; $I_D = -170$ mA	100	–	–	mS
C_{iss}	input capacitance	$V_{GS} = 0$; $V_{DS} = -25$ V; f = 1 MHz	–	60	90	pF
C_{oss}	output capacitance	$V_{GS} = 0$; $V_{DS} = -25$ V; f = 1 MHz	–	15	30	pF
C_{rss}	reverse transfer capacitance	$V_{GS} = 0$; $V_{DS} = -25$ V; f = 1 MHz	–	5	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$V_{GS} = 0$ to -10 V; $V_{DD} = -50$ V; $I_D = -250$ mA	–	5	10	ns
t_{off}	turn-off time	$V_{GS} = -10$ to 0 V; $V_{DD} = -50$ V; $I_D = -250$ mA	–	15	30	ns

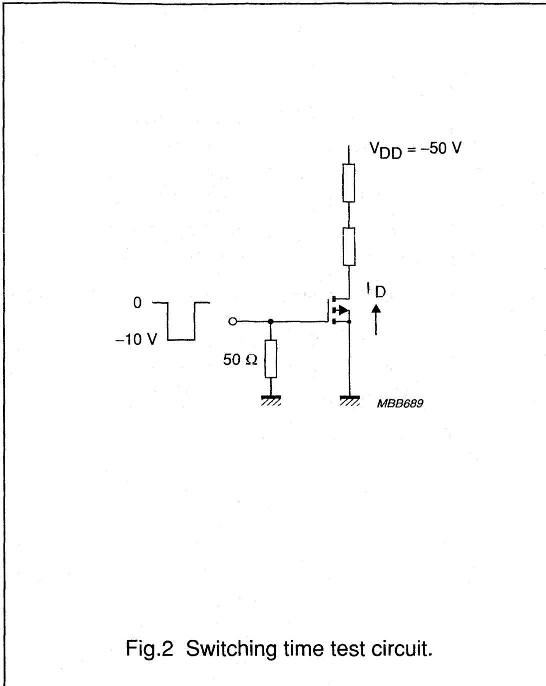


Fig.2 Switching time test circuit.

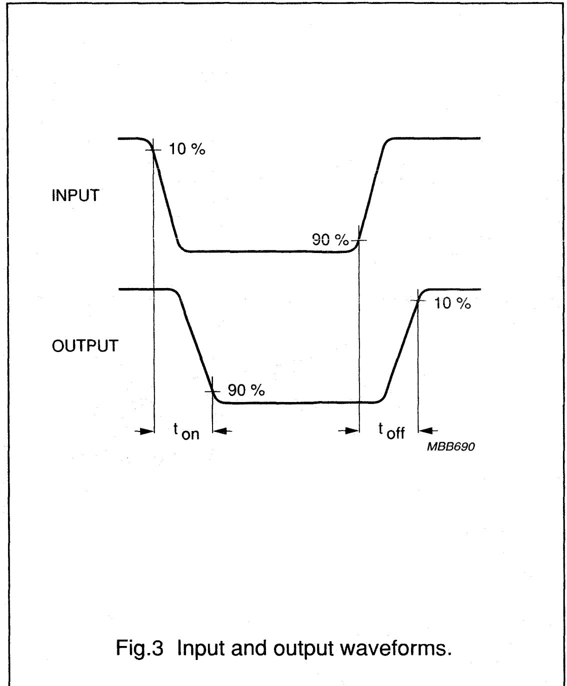


Fig.3 Input and output waveforms.

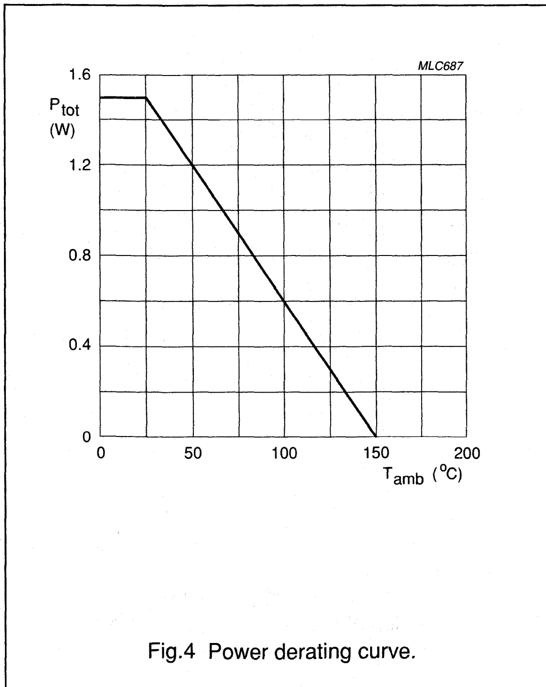
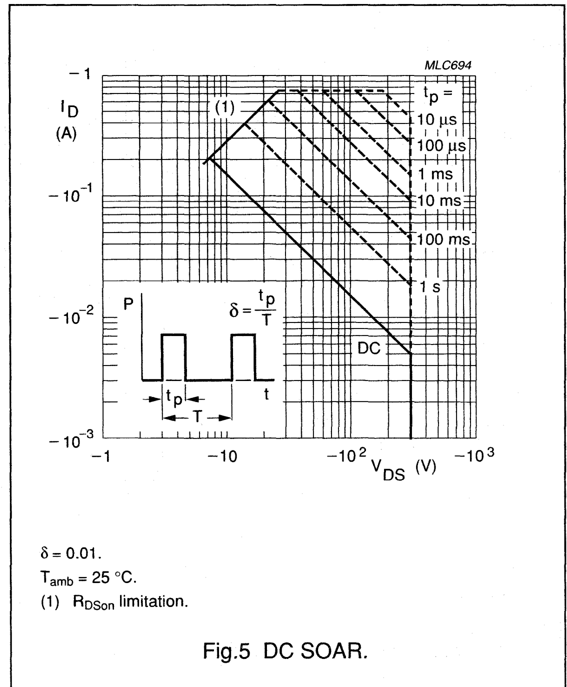


Fig.4 Power derating curve.

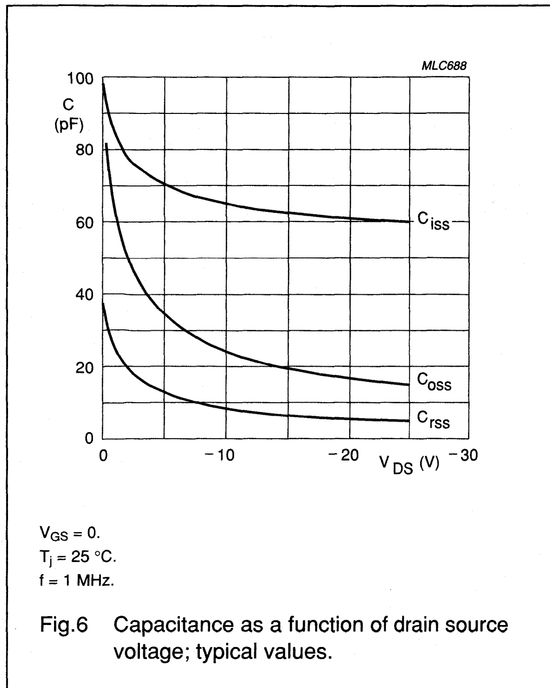


$\delta = 0.01$.

$T_{amb} = 25$ °C.

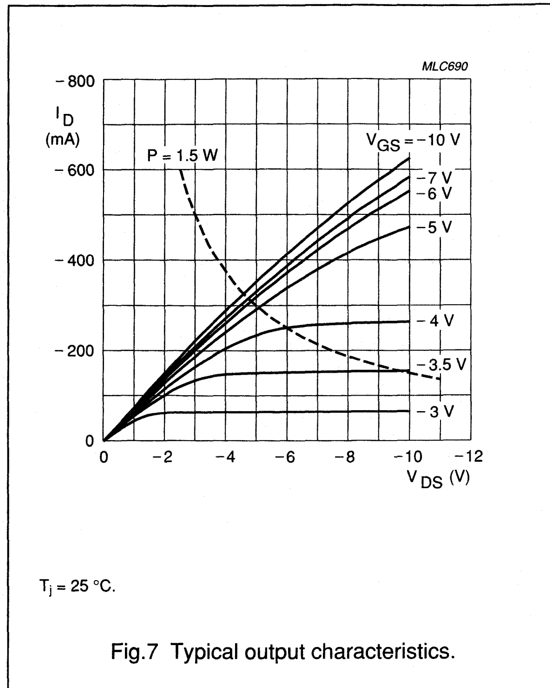
(1) R_{DSon} limitation.

Fig.5 DC SOAR.



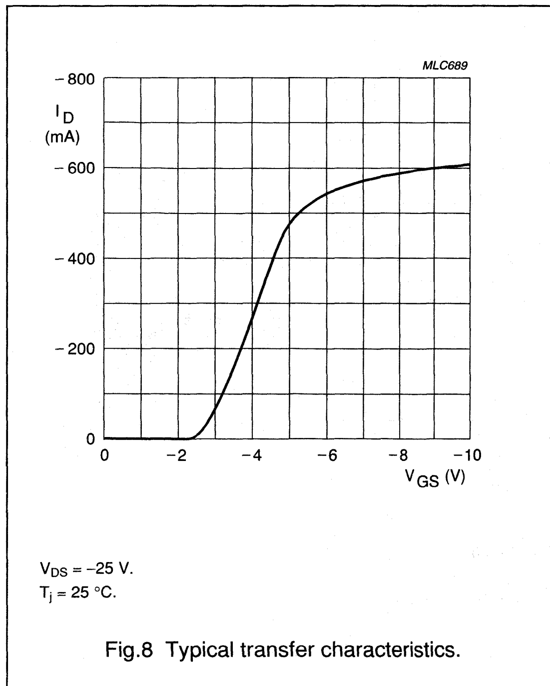
V_{GS} = 0.
T_j = 25 °C.
f = 1 MHz.

Fig.6 Capacitance as a function of drain source voltage; typical values.



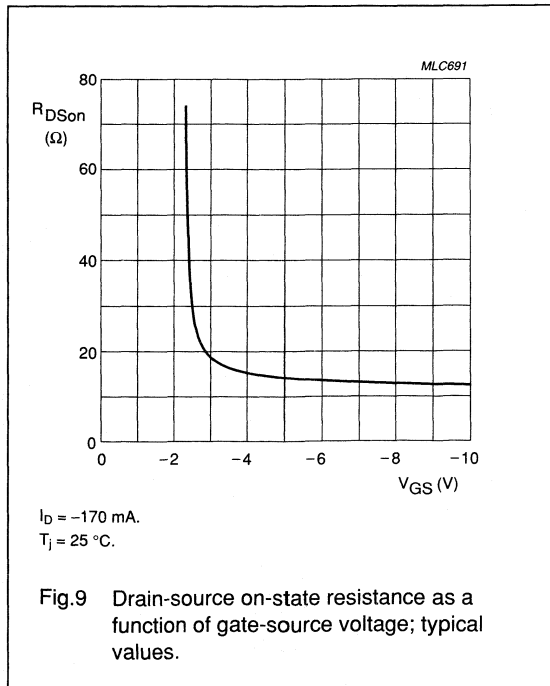
T_j = 25 °C.

Fig.7 Typical output characteristics.



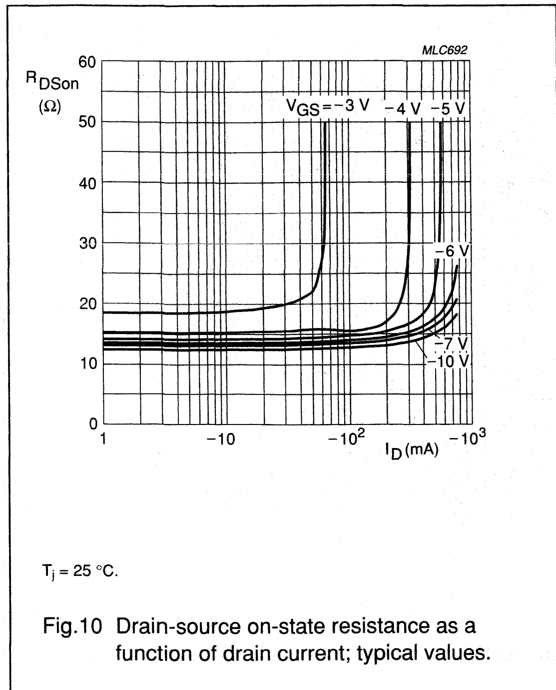
V_{DS} = −25 V.
T_j = 25 °C.

Fig.8 Typical transfer characteristics.



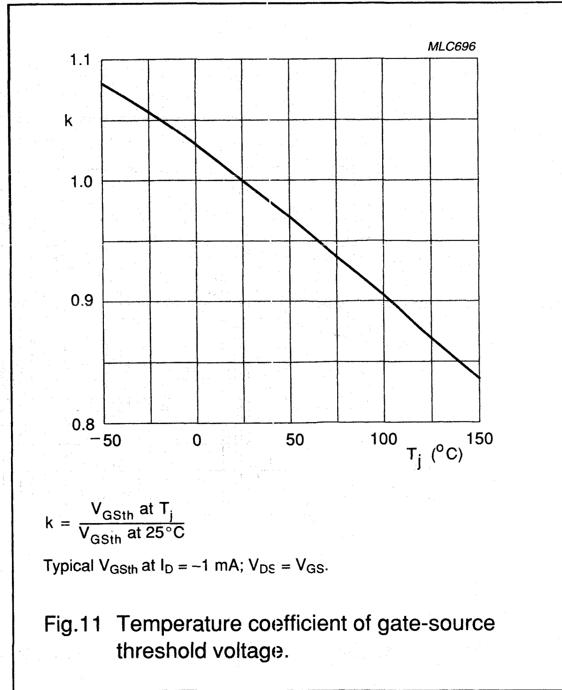
I_D = −170 mA.
T_j = 25 °C.

Fig.9 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$T_j = 25$ °C.

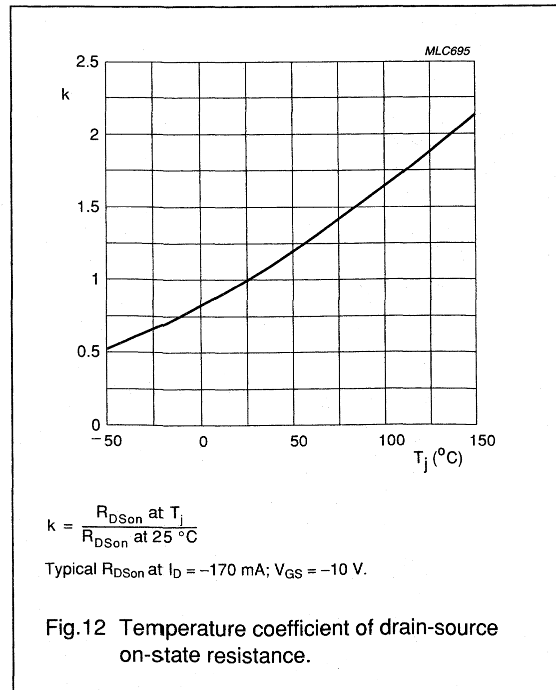
Fig.10 Drain-source on-state resistance as a function of drain current; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25\,°C}$$

Typical V_{GSth} at $I_D = -1$ mA; $V_{DS} = V_{GS}$.

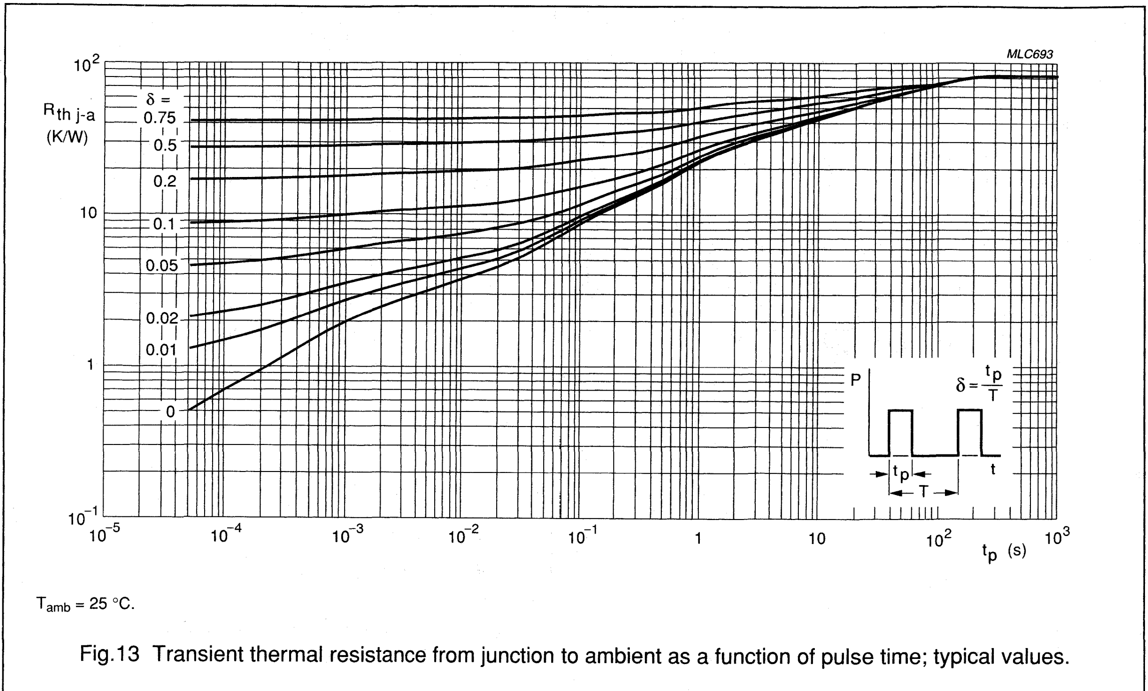
Fig.11 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\,°C}$$

Typical R_{DSon} at $I_D = -170$ mA; $V_{GS} = -10$ V.

Fig.12 Temperature coefficient of drain-source on-state resistance.



T_{amb} = 25 °C.

Fig.13 Transient thermal resistance from junction to ambient as a function of pulse time; typical values.

P-channel enhancement mode vertical D-MOS transistor

BSP250

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Low-loss motor and actuator drivers
- Power switching.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a SOT223 plastic SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT223

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source
4	d	drain

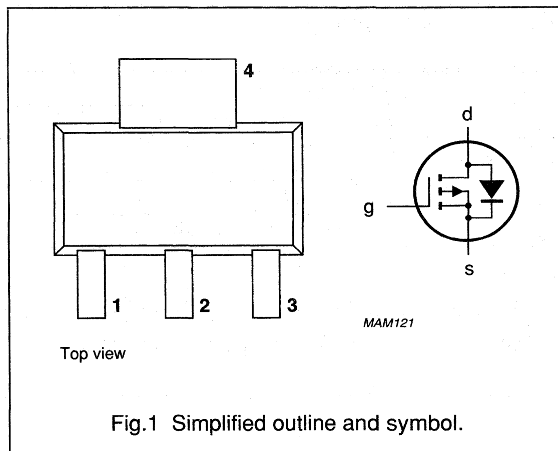


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	I_S = –1.25 A	–	–1.6	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = –1 mA; V_{DS} = V_{GS}	–1	–2.8	V
I_D	drain current (DC)		–	–3	A
R_{DSon}	drain-source on-state resistance	I_D = –1 A; V_{GS} = –10 V	–	0.25	Ω
P_{tot}	total power dissipation	T_s = 100 °C	–	5	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)	$T_s \leq 100$ °C	–	–3	A
I_{DM}	peak drain current	note 1	–	–12	A
P_{tot}	total power dissipation	$T_s = 100$ °C	–	5	W
		$T_{amb} = 25$ °C; note 2	–	1.65	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C
Source-drain diode					
I_S	source current (DC)	$T_s \leq 100$ °C	–	–1.5	A
I_{SM}	peak pulsed source current	note 1	–	–6	A

Notes

1. Pulse width and duty cycle limited by maximum junction temperature.
2. Device mounted on an epoxy printed-circuit board, 40 × 40 × 1.5 mm; mounting pad for drain lead minimum 6 cm^2.

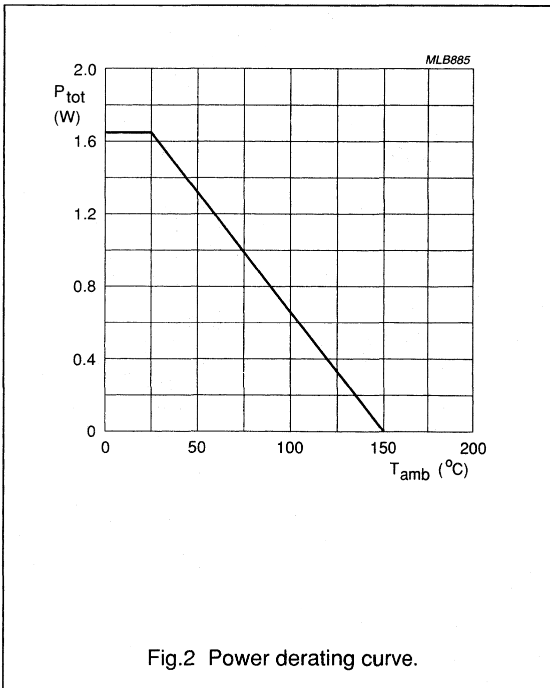
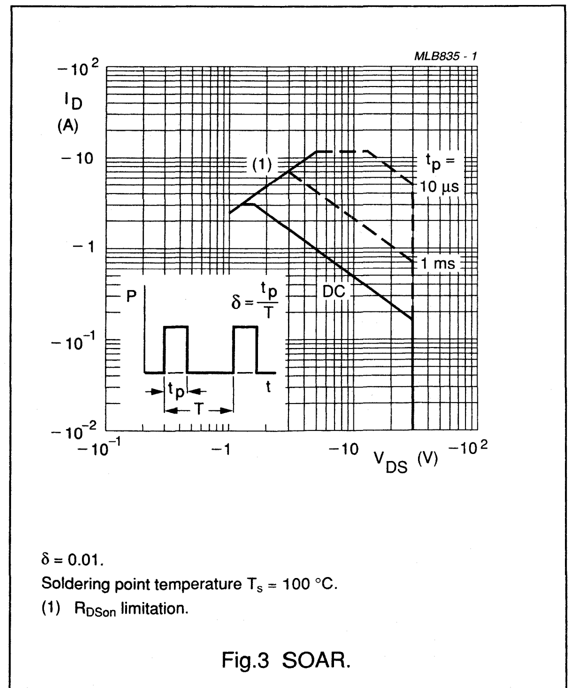


Fig.2 Power derating curve.



δ = 0.01.
Soldering point temperature T_s = 100 °C.
(1) R_{DSon} limitation.

Fig.3 SOAR.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	75	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point		10	K/W

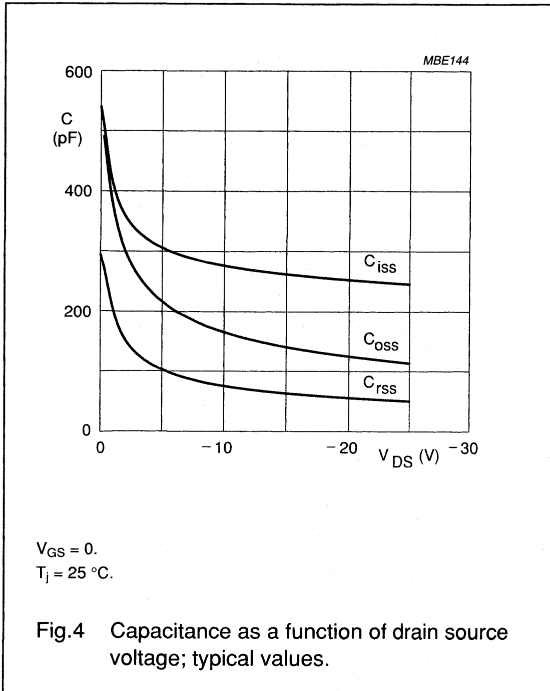
Note

1. Device mounted on an epoxy printed-circuit board, 40 × 40 × 1.5 mm; mounting pad for drain lead minimum 6 cm^2.

CHARACTERISTICS

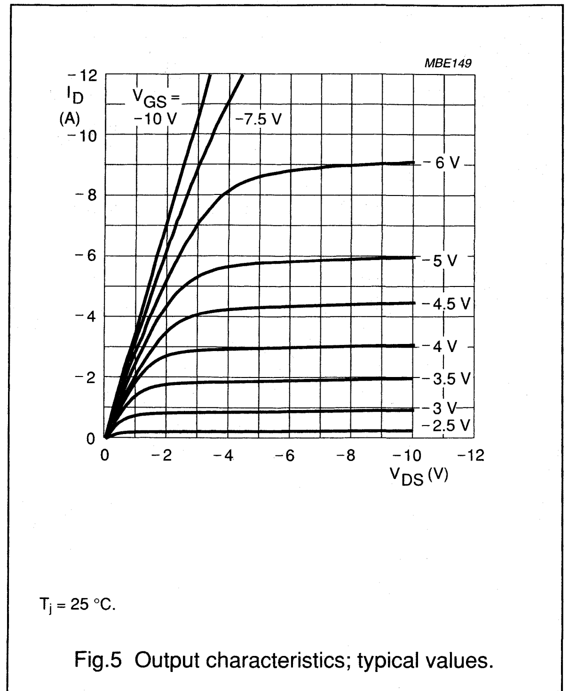
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−1	–	−2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −24 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
I_{Don}	on-state drain current	V_{GS} = −10 V; V_{DS} = −1 V	−3	–	–	A
		V_{GS} = −4.5 V; V_{DS} = −5 V	−1	–	–	A
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −0.5 A	–	0.33	0.4	Ω
		V_{GS} = −10 V; I_D = −1 A	–	0.22	0.25	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = −20 V; I_D = −1 A	1	2	–	S
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	250	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	140	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	–	50	–	pF
Q_G	total gate charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −2.3 A	–	10	25	nC
Q_{GS}	gate-source charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −2.3 A	–	1	–	nC
Q_{GD}	gate-drain charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −2.3 A	–	3	–	nC
Switching times						
t_{on}	turn-on time	V_{GS} = 0 to −10 V; V_{DD} = −20 V; I_D = −1 A; R_L = 20 Ω	–	20	80	ns
t_{off}	turn-off time	V_{GS} = −10 to 0 V; V_{DD} = −20 V; I_D = −1 A; R_L = 20 Ω	–	50	140	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = −1.25 A	–	–	−1.6	V
t_{rr}	reverse recovery time	I_S = −1.25 A; di/dt = 100 A/μs	–	150	200	ns



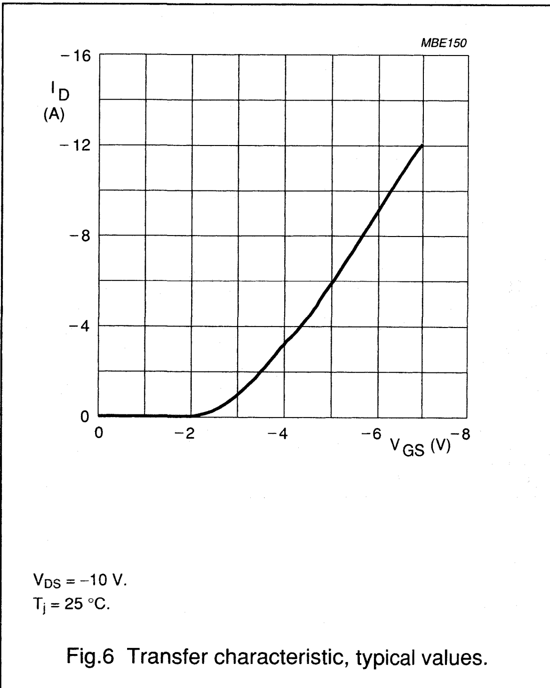
$V_{GS} = 0$.
$T_j = 25$ °C.

Fig.4 Capacitance as a function of drain source voltage; typical values.



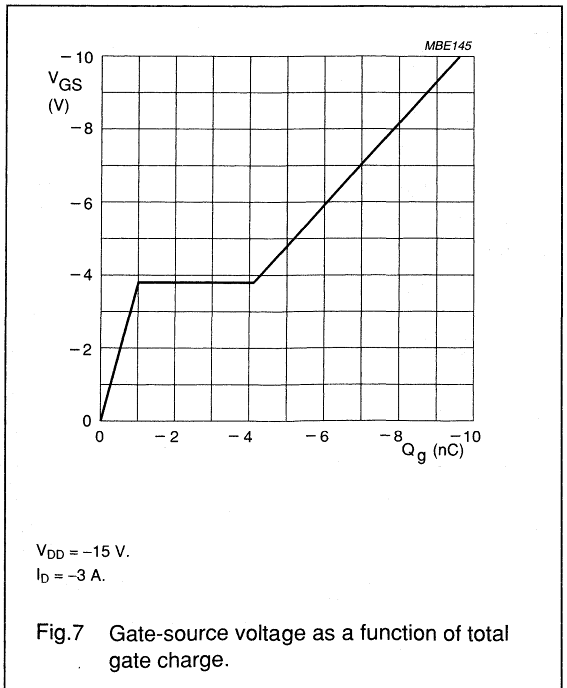
$T_j = 25$ °C.

Fig.5 Output characteristics; typical values.



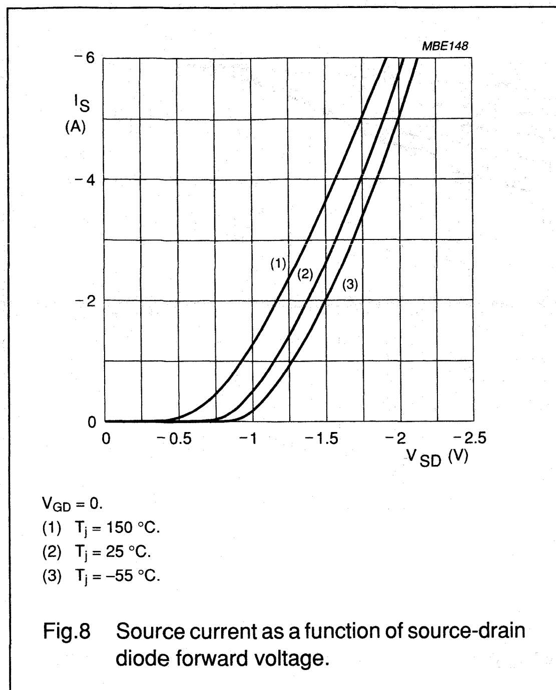
$V_{DS} = -10$ V.
$T_j = 25$ °C.

Fig.6 Transfer characteristic, typical values.



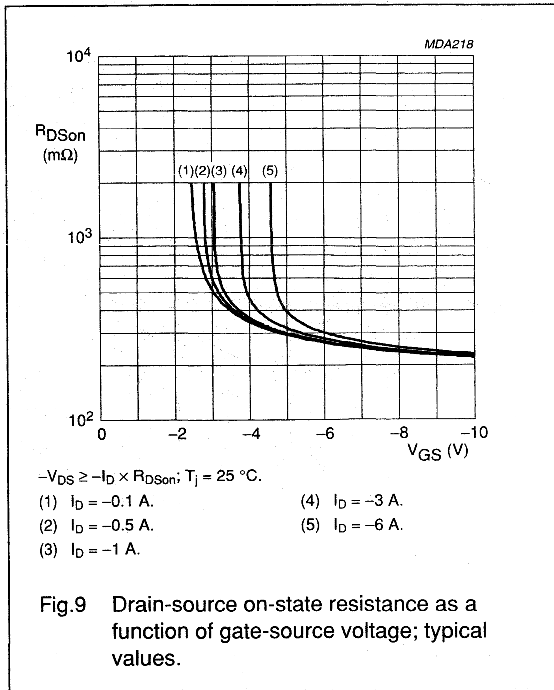
$V_{DD} = -15$ V.
$I_D = -3$ A.

Fig.7 Gate-source voltage as a function of total gate charge.



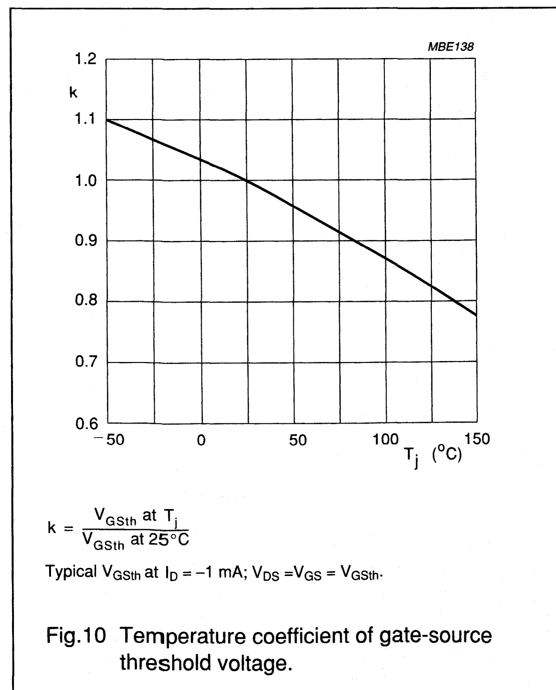
$V_{GD} = 0$.
(1) $T_j = 150$ °C.
(2) $T_j = 25$ °C.
(3) $T_j = -55$ °C.

Fig.8 Source current as a function of source-drain diode forward voltage.



$-V_{DS} \geq -I_D \times R_{DSon}$; $T_j = 25$ °C.
(1) $I_D = -0.1$ A.
(2) $I_D = -0.5$ A.
(3) $I_D = -1$ A.
(4) $I_D = -3$ A.
(5) $I_D = -6$ A.

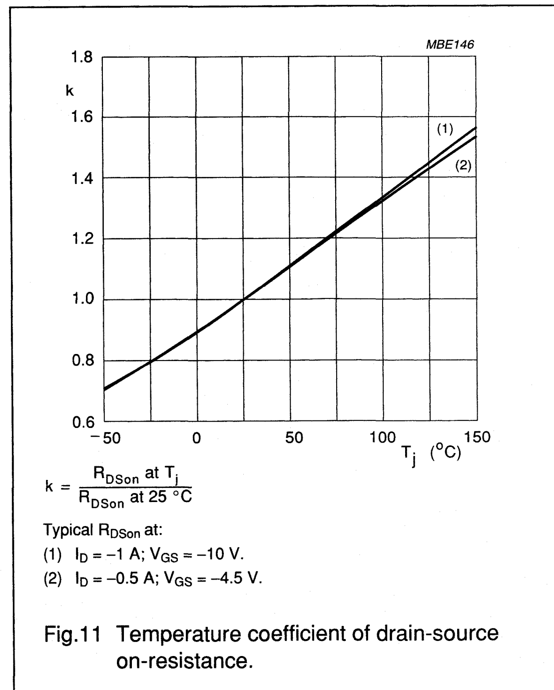
Fig.9 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

Typical V_{GSth} at $I_D = -1$ mA; $V_{DS} = V_{GS} = V_{GSth}$.

Fig.10 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25 °C}$$

Typical R_{DSon} at:
(1) $I_D = -1$ A; $V_{GS} = -10$ V.
(2) $I_D = -0.5$ A; $V_{GS} = -4.5$ V.

Fig.11 Temperature coefficient of drain-source on-resistance.

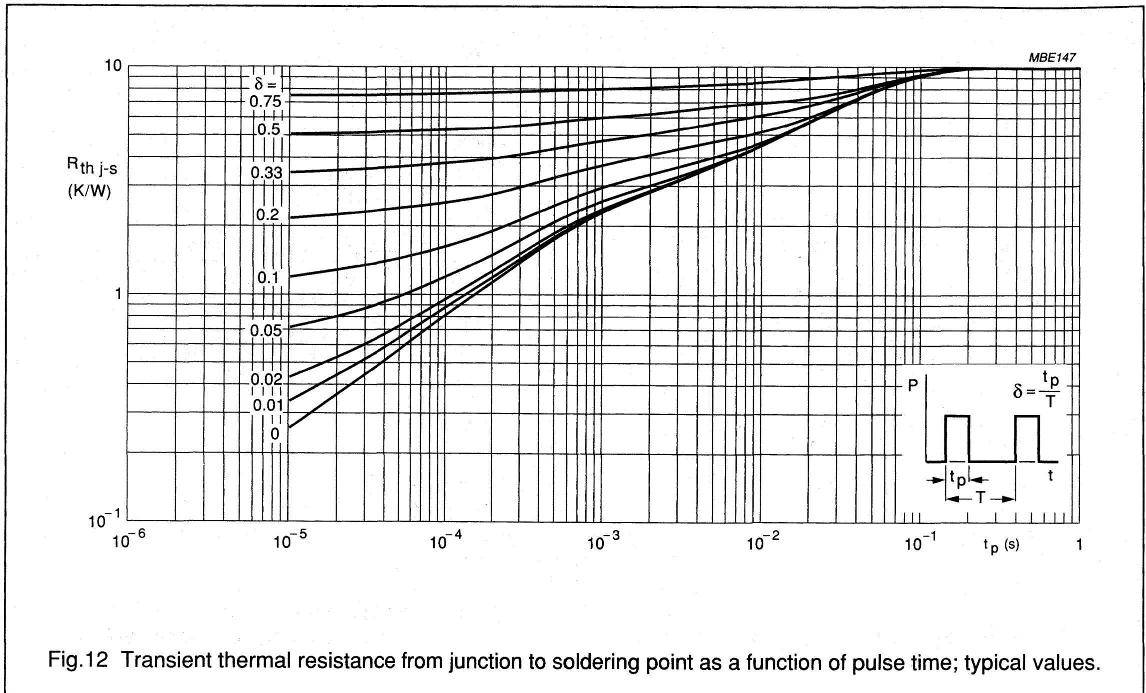


Fig.12 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

P-channel enhancement mode vertical D-MOS transistor

BSP254; BSP254A

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

P-channel vertical D-MOS transistor in a TO-92 variant envelope and intended for use as a line current interruptor in relay, high-speed and line transformer drivers.

PINNING - TO-92 variant BSP254

PIN	DESCRIPTION
1	gate
2	drain
3	source

PINNING - TO-92 variant BSP254A

PIN	DESCRIPTION
1	source
2	gate
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	–250	V
V_{GSO}	gate-source voltage	open drain	–	–	±20	V
$\|Y_{fs}\|$	forward transfer admittance	I_D = –200 mA; V_{DS} = –25V	100	200	–	mS
I_D	drain current (DC)		–	–	–0.2	A
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = –10 V; I_D = –200 mA	–	10	15	Ω
P_{tot}	total power dissipation	T_{amb} = 25 °C	–	–	1	W

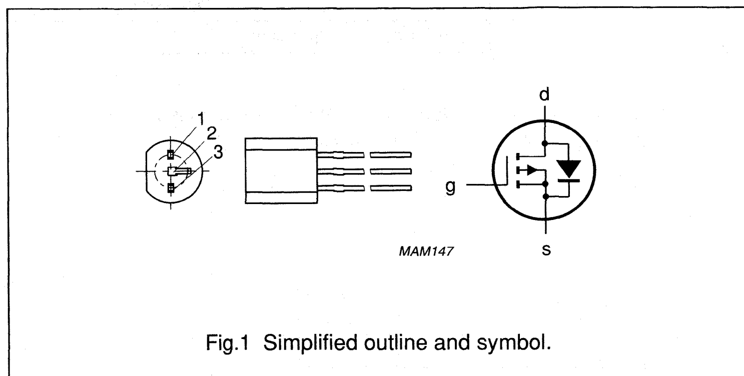


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	250	V
V_{GSO}	gate-source voltage	open drain	–	20	V
$-I_D$	drain current	DC	–	0.2	A
$-I_{DM}$	drain current	peak value	–	0.6	A
P_{tot}	total power dissipation	T_{amb} = 25 °C (note 1)	–	1	W
T_{stg}	storage temperature range		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	125	K/W

Note

1. Transistor mounted on printed circuit board, maximum lead length 4 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

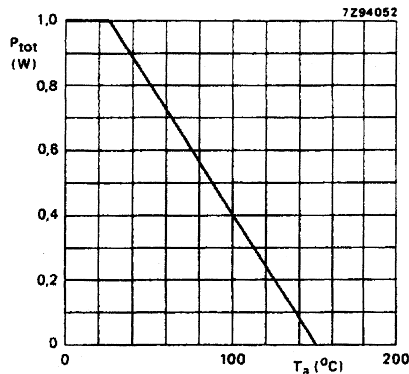


Fig.2 Power derating curve.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-V_{GS}$ = 0 $-I_D$ = 10 μA	250	–	–	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS}$ = 200 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$V_{GS} = V_{DS}$ $-I_D$ = 1 mA	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-V_{GS}$ = 10 V $-I_D$ = 200 mA;	–	10	15	Ω
$\|Y_{fs}\|$	transfer admittance	$-V_{DS}$ = 25 V $-I_D$ = 200 mA	100	200	–	mS
C_{iss}	input capacitance	note 1	–	65	90	pF
C_{oss}	output capacitance	note 1	–	20	30	pF
C_{rss}	feedback capacitance	note 1	–	6	15	pF
t_{on}	turn-on time	note 2	–	5	10	ns
t_{off}	turn-off time	note 2	–	20	30	ns

Notes

1. Measured at f = 1 MHz; $-V_{DS}$ = 25 V; V_{GS} = 0.
2. $-V_{GS}$ = 0 to 10 V; $-I_D$ = 250 mA; $-V_{DD}$ = 50 V.

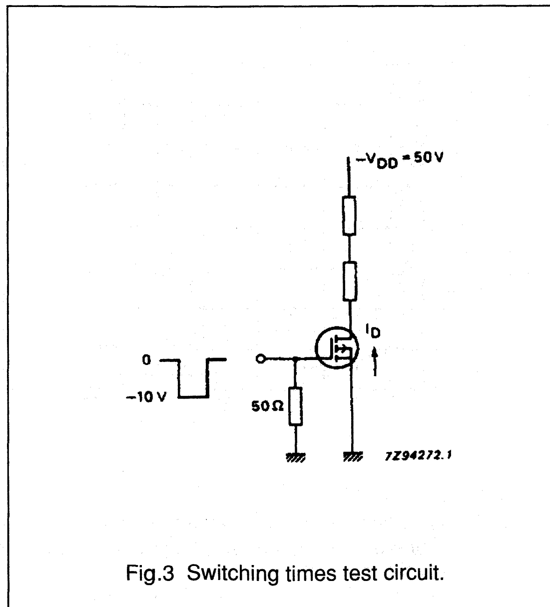


Fig.3 Switching times test circuit.

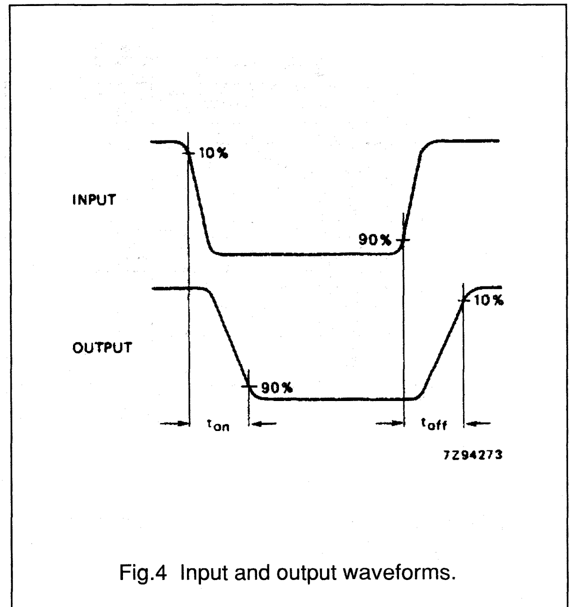


Fig.4 Input and output waveforms.

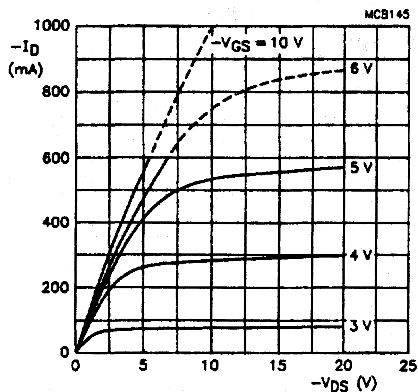


Fig.5 Typical output characteristics; T_j = 25 °C.

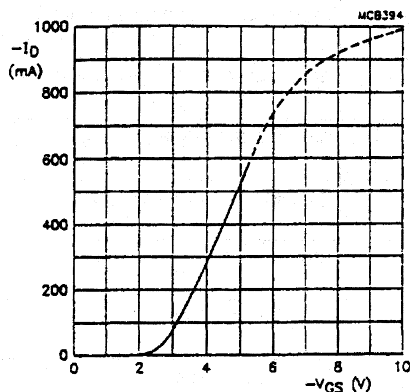


Fig.6 Typical transfer characteristic; V_{DS} = −10 V; T_j = 25 °C.

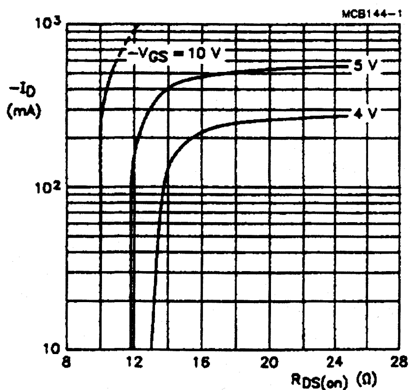


Fig.7 Typical on-resistance as a function of drain current, T_j = 25 °C.

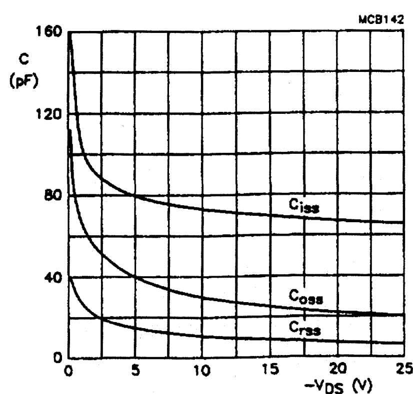


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

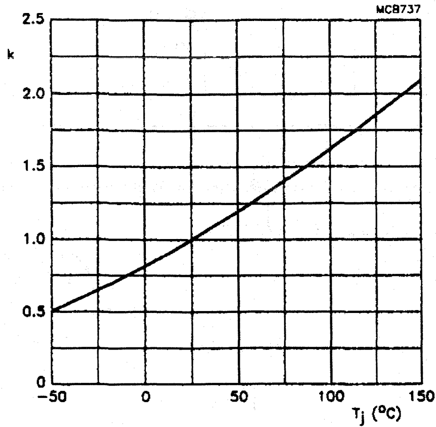


Fig.9

$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25\ °C}$$

typical $R_{DS(on)}$ at −200 mA/−10 V.

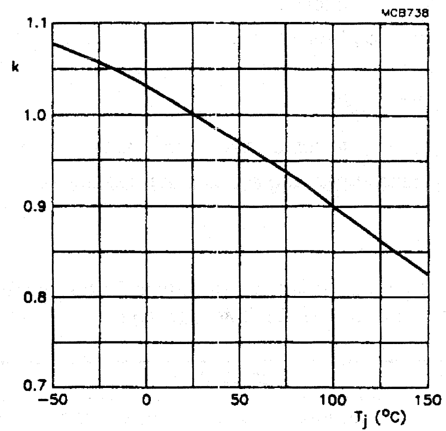


Fig.10

$$k = \frac{-V_{GS(th)} \text{ at } T_j}{-V_{GS(th)} \text{ at } 25\ °C}$$

typical $V_{GS(th)}$ at −1 mA.

P-channel enhancement mode vertical D-MOS transistor

BSP255

FEATURES

- Direct interface to C-MOS, TTL etc
- Low threshold voltage
- High speed switching
- No secondary breakdown.

APPLICATIONS

- Line current interrupter in telephone sets
- Relay, high speed and line transformer drivers.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a 4-pin plastic SOT223 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT223

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source
4	d	drain

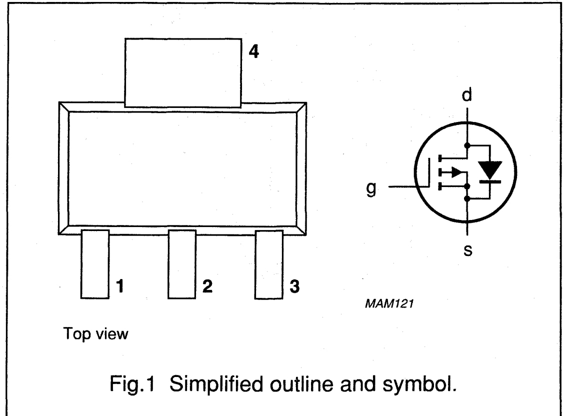


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–300	V
V_{SD}	source-drain diode forward voltage	$I_S = -0.5$ A	–	–1.8	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	$I_D = -1$ mA; $V_{DS} = V_{GS}$	–0.8	–2	V
I_D	drain current (DC)	$T_s = 100$ °C	–	–325	mA
R_{DSon}	drain-source on-state resistance	$I_D = -160$ mA; $V_{GS} = -10$ V	–	17	Ω
P_{tot}	total power dissipation	$T_s = 100$ °C	–	4	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–300	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 100 °C; note 1	–	–325	mA
I_{DM}	peak drain current	note 2	–	–1.3	A
P_{tot}	total power dissipation	T_s = 100 °C	–	4	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–65	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 100 °C	–	–0.5	A
I_{SM}	peak pulsed source current	note 2	–	–2	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.

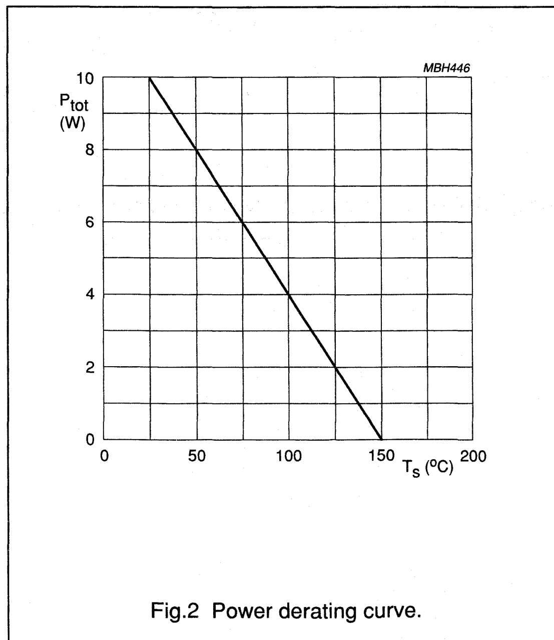
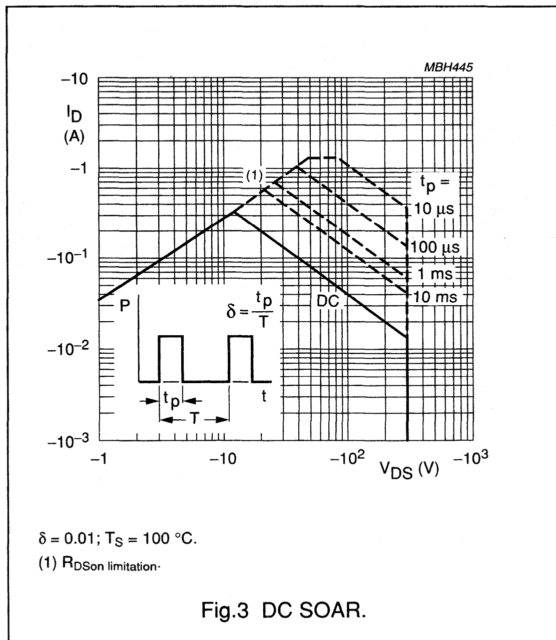


Fig.2 Power derating curve.



δ = 0.01; T_S = 100 °C.

(1) R_{DSon} limitation.

Fig.3 DC SOAR.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	12	K/W

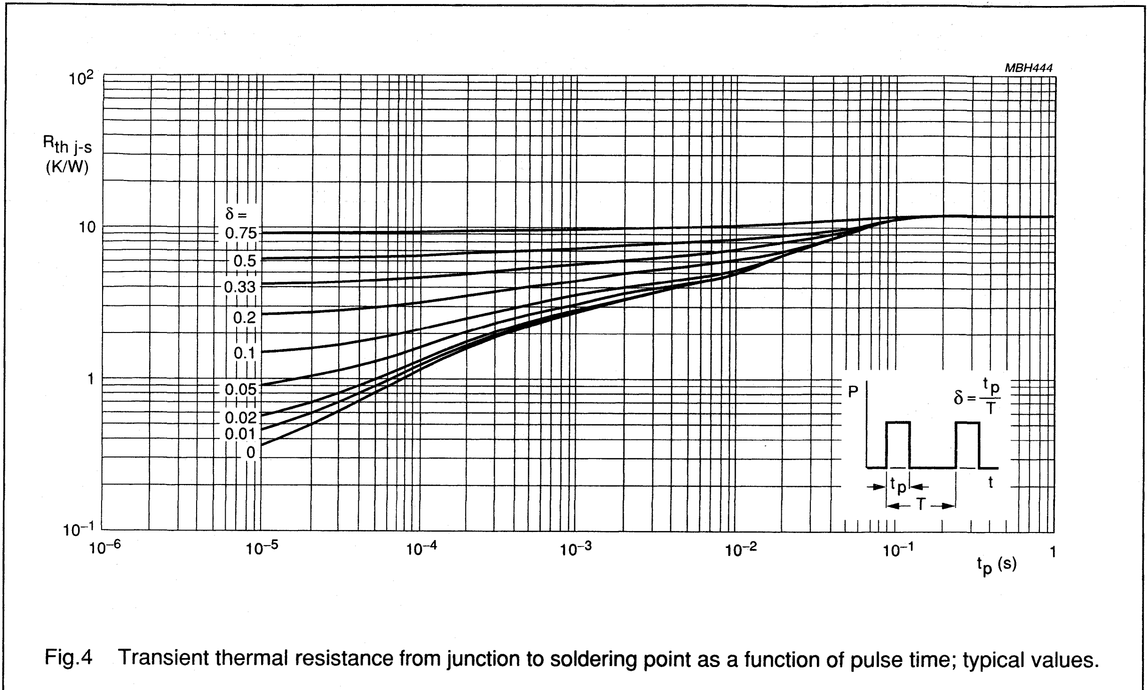
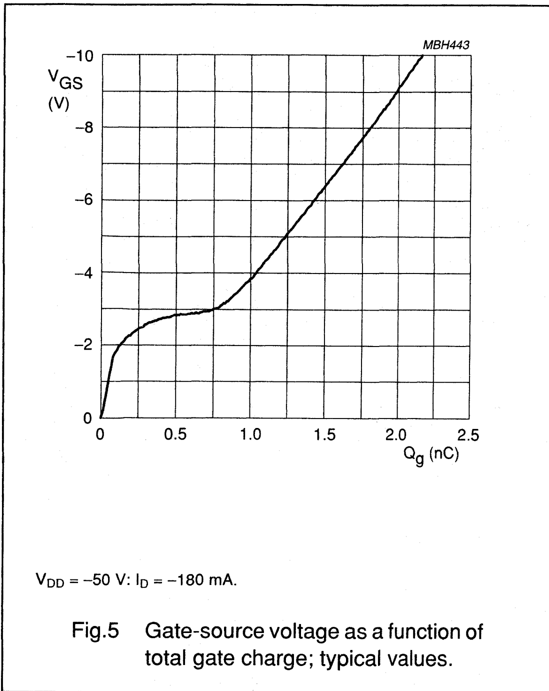


Fig.4 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

CHARACTERISTICS

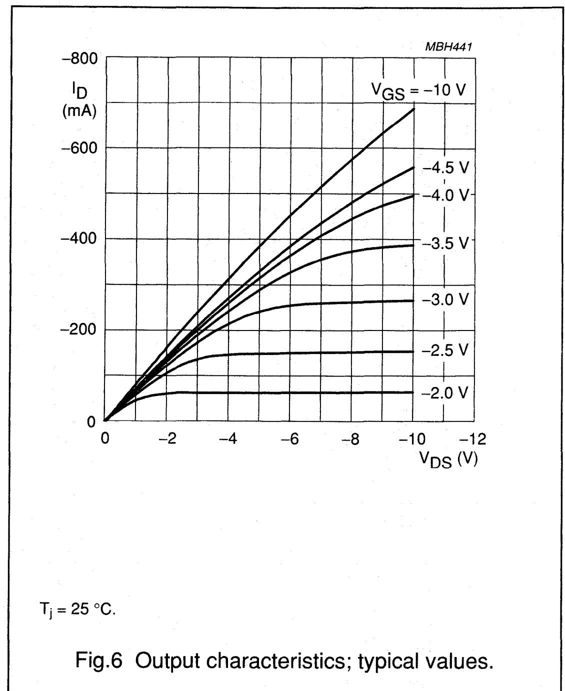
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−300	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−0.8	–	−2	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −240 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −10 V; I_D = −160 mA	–	–	17	Ω
		V_{GS} = −4.5 V; I_D = −80 mA	–	–	20	Ω
		V_{GS} = −2.8 V; I_D = −50 mA	–	–	25	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −50 V; f = 1 MHz	–	45	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −50 V; f = 1 MHz	–	15	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −50 V; f = 1 MHz	–	3	–	pF
Q_g	total gate charge	V_{GS} = −10 V; V_{DD} = −50 V; I_D = −160 mA; T_{amb} = 25 °C	–	2.3	–	nC
Q_{gs}	gate-source charge	V_{GS} = −10 V; V_{DD} = −50 V; I_D = −160 mA; T_{amb} = 25 °C	–	0.1	–	nC
Q_{gd}	gate-drain charge	V_{GS} = −10 V; V_{DD} = −50 V; I_D = −160 mA; T_{amb} = 25 °C	–	0.7	–	nC
Switching times (see Fig.11)						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −10 V; V_{DD} = −50 V; I_D = −160 mA; R_{gen} = 50 Ω	–	2.4	–	ns
t_r	rise time		–	1.6	–	ns
t_{on}	turn-on switching time		–	4	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = −10 to 0 V; V_{DD} = −50 V; I_D = −160 mA; R_{gen} = 50 Ω	–	13	–	ns
t_f	fall time		–	12	–	ns
t_{off}	turn-off switching time		–	25	–	ns
Source-drain diode						
V_{SD}	source-drain forward voltage	V_{GD} = 0; I_S = −0.5 A	–	–	−1.8	V



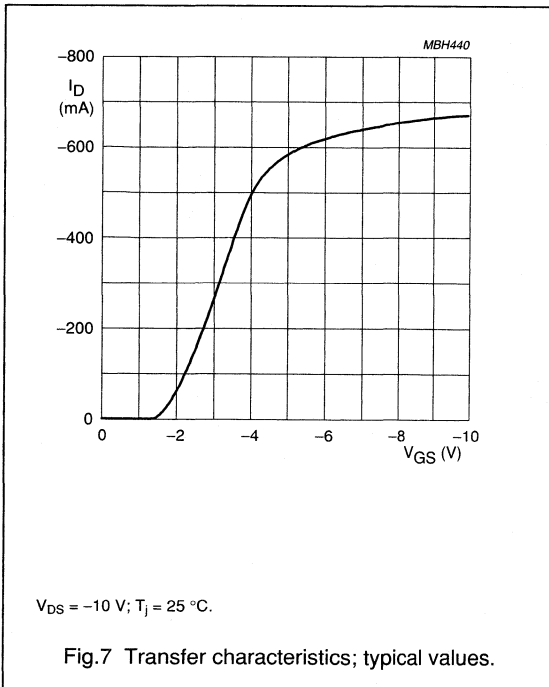
V_{DD} = −50 V: I_D = −180 mA.

Fig.5 Gate-source voltage as a function of total gate charge; typical values.



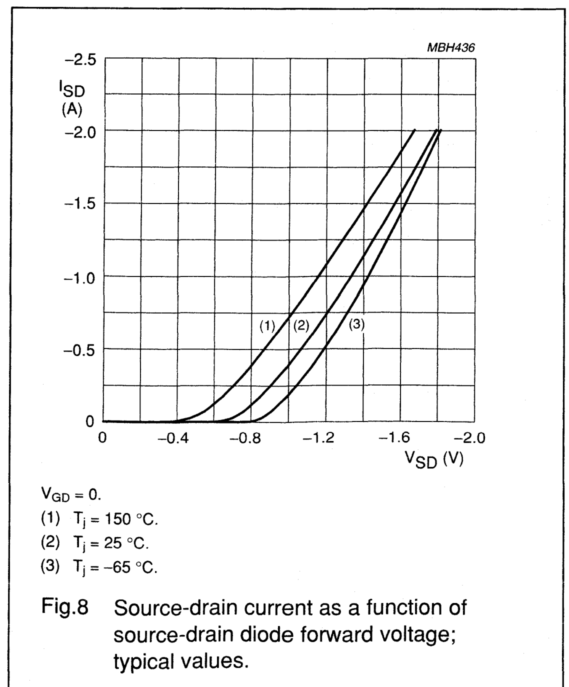
T_j = 25 °C.

Fig.6 Output characteristics; typical values.



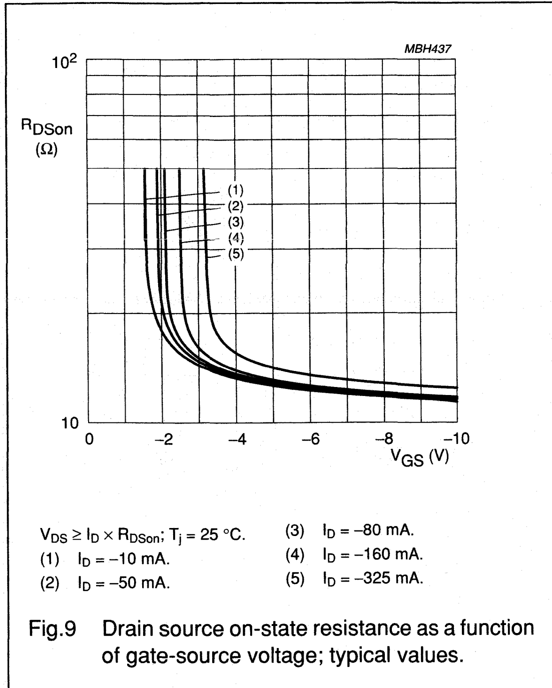
V_{DS} = −10 V; T_j = 25 °C.

Fig.7 Transfer characteristics; typical values.



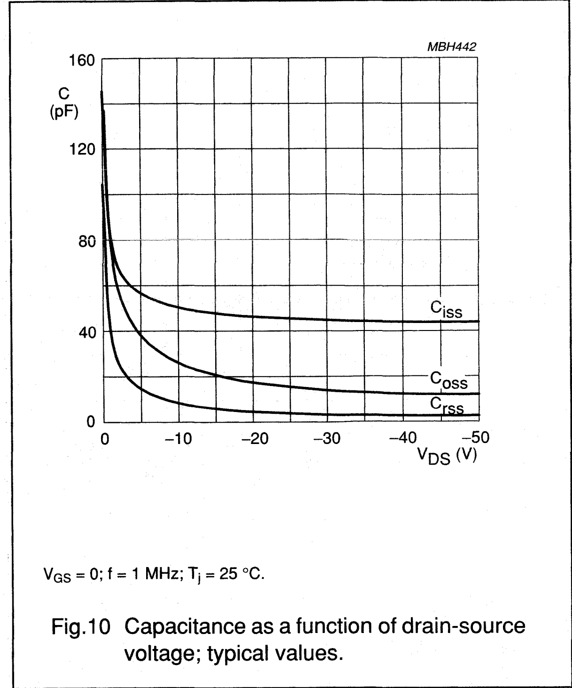
V_{GD} = 0.
(1) T_j = 150 °C.
(2) T_j = 25 °C.
(3) T_j = −65 °C.

Fig.8 Source-drain current as a function of source-drain diode forward voltage; typical values.



$V_{DS} \geq I_D \times R_{DSon}$; T_j = 25 °C.
(1) I_D = −10 mA.
(2) I_D = −50 mA.
(3) I_D = −80 mA.
(4) I_D = −160 mA.
(5) I_D = −325 mA.

Fig.9 Drain source on-state resistance as a function of gate-source voltage; typical values.



V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.10 Capacitance as a function of drain-source voltage; typical values.

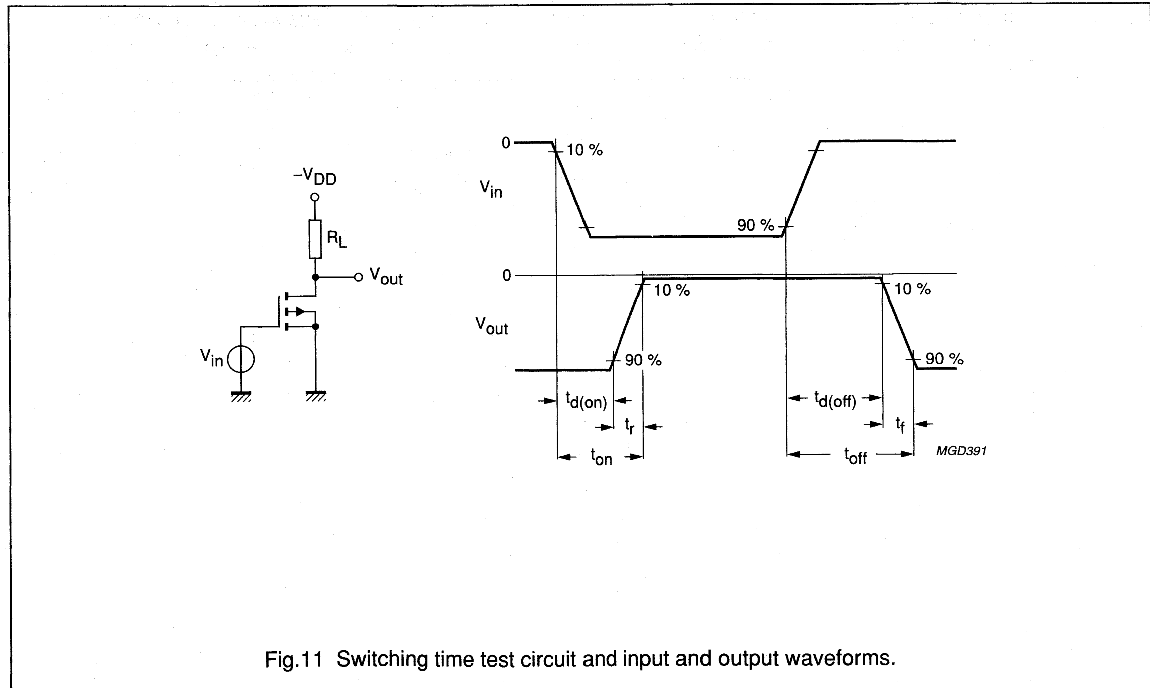
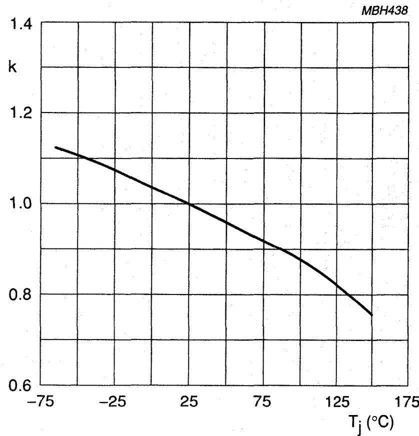


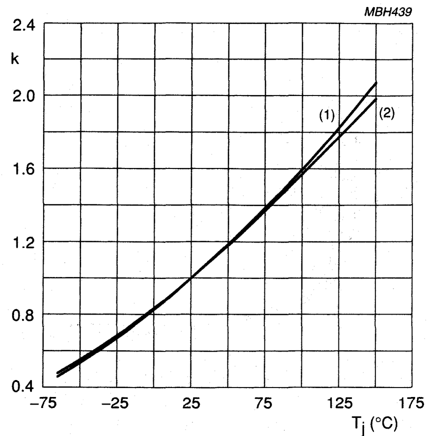
Fig.11 Switching time test circuit and input and output waveforms.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; $I_D = -1$ mA.

Fig.12 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25 °C}$$

(1) $V_{GS} = -4.5$ V; $I_D = -80$ mA.
(2) $V_{GS} = -2.8$ V; $I_D = -50$ mA.

Fig.13 Temperature coefficient of drain-source on-state resistance as a function of junction temperature; typical values.

P-channel enhancement mode vertical D-MOS transistors

BSP304; BSP304A

FEATURES

- Direct interface to C-MOS, TTL etc.
- High speed switching
- No secondary breakdown.

APPLICATIONS

- Intended for use as a Line current interruptor in telephone sets and for applications in relay, high speed and line transformer drivers.

PINNING - TO-92 variant

PIN	SYMBOL	DESCRIPTION
BSP304		
1	g	gate
2	d	drain
3	s	source
BSP304A		
1	s	source
2	g	gate
3	d	drain

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a TO-92 variant package.

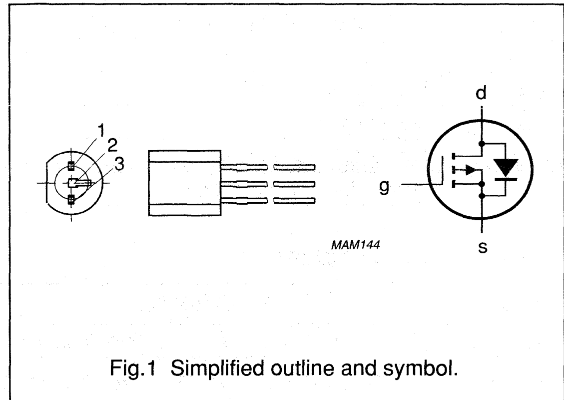


Fig.1 Simplified outline and symbol.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–300	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	$I_D = -1$ mA; $V_{DS} = V_{GS}$	–1.7	–2.55	V
I_D	drain current (DC)		–	–170	mA
R_{DSon}	drain-source on-state resistance	$I_D = -170$ mA; $V_{GS} = -10$ V	–	17	Ω
P_{tot}	total power dissipation	up to $T_{amb} = 25$ °C	–	1	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–300	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	–170	mA
I_{DM}	peak drain current		–	–0.75	A
P_{tot}	total power dissipation	up to T_{amb} = 25 °C; note 1	–	1	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	125	K/W

Note to the "Limiting values" and "Thermal characteristics"

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for drain lead minimum 1 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = –10 μA	–300	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = –1 mA	–1.7	–	–2.55	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = –240 V	–	–	–100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = –10 V; I_D = –170 mA	–	–	17	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = –25 V; I_D = –170 mA	100	–	–	mS
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = –25 V; f = 1 MHz	–	60	90	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = –25 V; f = 1 MHz	–	15	30	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = –20 V; f = 1 MHz	–	5	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	V_{GS} = 0 to –10 V; V_{DD} = –50 V; I_D = –250 mA	–	5	10	ns
t_{off}	turn-off time	V_{GS} = –10 to 0 V; V_{DD} = –50 V; I_D = –250 mA	–	15	30	ns

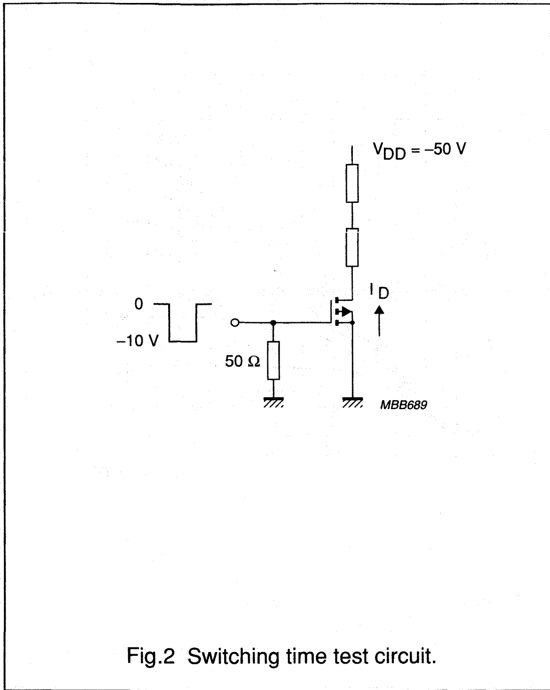


Fig.2 Switching time test circuit.

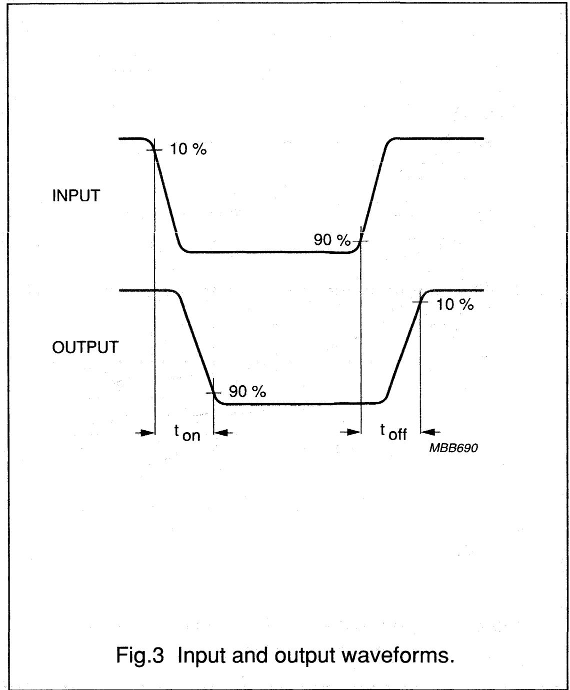


Fig.3 Input and output waveforms.

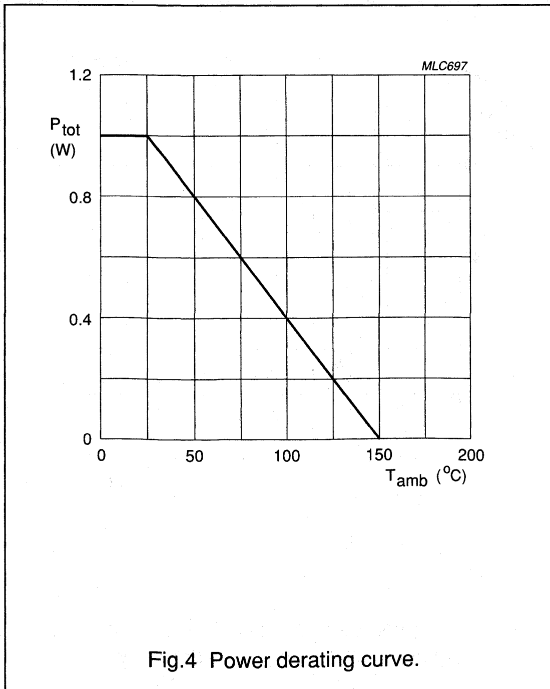
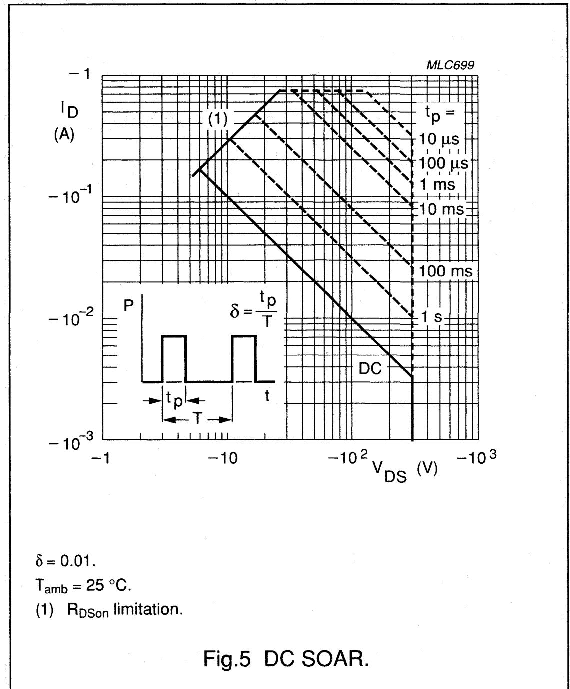


Fig.4 Power derating curve.

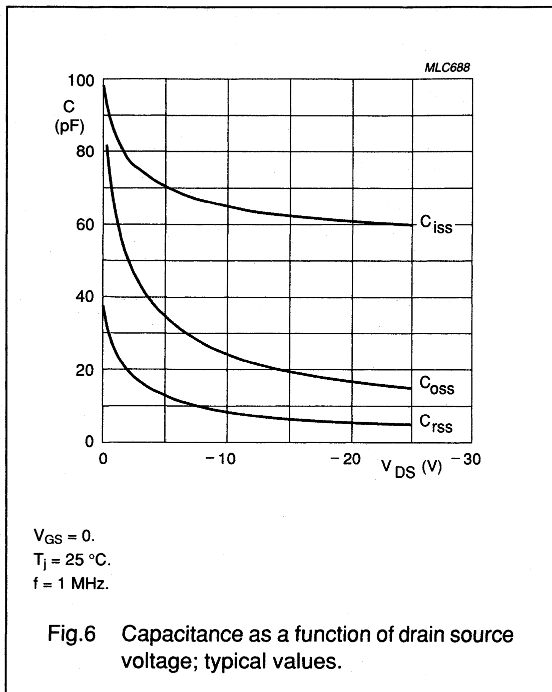


δ = 0.01.

T_{amb} = 25 °C.

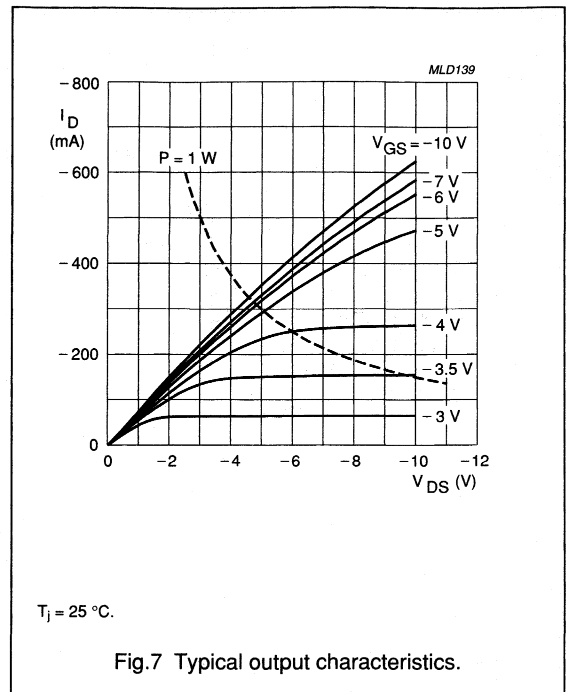
(1) R_{DSon} limitation.

Fig.5 DC SOAR.



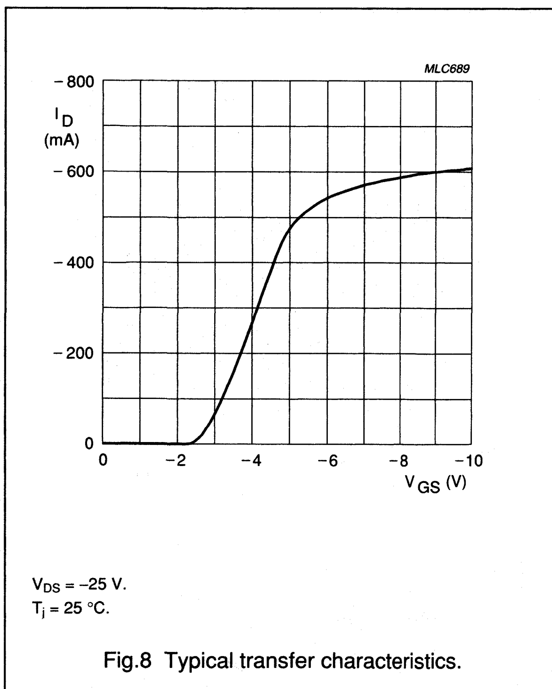
V_{GS} = 0.
T_j = 25 °C.
f = 1 MHz.

Fig.6 Capacitance as a function of drain source voltage; typical values.



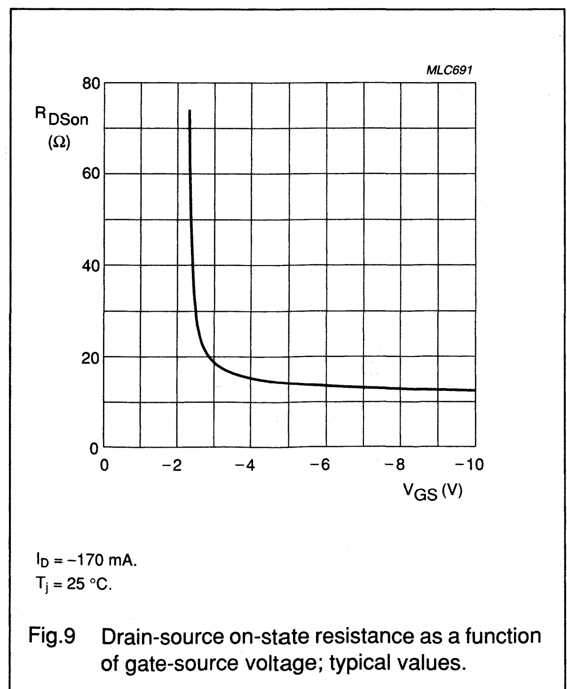
T_j = 25 °C.

Fig.7 Typical output characteristics.



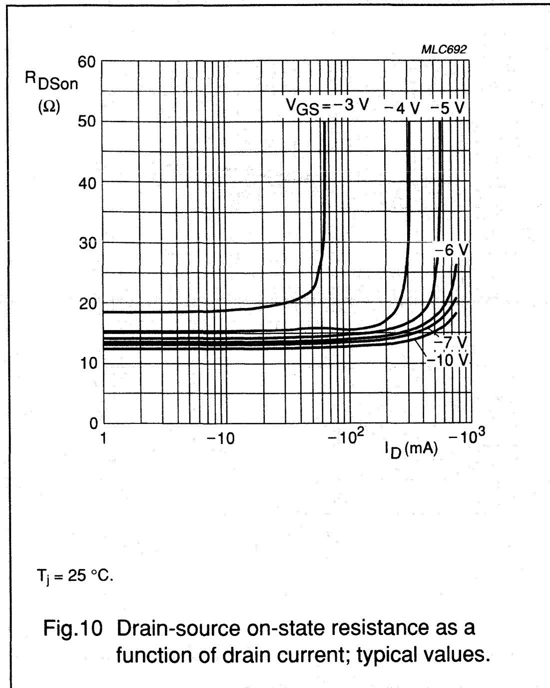
V_{DS} = −25 V.
T_j = 25 °C.

Fig.8 Typical transfer characteristics.



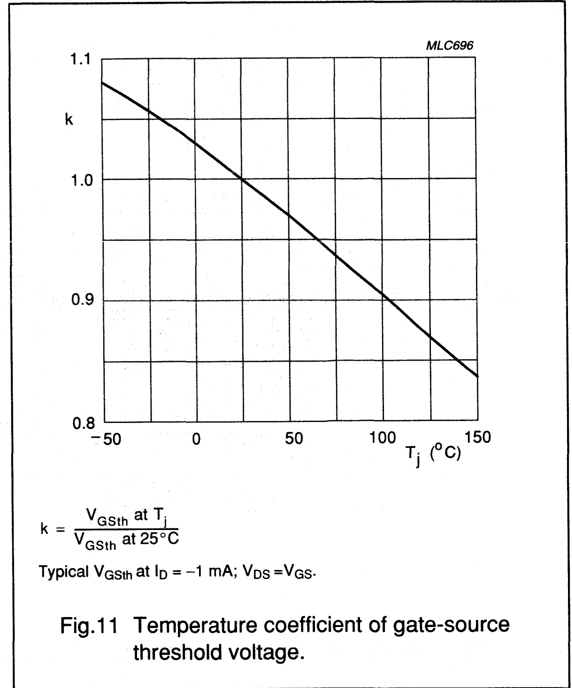
I_D = −170 mA.
T_j = 25 °C.

Fig.9 Drain-source on-state resistance as a function of gate-source voltage; typical values.



T_j = 25 °C.

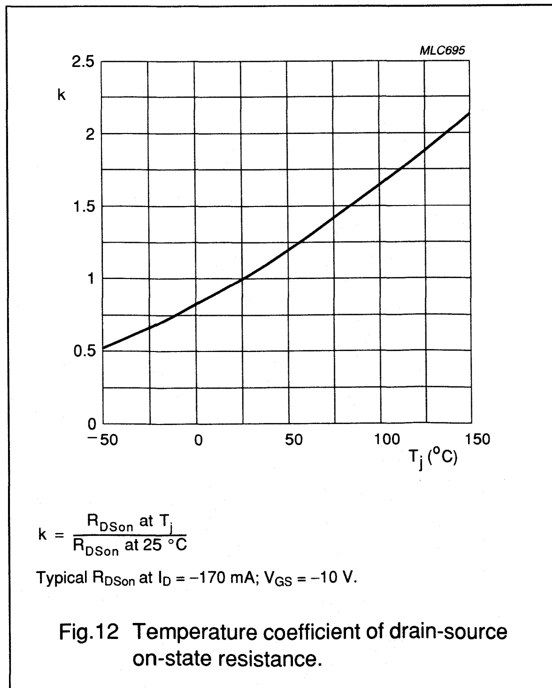
Fig.10 Drain-source on-state resistance as a function of drain current; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25\,°C}$$

Typical V_{GSth} at I_D = −1 mA; V_{DS} = V_{GS}.

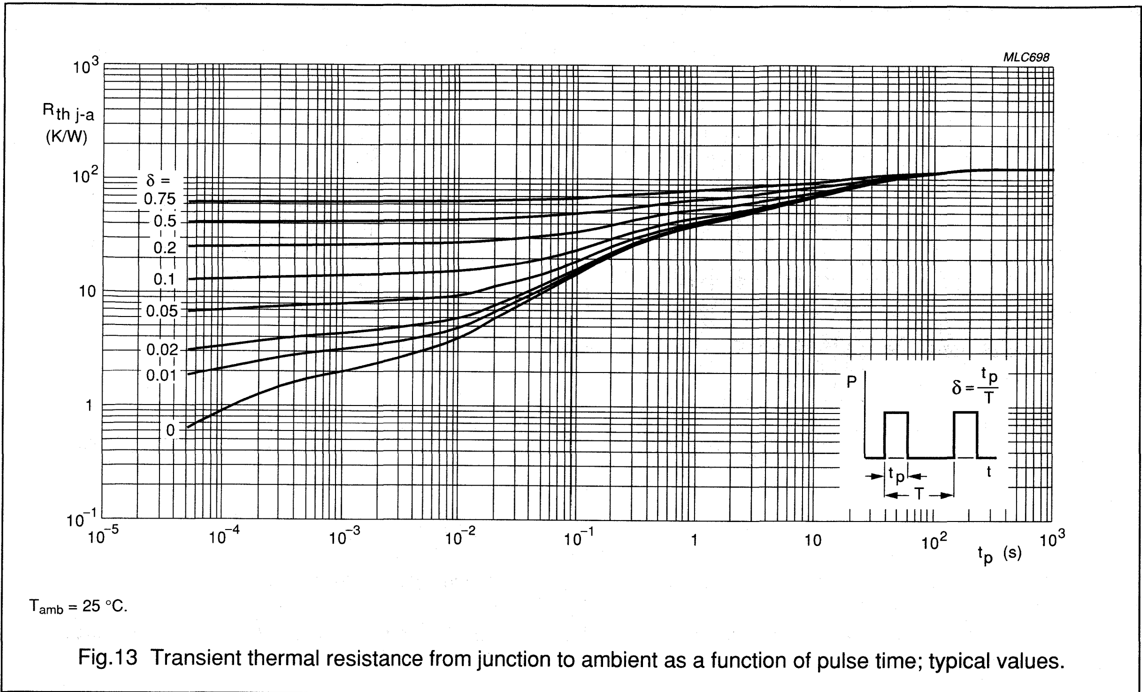
Fig.11 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\,°C}$$

Typical R_{DSon} at I_D = −170 mA; V_{GS} = −10 V.

Fig.12 Temperature coefficient of drain-source on-state resistance.



T_{amb} = 25 °C.

Fig.13 Transient thermal resistance from junction to ambient as a function of pulse time; typical values.

P-channel enhancement mode vertical D-MOS transistor

BSS84

FEATURES

- Low threshold voltage
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Line current interrupter in telephone sets
- Relay, high speed and line transformer drivers.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a SOT23 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain

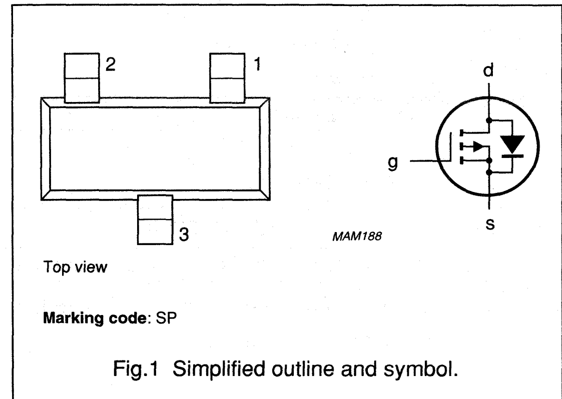


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–50	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	$I_D = -1$ mA; $V_{DS} = V_{GS}$	–0.8	–2	V
I_D	drain current (DC)		–	–130	mA
R_{DSon}	drain-source on-state resistance	$I_D = -130$ mA; $V_{GS} = -10$ V	–	10	Ω
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	250	mW

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–50	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	–130	mA
I_{DM}	peak drain current		–	–520	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	250	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	500	K/W

Note to the Limiting values and Thermal characteristics

1. Device mounted on a printed-circuit board.

CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = -10$ μA	–50	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = V_{GS}$; $I_D = -1$ mA	–0.8	–	–2	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = -40$ V	–	–	–100	nA
		$V_{GS} = 0$; $V_{DS} = -50$ V	–	–	–10	μA
		$V_{GS} = 0$; $V_{DS} = -50$ V; $T_j = 125$ °C	–	–	–60	μA
I_{GSS}	gate leakage current	$V_{DS} = 0$; $V_{GS} = \pm 20$ V	–	–	±10	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -10$ V; $I_D = -130$ mA	–	–	10	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	$V_{DS} = -25$ V; $I_D = -130$ mA	50	–	–	mS
C_{iss}	input capacitance	$V_{GS} = 0$; $V_{DS} = -25$ V; f = 1 MHz	–	25	45	pF
C_{oss}	output capacitance	$V_{GS} = 0$; $V_{DS} = -25$ V; f = 1 MHz	–	15	25	pF
C_{rss}	reverse transfer capacitance	$V_{GS} = 0$; $V_{DS} = -25$ V; f = 1 MHz	–	3.5	12	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$V_{GS} = 0$ to -10 V; $V_{DD} = -40$ V; $I_D = -200$ mA	–	3	–	ns
t_{off}	turn-off time	$V_{GS} = -10$ to 0 V; $V_{DD} = -40$ V; $I_D = -200$ mA	–	7	–	ns

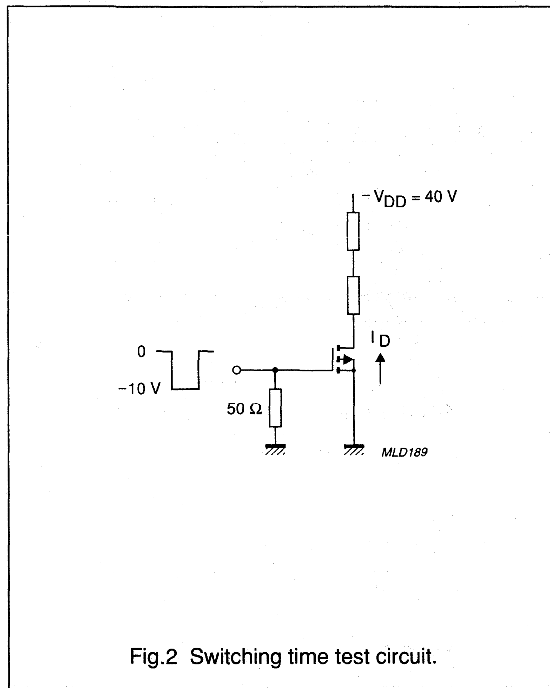


Fig.2 Switching time test circuit.

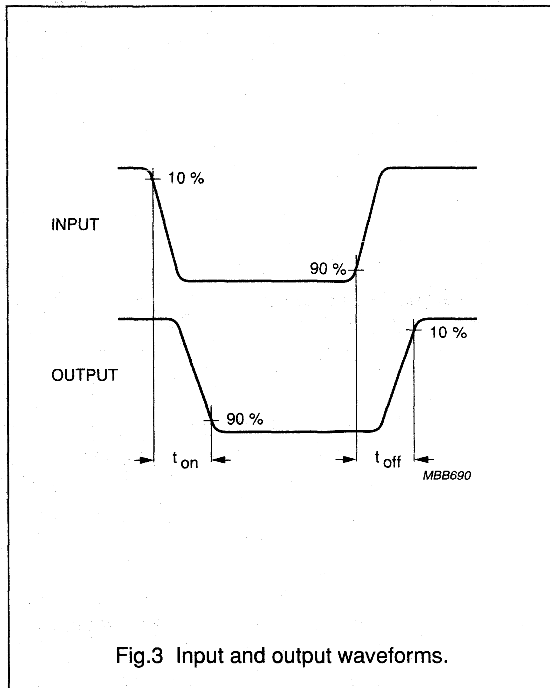


Fig.3 Input and output waveforms.

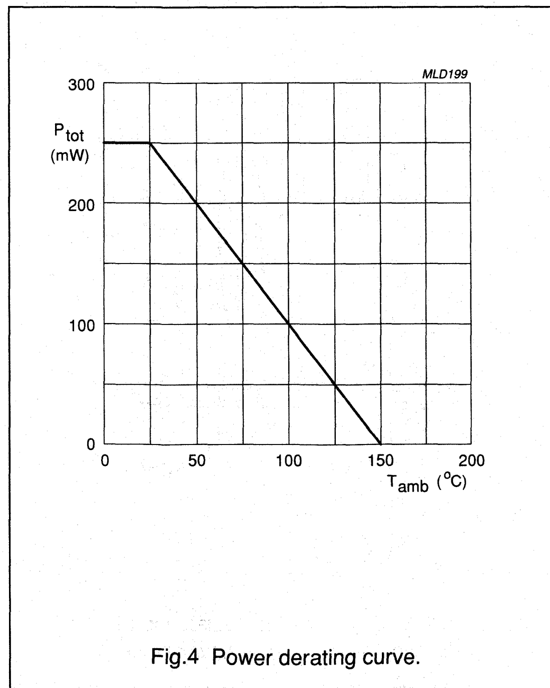
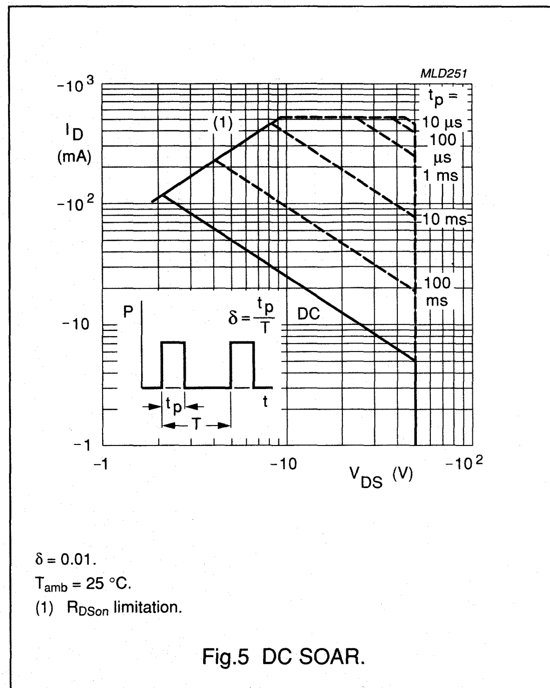


Fig.4 Power derating curve.

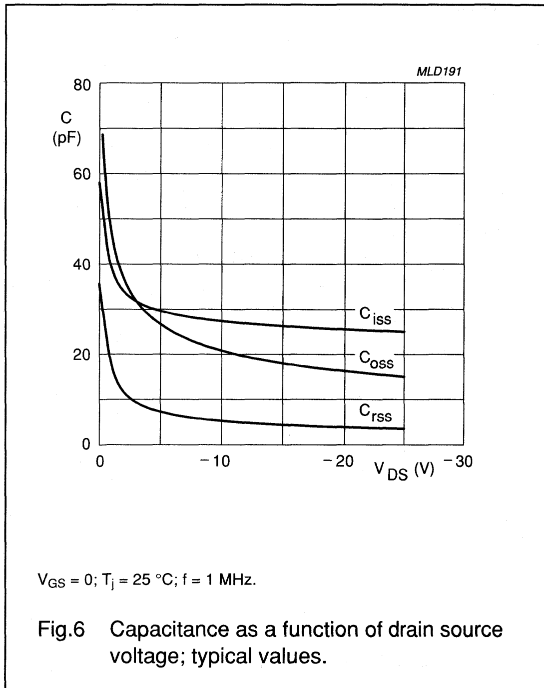


$\delta = 0.01$.

$T_{amb} = 25$ °C.

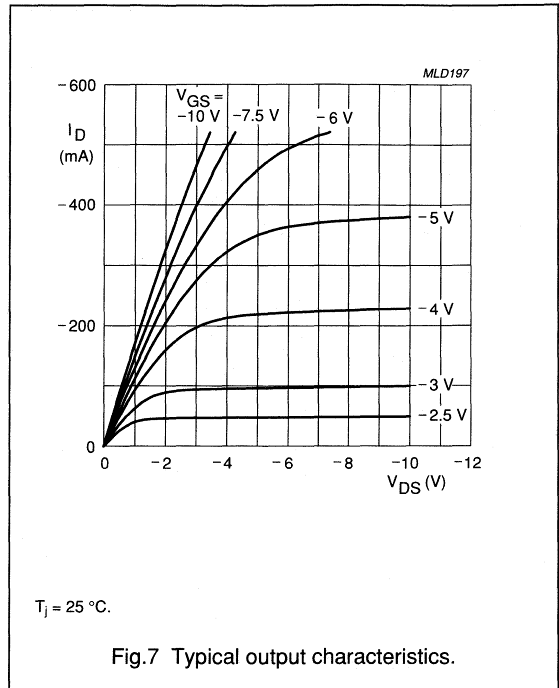
(1) R_{DSon} limitation.

Fig.5 DC SOAR.



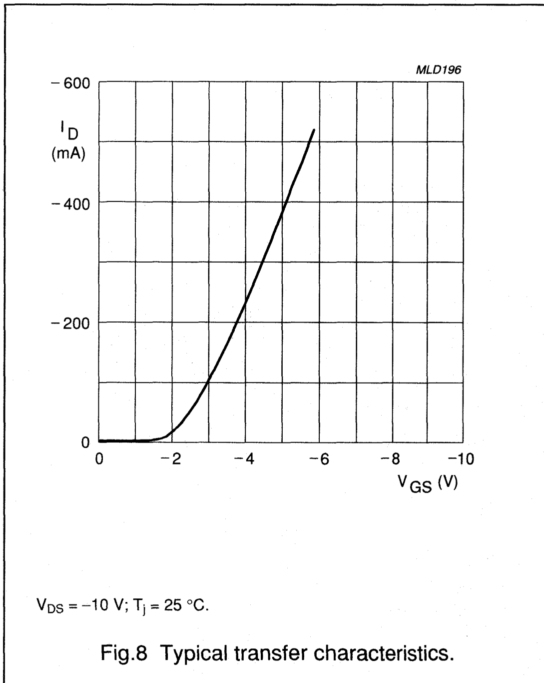
V_{GS} = 0; T_j = 25 °C; f = 1 MHz.

Fig.6 Capacitance as a function of drain source voltage; typical values.



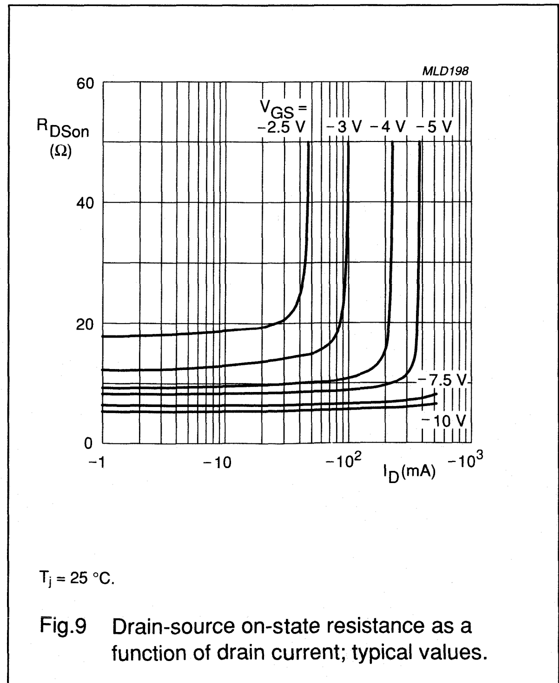
T_j = 25 °C.

Fig.7 Typical output characteristics.



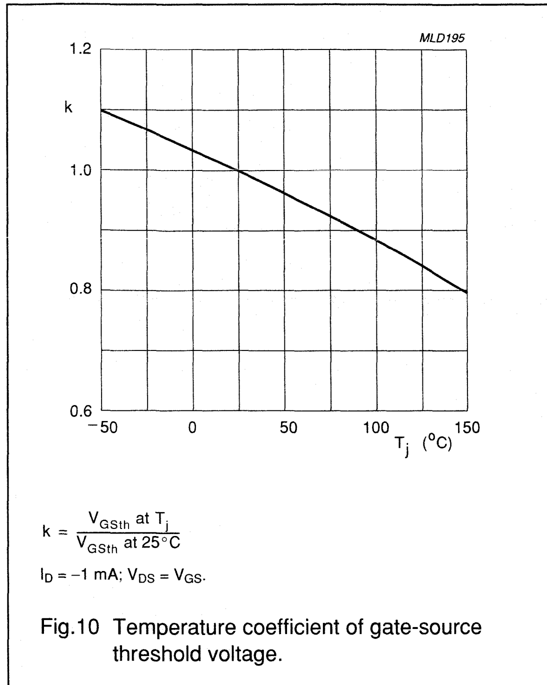
V_{DS} = −10 V; T_j = 25 °C.

Fig.8 Typical transfer characteristics.



T_j = 25 °C.

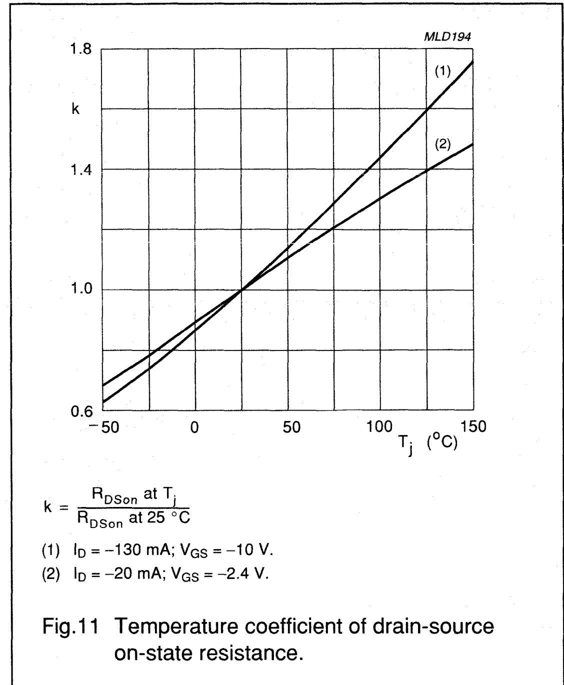
Fig.9 Drain-source on-state resistance as a function of drain current; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25\,°C}$$

I_D = −1 mA; V_{DS} = V_{GS}.

Fig.10 Temperature coefficient of gate-source threshold voltage.

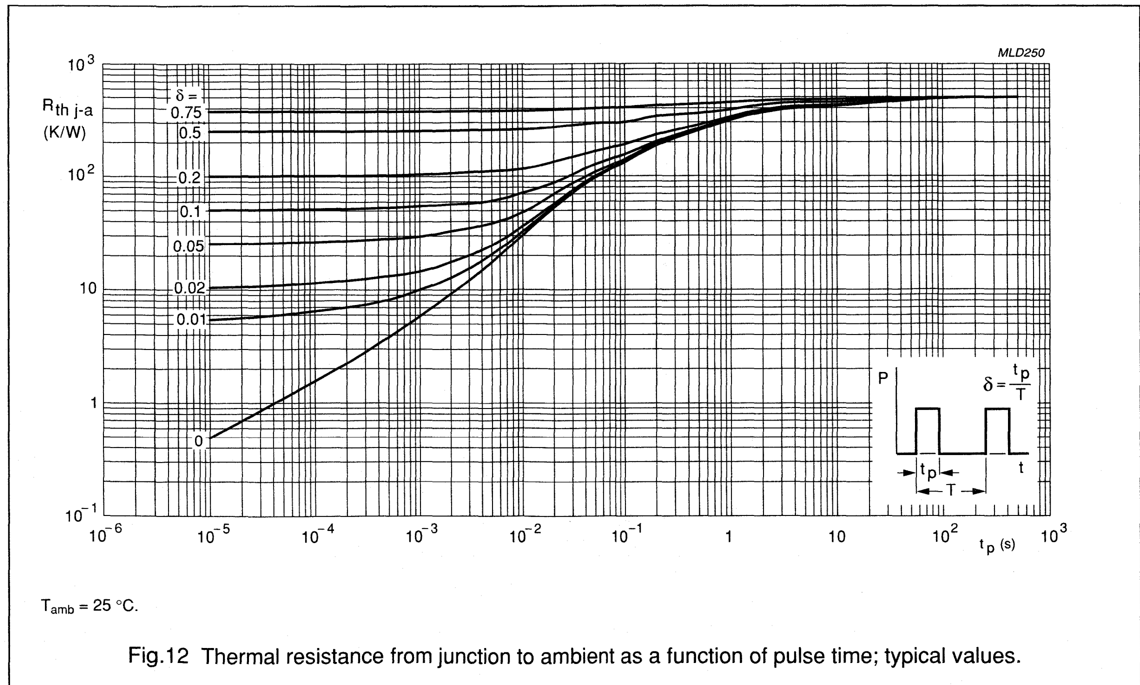


$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\,°C}$$

(1) I_D = −130 mA; V_{GS} = −10 V.

(2) I_D = −20 mA; V_{GS} = −2.4 V.

Fig.11 Temperature coefficient of drain-source on-state resistance.



T_{amb} = 25 °C.

Fig.12 Thermal resistance from junction to ambient as a function of pulse time; typical values.

N-channel enhancement mode vertical D-MOS transistor

BSS87

DESCRIPTION

N-channel vertical D-MOS transistor in a SOT89 envelope. Designed primarily as a line current interrupter in telephone sets, it can also be applied in other applications such as in relays, line and high-speed transformer drivers etc.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.
- Low $R_{DS(on)}$

QUICK REFERENCE DATA

Parameter	Symbol		Value	Unit
Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	280	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source on-resistance				
I_D = 400 mA; V_{GS} = 10 V	$R_{DS(on)}$	max.	6	Ω
		typ.	4.5	Ω
Transfer admittance				
I_D = 400 mA; V_{DS} = 25 V	$\lvert Y_{fs} \rvert$	typ.	350	mS
		min.	140	mS

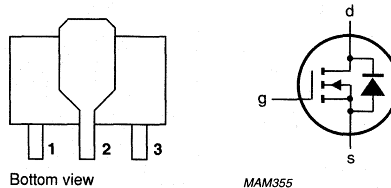
PINNING - SOT89

1 = source

2 = drain

3 = gate

PIN CONFIGURATION



marking: KA

Fig.1 Simplified outline and symbol.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	280	mA
Drain current (peak)	I_{DM}	max.	1.1	A
Total power dissipation up to T_{amb} = 25 °C [1]	P_{tot}	max.	1	W
Storage temperature range	T_{stg}	−65 to + 150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient [1]	$R_{th\ j\text{-}a}$	=	125	K/W

Note

1. Transistor mounted on ceramic substrate area 2.5 cm^2, thickness 0.7 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Drain-source breakdown voltage				
I_D = 250 µA; V_{GS} = 0	$V_{(BR)\ DSS}$	min.	200	V
Drain-source leakage current				
V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	200	nA
V_{DS} = 200 V; V_{GS} = 0	I_{DSS}	max.	60	µA
		typ.	100	nA
Gate-source leakage current				
V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage				
I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.8	V
		max.	2.8	V
Drain-source on-resistance				
I_D = 400 mA; V_{GS} = 10 V	$R_{DS(on)}$	max.	6	Ω
		typ.	4.5	Ω
Transfer admittance				
I_D = 400 mA; V_{DS} = 25 V	$\lvert Y_{fs} \rvert$	typ.	350	mS
		min.	140	mS
Input capacitance f = 1 MHz;				
V_{DS} = 25 V; V_{GS} = 0	C_{iss}	max.	60	pF
		typ.	45	pF
Output capacitance f = 1 MHz;				
V_{DS} = 25 V; V_{GS} = 0	C_{oss}	max.	25	pF
		typ.	15	pF

Feedback capacitance f = 1 MHz; V_{DS} = 25 V; V_{GS} = 0	C_{rss}	max.	10	pF
		typ.	3.5	pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V;	t_{on}	typ.	5	ns
		max.	10	ns
V_{GS} = 0 to 10	t_{off}	typ.	15	ns
		max.	25	ns

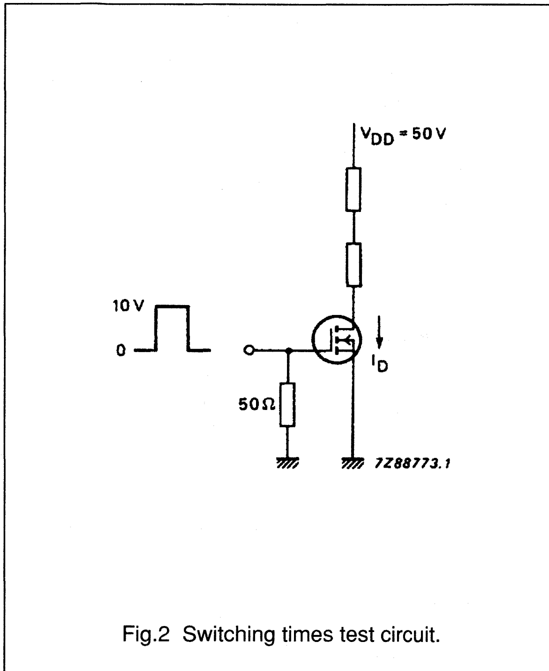


Fig.2 Switching times test circuit.

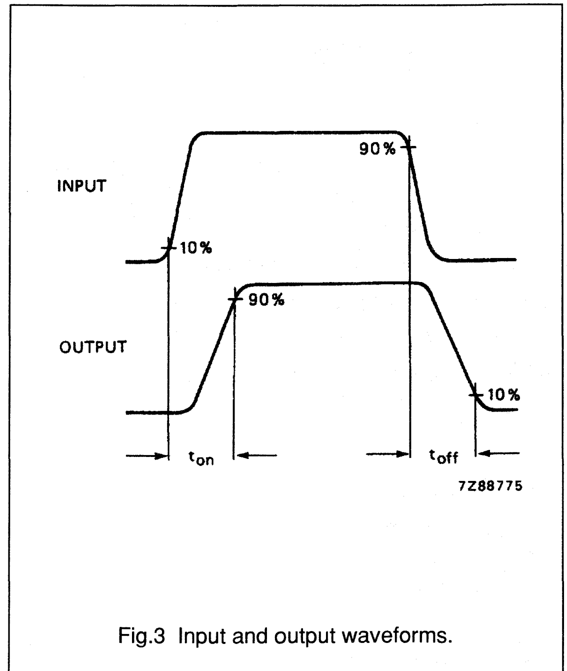


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BSS89

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Line current interruptor in telephone sets
- Relay, high-speed and line transformer drivers.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant package.

PINNING - TO-92 variant

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source

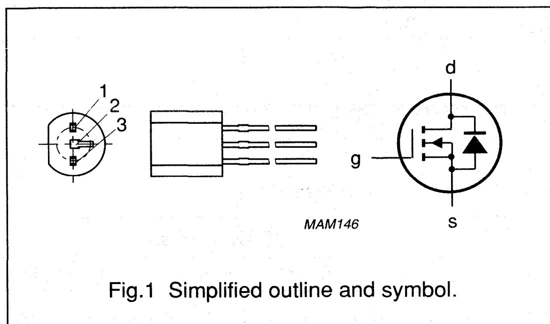


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–	240	V
V_{GSO}	gate-source voltage (DC)	open drain	–	–	±20	V
I_D	drain current (DC)		–	–	300	mA
P_{tot}	total power dissipation	up to $T_{amb} \leq 25$ °C	–	–	1	W
R_{DSon}	drain-source on-state resistance	$I_D = 400$ mA; $V_{GS} = 10$ V	–	4.5	6	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	$I_D = 400$ mA; $V_{DS} = 25$ V	140	350	–	mS

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	240	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	300	mA
I_{DM}	peak drain current		–	1.2	A
P_{tot}	total power dissipation	T_{amb} ≤ 25 °C; note 1	–	1	W
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	125	K/W

Note to the Limiting values and Thermal characteristics

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for drain lead minimum 10 × 10 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 250 µA	240	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	0.8	–	2.8	V
I_{DSS}	drain-source leakage current	V_{DS} = 60 V; V_{GS} = 0	–	–	200	nA
		V_{DS} = 200 V; V_{GS} = 0	–	0.1	60	µA
I_{GSS}	gate leakage current	V_{DS} = 0; V_{GS} = ±20 V	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 400 mA	–	4.5	6	Ω
$\|y_{fs}\|$	forward transfer admittance	I_D = 400 mA; V_{DS} = 25 V	140	350	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	45	–	pF
C_{oss}	output capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	15	–	pF
C_{rss}	reverse transfer capacitance	V_{DS} = 25 V; V_{GS} = 0; f = 1 MHz	–	3.5	–	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	V_{GS} = 0 to 10 V; V_{DD} = 50 V; I_D = 250 mA	–	5	–	ns
t_{off}	turn-off time	V_{GS} = 10 to 0 V; V_{DD} = 50 V; I_D = 250 mA	–	15	–	ns

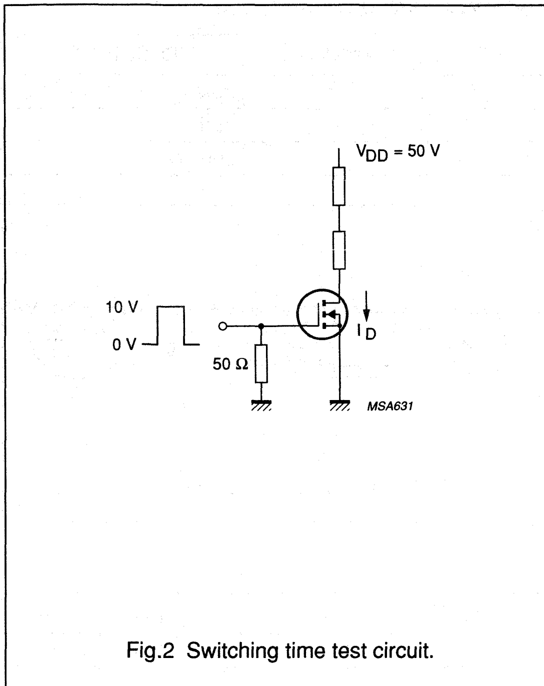


Fig.2 Switching time test circuit.

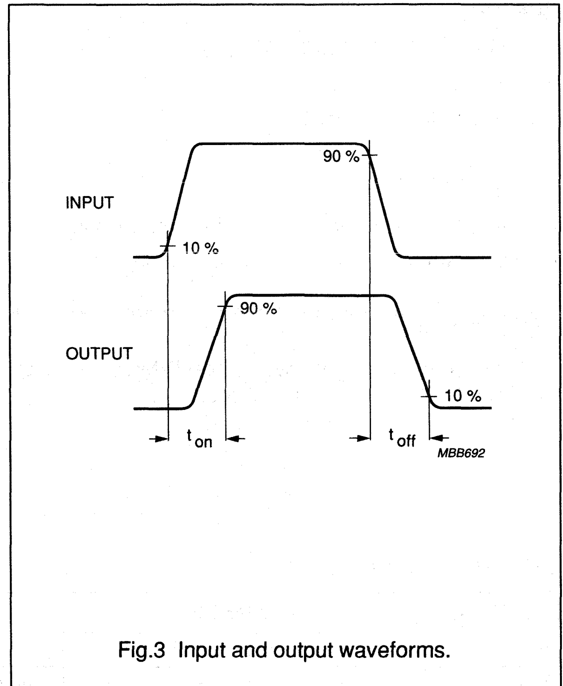


Fig.3 Input and output waveforms.

P-channel enhancement mode vertical D-MOS transistor

BSS92

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Line current interrupter in telephony applications
- Relay, high speed and line transformer drivers.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a TO-92 (SOT54) variant package.

PINNING - TO-92 (SOT54) variant

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source

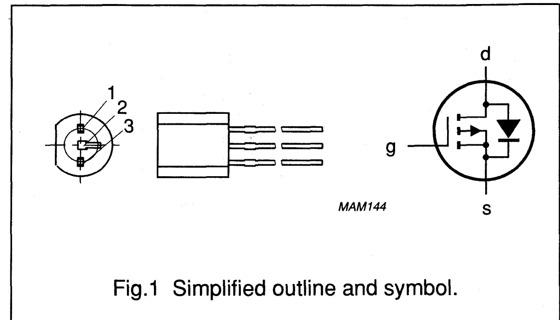


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–	–240	V
V_{GSO}	gate-source voltage (DC)	open drain	–	–	±20	V
I_D	drain current (DC)		–	–	–150	mA
R_{DSon}	drain-source on-state resistance	I_D = –100 mA; V_{GS} = –10 V	–	10	20	Ω
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	–	1	W
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = –25 V; I_D = –100 mA	60	200	–	mS

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–240	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	–150	mA
I_{DM}	peak drain current		–	–600	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	1	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	125	K/W

Note to the Limiting values and Thermal characteristics

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for drain lead minimum 10 mm × 10 mm.

CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = -250$ µA	–240	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = V_{GS}$; $I_D = -1$ mA	–0.8	–	–2.8	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = -60$ V	–	–	–200	nA
		$V_{GS} = 0$; $V_{DS} = -200$ V	–	–	–60	µA
I_{GSS}	gate leakage current	$V_{DS} = 0$; $V_{GS} = \pm 20$ V	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -10$ V; $I_D = -100$ mA	–	10	20	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	$V_{DS} = -25$ V; $I_D = -100$ mA	60	200	–	mS
C_{iss}	input capacitance	$V_{GS} = 0$; $V_{DS} = -25$ V; f = 1 MHz	–	65	–	pF
C_{oss}	output capacitance	$V_{GS} = 0$; $V_{DS} = -25$ V; f = 1 MHz	–	20	–	pF
C_{rss}	reverse transfer capacitance	$V_{GS} = 0$; $V_{DS} = -25$ V; f = 1 MHz	–	6	–	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$V_{GS} = 0$ to -10 V; $V_{DD} = -50$ V; $I_D = -250$ mA	–	5	–	ns
t_{off}	turn-off time	$V_{GS} = -10$ to 0 V; $V_{DD} = -50$ V; $I_D = -250$ mA	–	20	–	ns

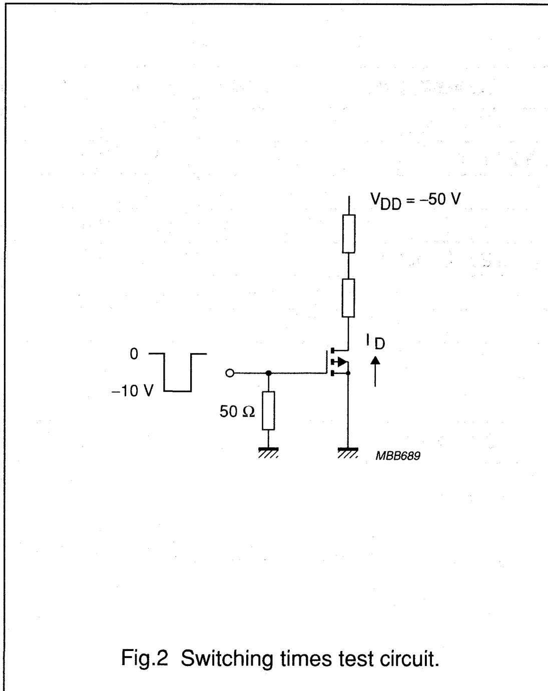


Fig.2 Switching times test circuit.

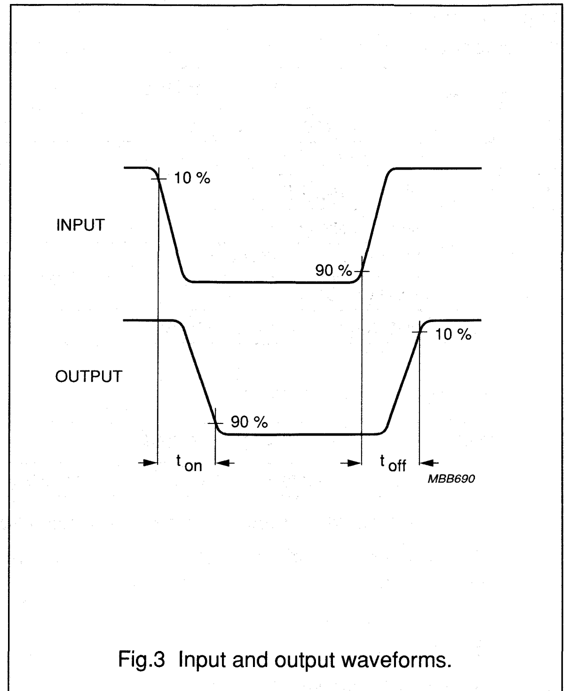


Fig.3 Input and output waveforms.

N-channel enhancement mode vertical D-MOS transistor

BSS123

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - SOT23

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		100	V
I_D	drain current	DC value	150	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 120 mA V_{GS} = 10 V	6	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	2.8	V

PIN CONFIGURATION

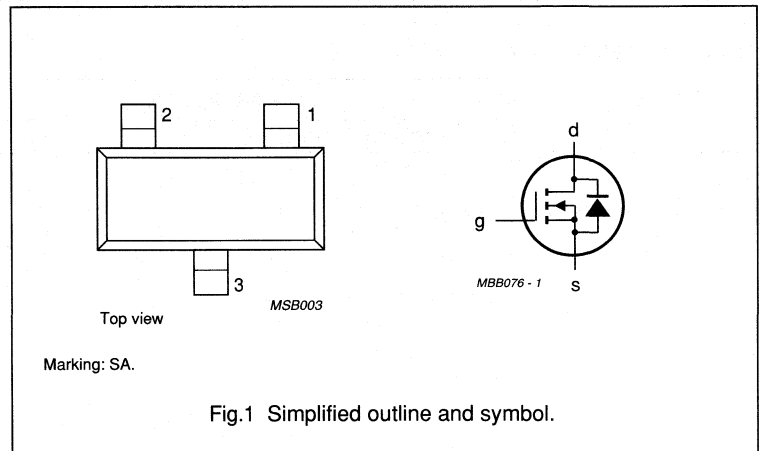


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	100	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	drain current	DC value	–	150	mA
I_{DM}	drain current	peak value	–	600	mA
P_{tot}	total power dissipation	up to T_{amb} = 25 °C	–	250	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500	K/W

Note

1. Device mounted on a FR4 printboard.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	100	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 60 V V_{GS} = 0	–	–	10	nA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 20 V V_{DS} = 0	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA $V_{GS} = V_{DS}$	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 120 mA V_{GS} = 10 V	–	3	6	Ω
$\|Y_{fs}\|$	transfer admittance	I_D = 120 mA V_{DS} = 25 V	80	140	–	mS
C_{iss}	input capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	24	40	pF
C_{oss}	output capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	15	25	pF
C_{rss}	feedback capacitance	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz	–	4	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	4	10	ns
t_{off}	turn-off time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	10	20	ns

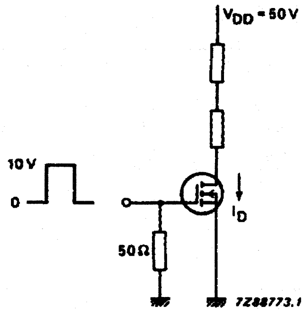


Fig.2 Switching time test circuit.

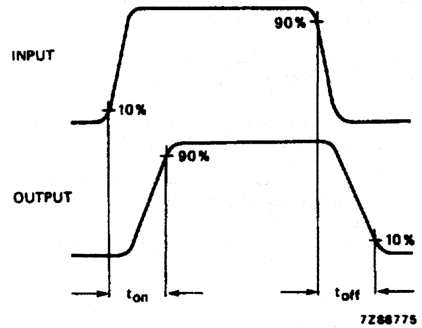


Fig.3 Input and output waveforms.

P-channel enhancement mode vertical D-MOS transistor

BSS192

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Line current interrupter in telephone sets
- Relay, high-speed and line transformer drivers.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a SOT89 package.

PINNING - SOT89

PIN	SYMBOL	DESCRIPTION
1	s	source
2	d	drain
3	g	gate

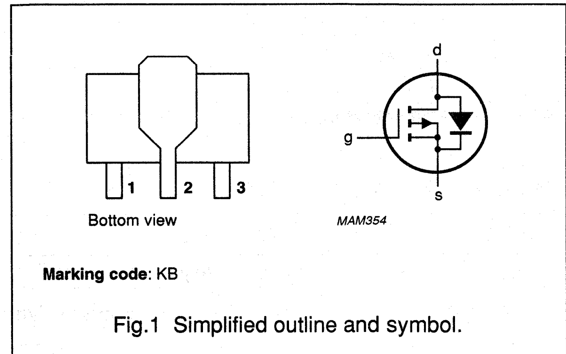


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		−240	V
V_{GSth}	gate-source threshold voltage	I_D = −1 mA; V_{GS} = V_{DS}	−2.8	V
I_D	drain current (DC)		−150	mA
R_{DSon}	drain-source on-state resistance	I_D = −100 mA; V_{GS} = −10 V	20	Ω

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–240	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	–150	mA
I_{DM}	peak drain current		–	–600	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	1	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	125	K/W

Note to the Limiting values and Thermal characteristics

1. Device mounted on a ceramic substrate; area 2.5 cm^2; thickness 0.7 mm.

CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = -10$ µA	–240	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{GS} = V_{DS}$; $I_D = -1$ mA	–0.8	–	–2.8	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = -60$ V	–	–	–200	nA
		$V_{GS} = -0.2$ V; $V_{DS} = -200$ V	–	–0.1	–60	µA
I_{GSS}	gate leakage current	$V_{DS} = 0$; $V_{GS} = \pm 20$ V	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -10$ V; $I_D = -100$ mA	–	10	20	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	$V_{DS} = -25$ V; $I_D = -200$ mA	60	200	–	mS
C_{iss}	input capacitance	$V_{GS} = 0$; $V_{DS} = -25$ V; f = 1 MHz	–	55	90	pF
C_{oss}	output capacitance	$V_{GS} = 0$; $V_{DS} = -25$ V; f = 1 MHz	–	20	30	pF
C_{rss}	reverse transfer capacitance	$V_{GS} = 0$; $V_{DS} = -25$ V; f = 1 MHz	–	5	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$V_{GS} = 0$ to -10 V; $V_{DD} = -50$ V; $I_D = -250$ mA	–	5	10	ns
t_{off}	turn-off time	$V_{GS} = -10$ to 0 V; $V_{DD} = -50$ V; $I_D = -250$ mA	–	20	30	ns

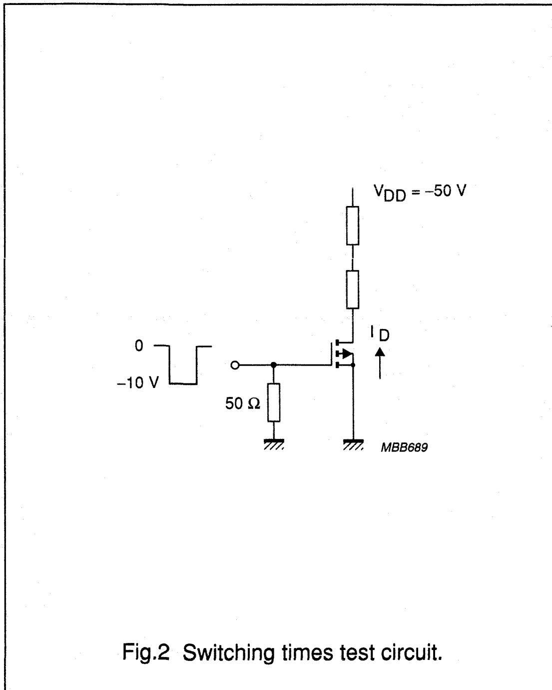


Fig.2 Switching times test circuit.

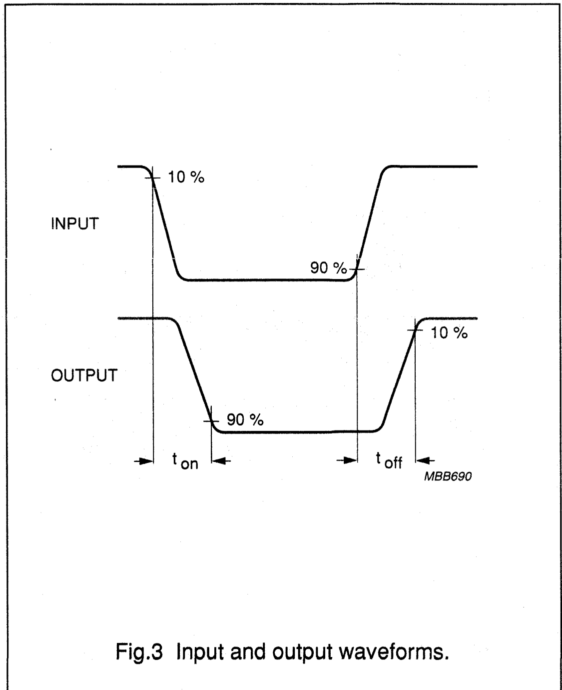


Fig.3 Input and output waveforms.

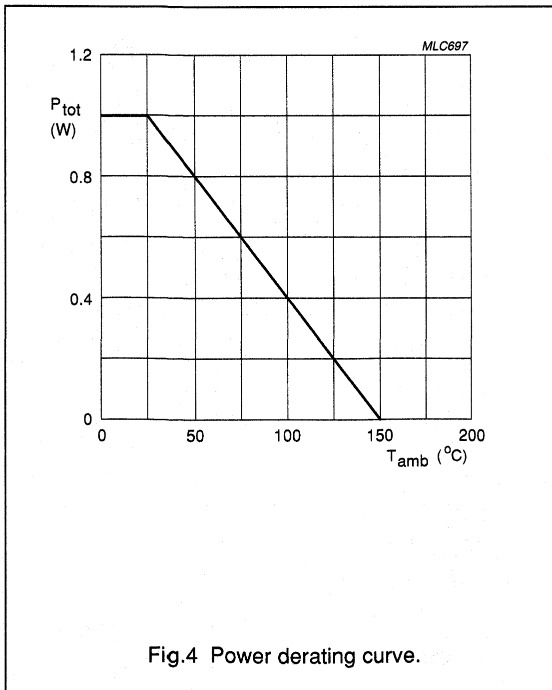
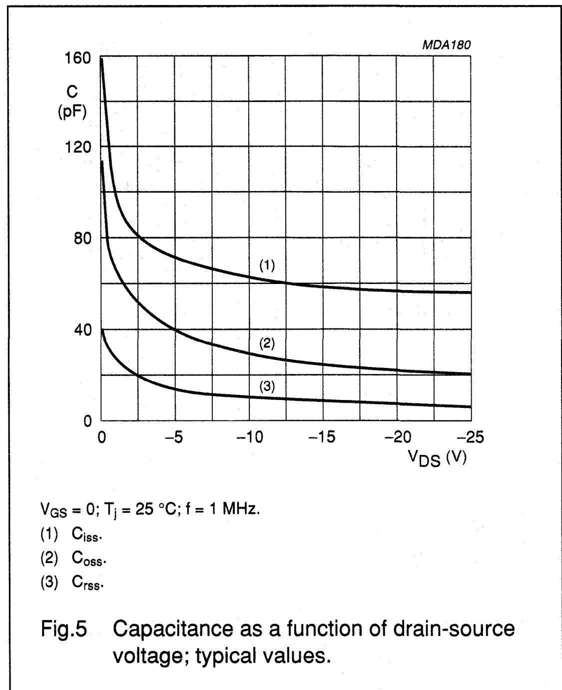


Fig.4 Power derating curve.



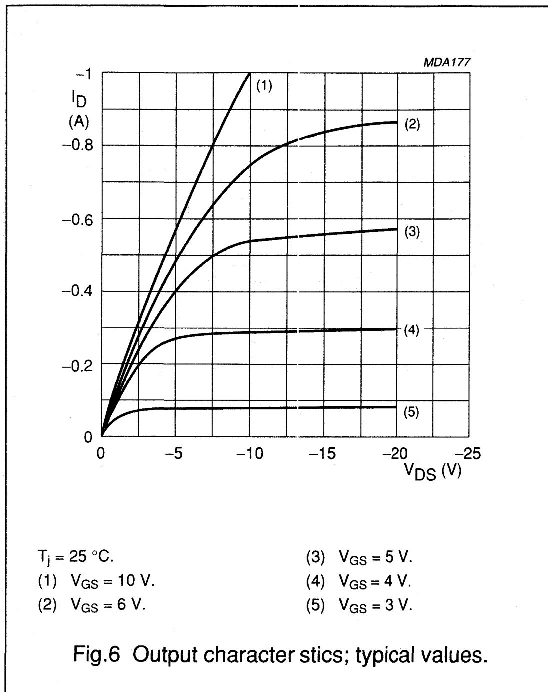
$V_{GS} = 0$; $T_j = 25$ °C; f = 1 MHz.

(1) C_{iss}.

(2) C_{oss}.

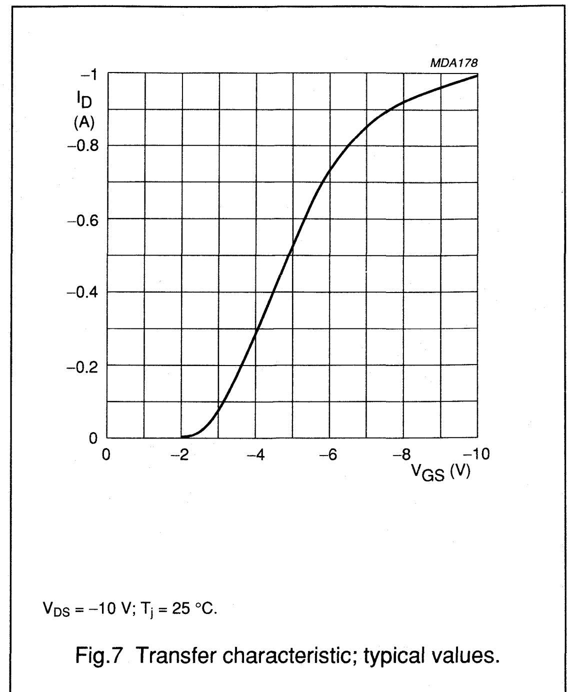
(3) C_{rss}.

Fig.5 Capacitance as a function of drain-source voltage; typical values.



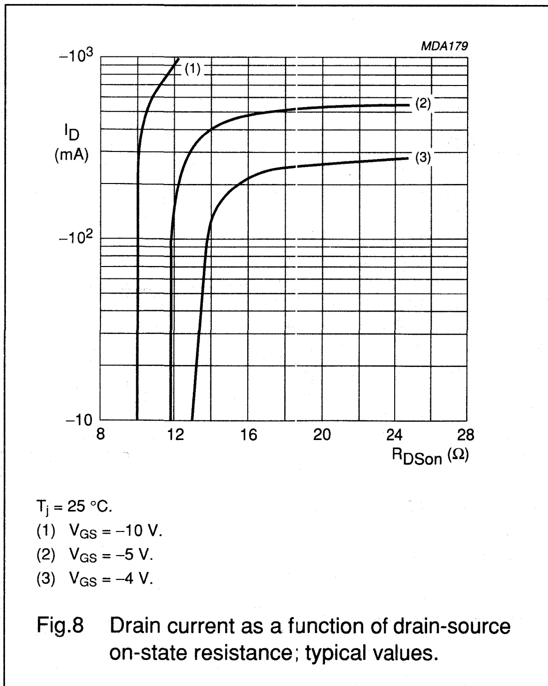
T_j = 25 °C.
(1) V_{GS} = 10 V.
(2) V_{GS} = 6 V.
(3) V_{GS} = 5 V.
(4) V_{GS} = 4 V.
(5) V_{GS} = 3 V.

Fig.6 Output characteristics; typical values.



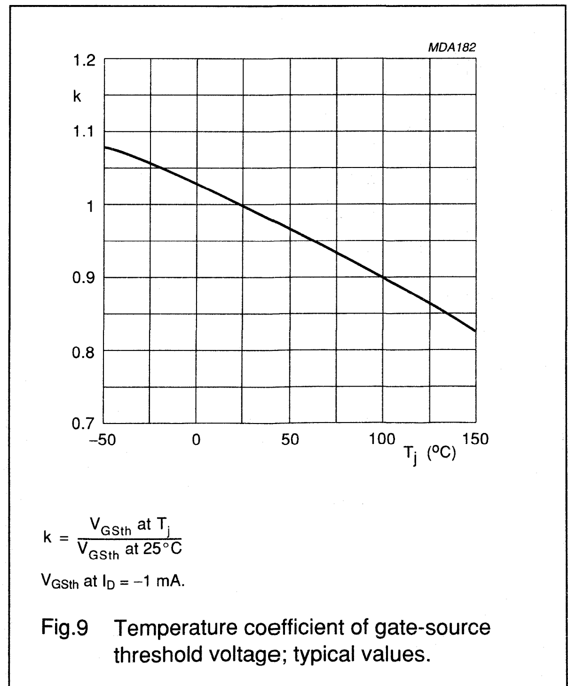
V_{DS} = −10 V; T_j = 25 °C.

Fig.7 Transfer characteristic; typical values.



T_j = 25 °C.
(1) V_{GS} = −10 V.
(2) V_{GS} = −5 V.
(3) V_{GS} = −4 V.

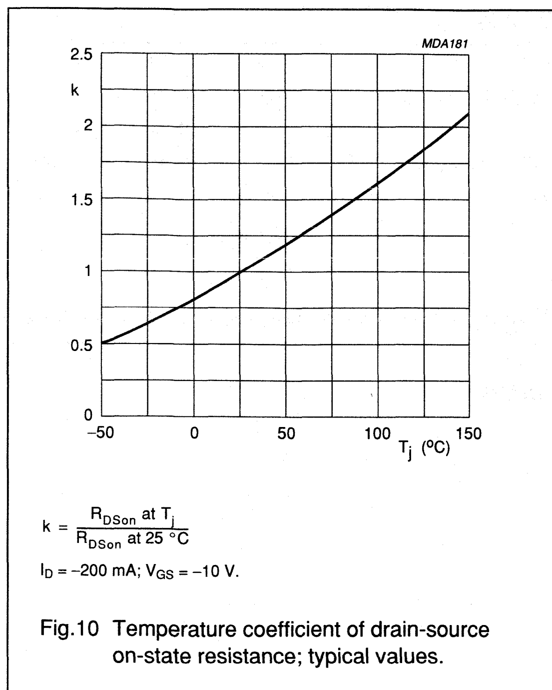
Fig.8 Drain current as a function of drain-source on-state resistance; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25\,°C}$$

V_{GSth} at I_D = −1 mA.

Fig.9 Temperature coefficient of gate-source threshold voltage; typical values.



$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$

$I_D = -200$ mA; $V_{GS} = -10$ V.

Fig.10 Temperature coefficient of drain-source on-state resistance; typical values.

N-channel vertical D-MOS transistor BST70A

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

FEATURES:

- Very low $R_{DS(on)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

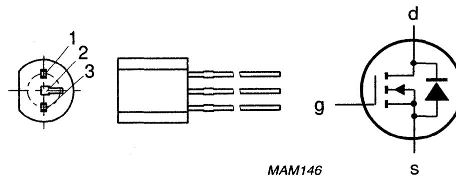
QUICK REFERENCE DATA

Parameter	Symbol		Value	Unit
Drain-source voltage	V_{DS}	max.	80	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (DC)	I_D	max.	0.5	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance				
I_D = 500 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	2	Ω
		max.	4	Ω
Transfer admittance				
I_D = 500 mA; V_{DS} = 15 V	$\lvert Y_{fs} \rvert$	typ.	300	mS

PINNING - TO-92 VARIANT

1 = source
2 = gate
3 = drain

PIN CONFIGURATION



Note: Various pinout configurations available.

Fig.1 Simplified outline and symbol.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (DC)	I_D	max.	0.5	A
Drain current (peak)	I_{DM}	max.	1.0	A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}		− 65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm × 10 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value	Unit
Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DS}$	min.	80	V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1	μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	1.5 3.5	V V
Drain-source ON-resistance (see Fig.4) I_D = 500 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ. max.	2.0 4.0	Ω Ω
Transfer admittance I_D = 500 mA; V_{DS} = 15 V	$\|Y_{fs}\|$	typ.	300	mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	45 60	pF pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	30 45	pF pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	8 12	pF pF
Switching times (see Figs 2 and 3) I_D = 500 mA; V_{DS} = 50 V; V_{GS} = 0 to 10 V	t_{on} t_{off}	max. max.	10 15	ns ns

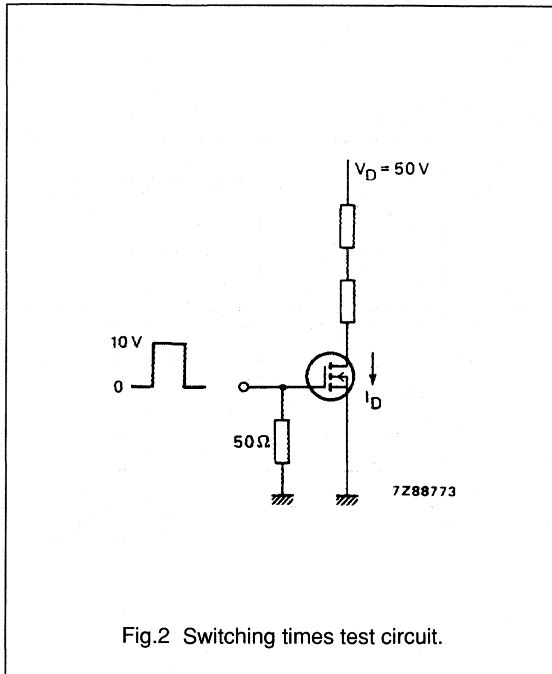


Fig.2 Switching times test circuit.

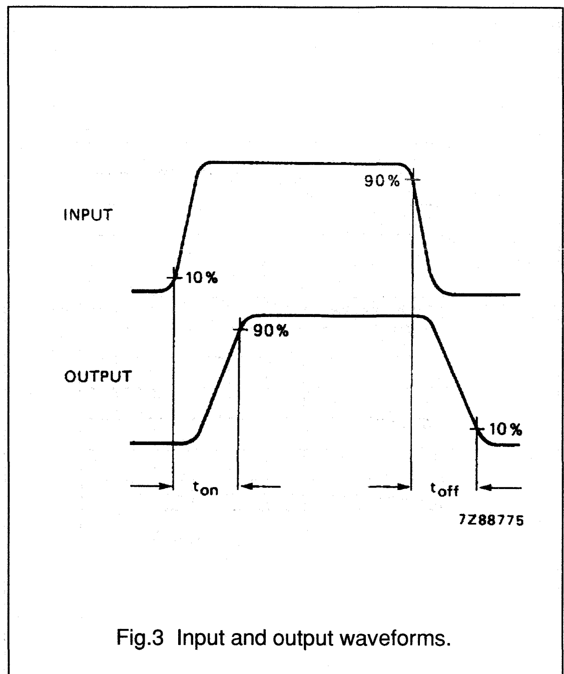


Fig.3 Input and output waveforms.

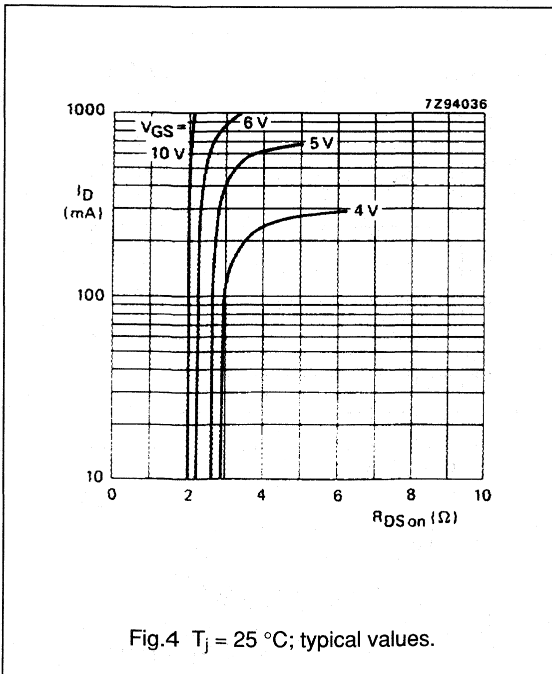


Fig.4 $T_j = 25$ °C; typical values.

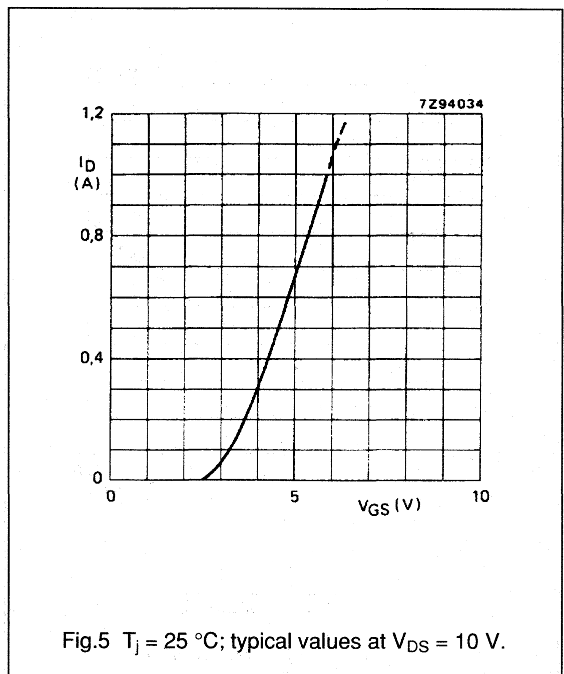


Fig.5 $T_j = 25$ °C; typical values at $V_{DS} = 10$ V.

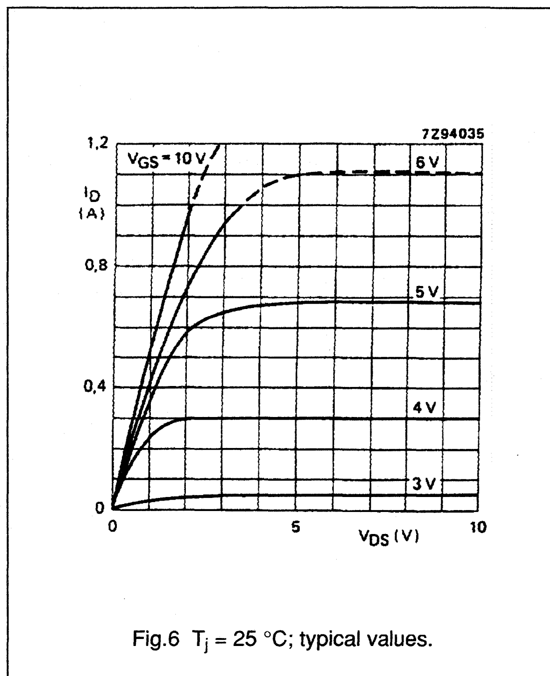


Fig.6 T_j = 25 °C; typical values.

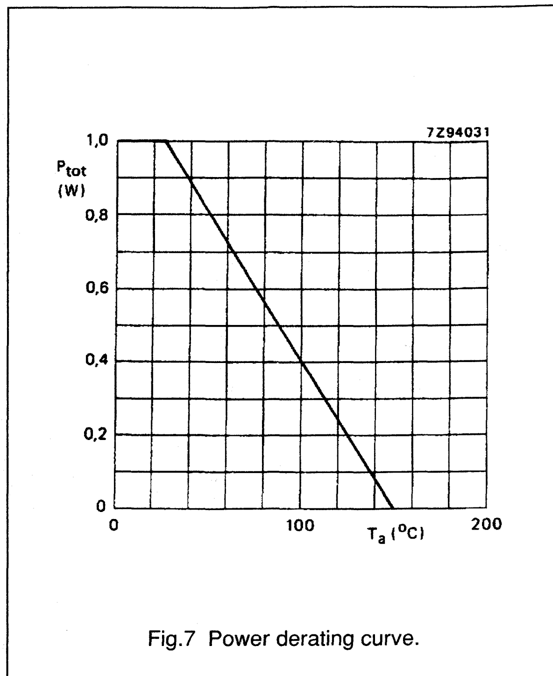


Fig.7 Power derating curve.

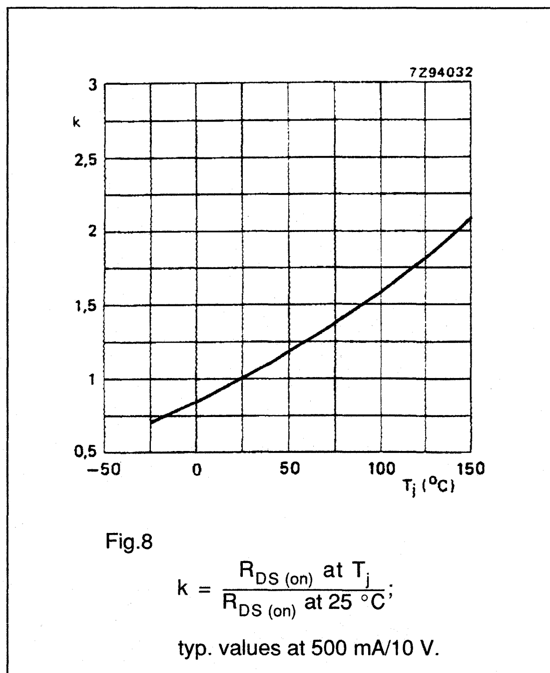


Fig.8

$$k = \frac{R_{DS\,(on)} \text{ at } T_j}{R_{DS\,(on)} \text{ at } 25\ °C};$$

typ. values at 500 mA/10 V.

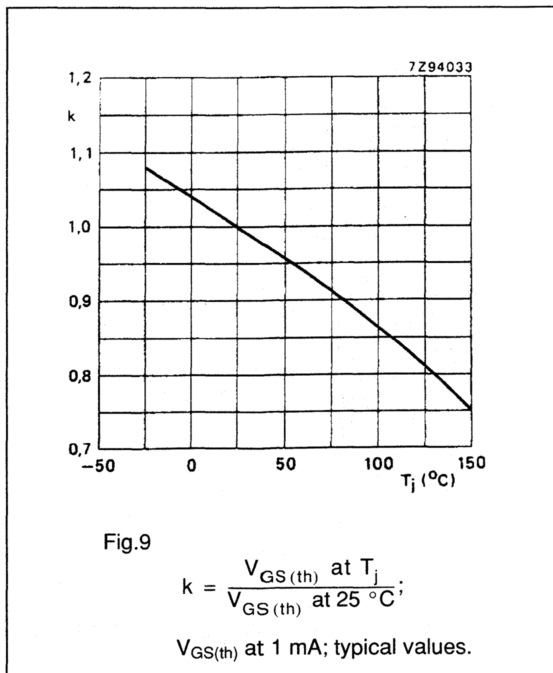


Fig.9

$$k = \frac{V_{GS\,(th)} \text{ at } T_j}{V_{GS\,(th)} \text{ at } 25\ °C};$$

$V_{GS(th)}$ at 1 mA; typical values.

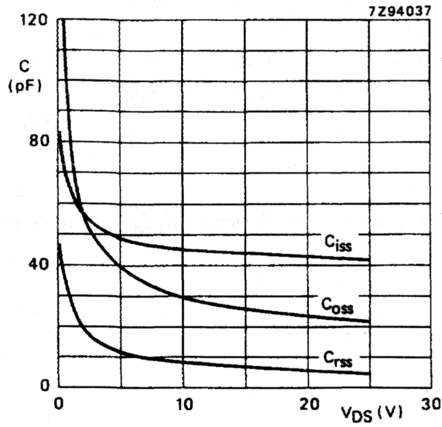


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-channel vertical D-MOS transistor BST72A

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use in telephone ringer circuits and for application with relay, high-speed and line-transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

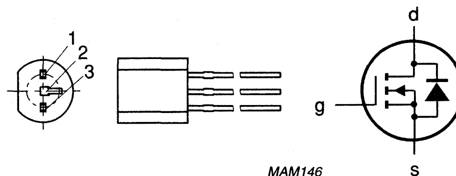
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Total power dissipation up to $T_{amb} = 25$ °C	P_{tot}	max.	0.83	W
Drain-source ON-resistance				
$I_D = 150$ mA; $V_{GS} = 5$ V	$R_{DS(on)}$	typ.	7	Ω
		max.	10	Ω
Transfer admittance				
$I_D = 200$ mA; $V_{DS} = 5$ V	$\lvert Y_{fs} \rvert$	typ.	150	mS

PINNING - TO-92 VARIANT

1 = source
2 = gate
3 = drain

PIN CONFIGURATION



Note: Various pinout configurations available.

Fig.1 Simplified outline and symbol.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Parameter	Symbol		Value	Unit
Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Drain current (peak)	I_{DM}	max.	600	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	0.83	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

Parameter	Symbol		Value	Unit
From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	150	K/W

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value	Unit
Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DS}$	min.	80	V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1.0	μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min. max.	1.5 3.5	V V
Drain-source ON-resistance (see Fig.4) I_D = 150 mA; V_{GS} = 5 V	$R_{DS(on)}$	typ. max.	7 10	Ω Ω
Transfer admittance I_D = 200 mA; V_{DS} = 5 V	$\|Y_{fs}\|$	typ.	150	mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	15 30	pF pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	13 20	pF pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	3 6	pF pF
Switching times (see Figs 2 and 3) I_D = 200 mA; V_{DS} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ. max.	4 10	ns ns
	t_{off}	typ. max.	4 10	ns ns

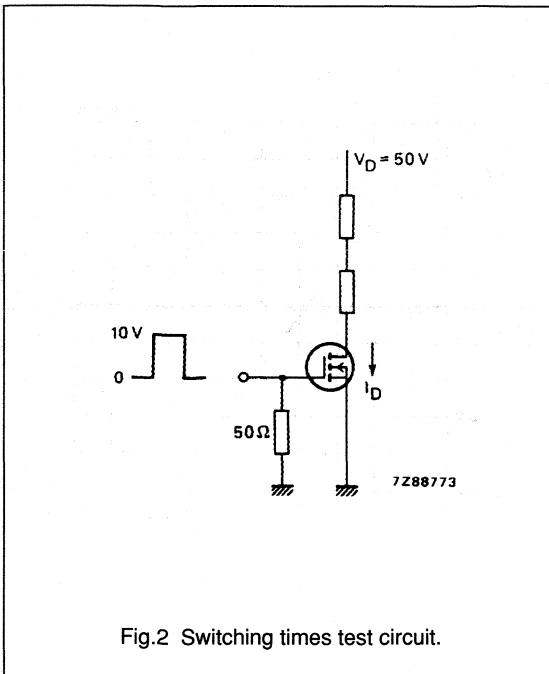


Fig.2 Switching times test circuit.

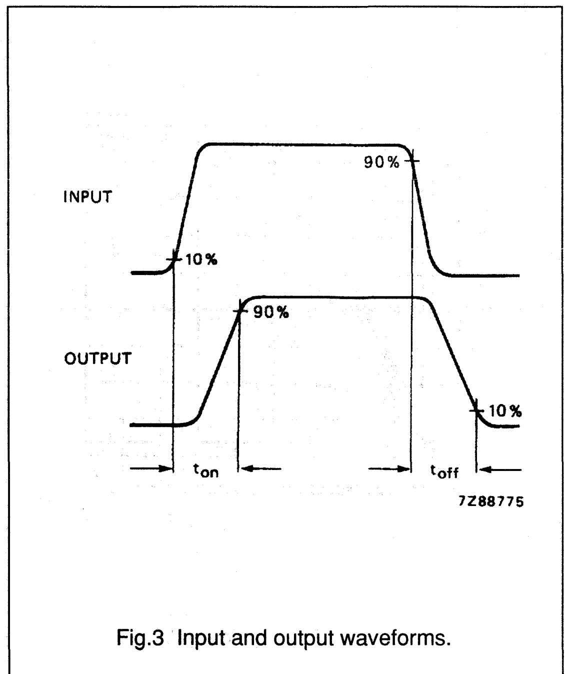


Fig.3 Input and output waveforms.

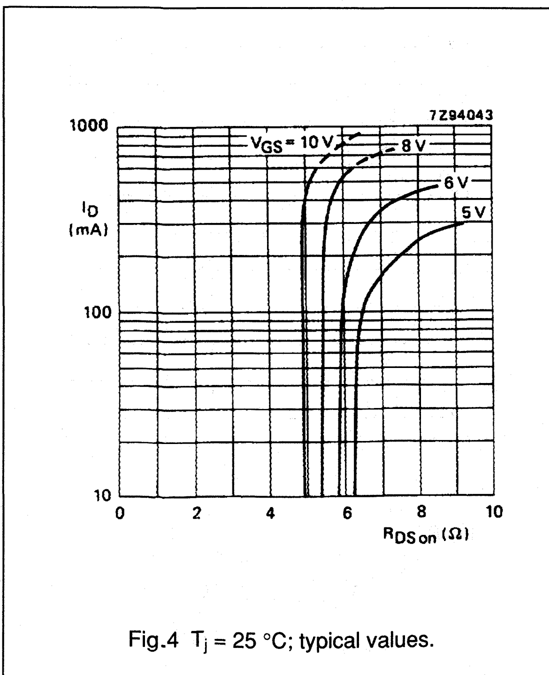


Fig.4 T_j = 25 °C; typical values.

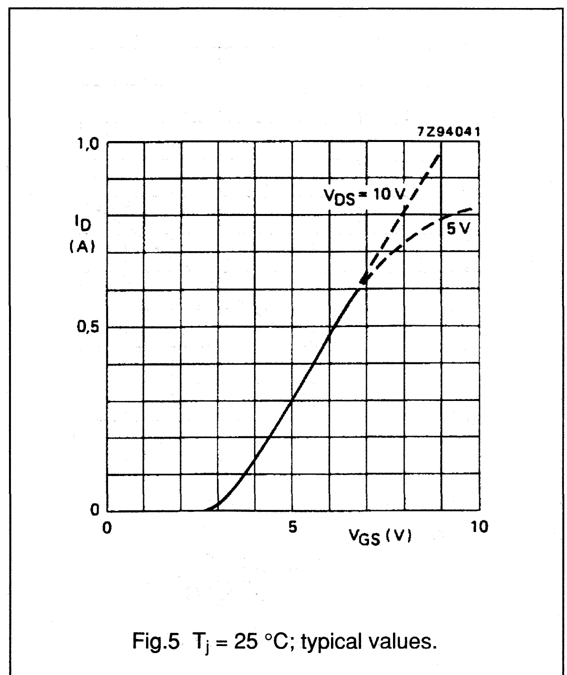


Fig.5 T_j = 25 °C; typical values.

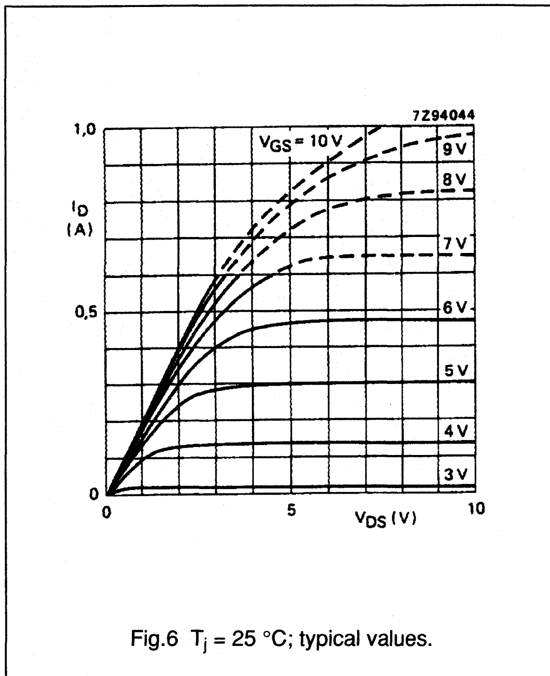


Fig.6 T_j = 25 °C; typical values.

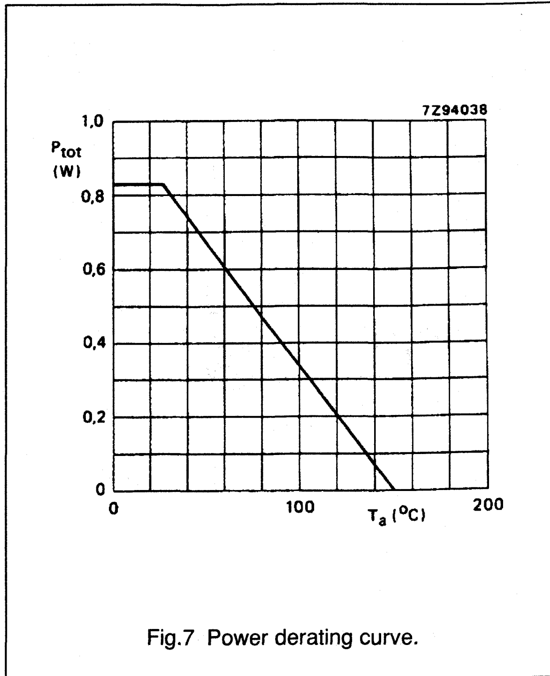


Fig.7 Power derating curve.

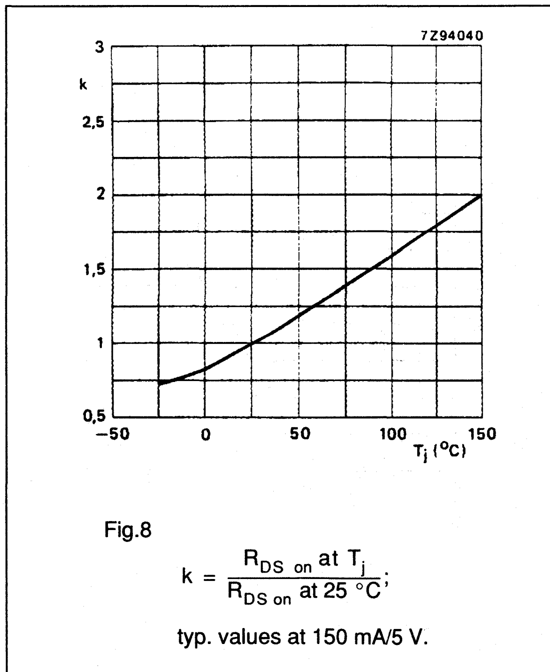


Fig.8

$$k = \frac{R_{DS\ on} \text{ at } T_j}{R_{DS\ on} \text{ at } 25\ °C};$$

typ. values at 150 mA/5 V.

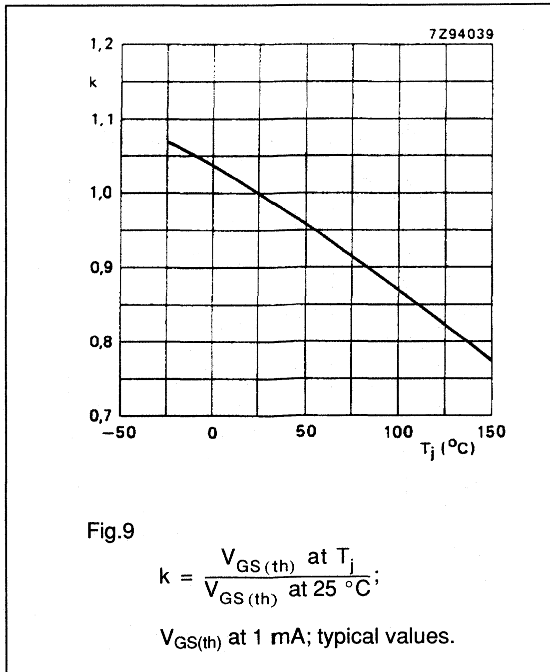


Fig.9

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C};$$

$V_{GS(th)}$ at 1 mA; typical values.

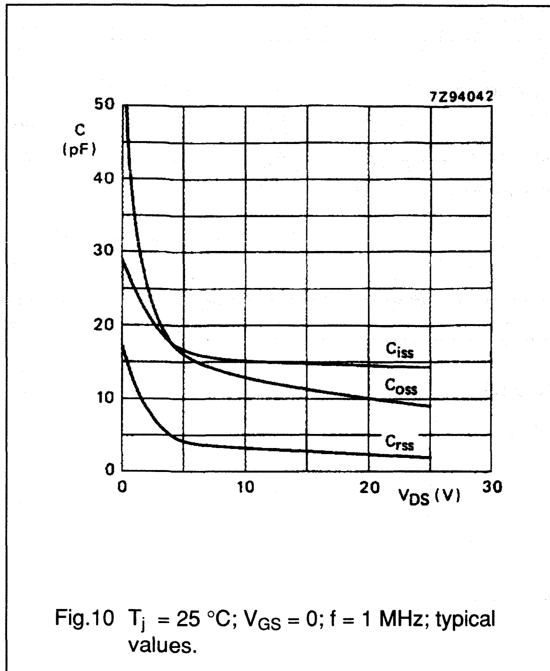


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-channel vertical D-MOS transistor — BST74A

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

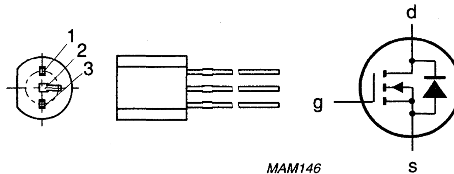
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance				
I_D = 250 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	6	Ω
		max.	12	Ω
Transfer admittance				
I_D = 250 mA; V_{DS} = 15 V	$\lvert Y_{fs} \rvert$	typ.	250	mS

PINNING - TO-92 VARIANT

1 = source
2 = gate
3 = drain

PIN CONFIGURATION



Note: Various pinout configurations available.

Fig.1 Simplified outline and symbol.

N-channel vertical D-MOS transistor　BST74A

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Parameter	Symbol		Value	Unit
Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	V_{GSO}	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Drain current (peak)	I_{DM}	max.	800	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}		−65 to +150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

Parameter	Symbol		Value	Unit
From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

Note

1. Transistor mounted on printed circuit board, max. lead length 4 mm, mounting pad for collector lead min. 10 mm × 10 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value	Unit
Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DS}$	min.	200	V
Drain-source leakage current V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	max.	10	μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.8	V
		max.	2.8	V
Drain-source ON-resistance (see Fig.4) I_D = 250 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	6	Ω
		max.	12	Ω
Transfer admittance I_D = 250 mA; V_{DS} = 15 V	$\|Y_{fs}\|$	typ.	250	mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ.	70	pF
		max.	90	pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ.	20	pF
		max.	30	pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ.	5	pF
		max.	10	pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DS} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	4	ns
		max.	10	ns
	t_{off}	typ.	15	ns
		max.	25	ns

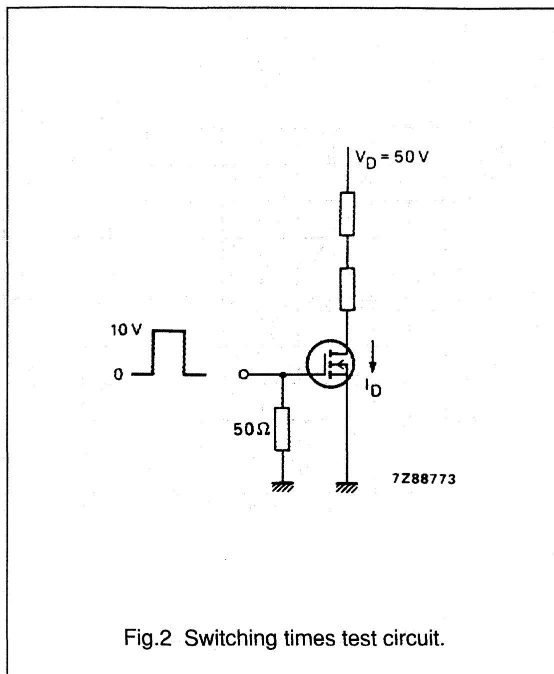


Fig.2 Switching times test circuit.

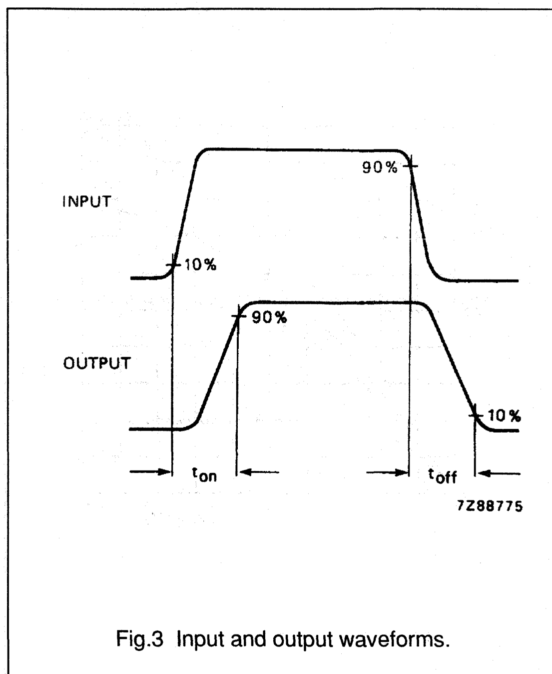


Fig.3 Input and output waveforms.

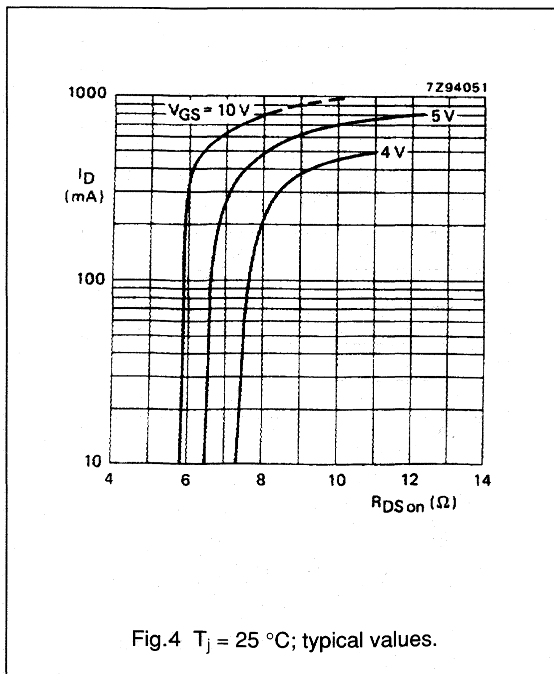


Fig.4 $T_j = 25\ °C$; typical values.

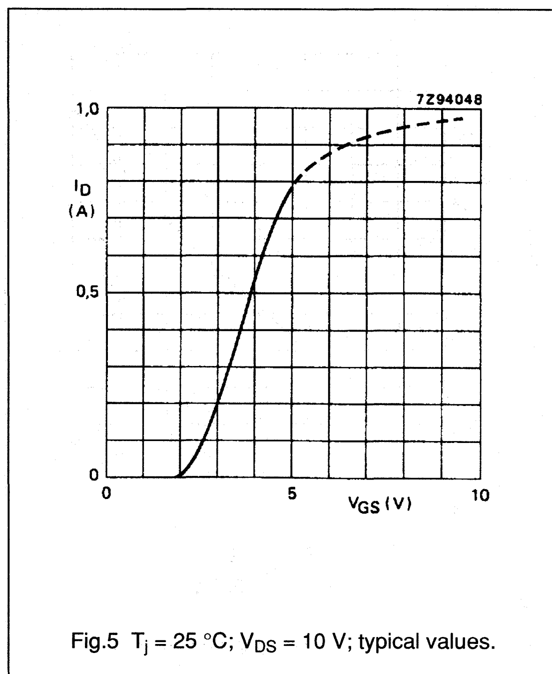


Fig.5 $T_j = 25\ °C$; $V_{DS} = 10\ V$; typical values.

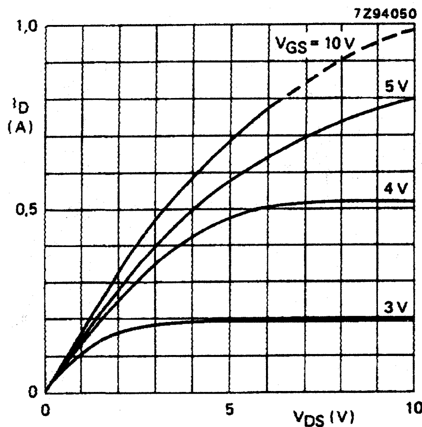


Fig.6 T_j = 25 °C; typical values.

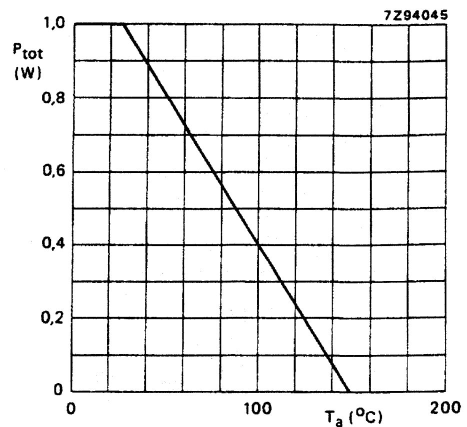


Fig.7 Power derating curve.

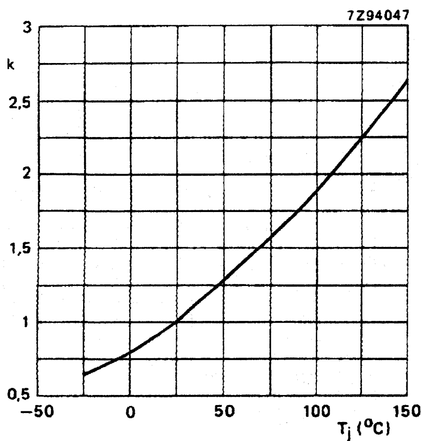


Fig.8

$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C};$$

at 400 mA/10 V; typical values.

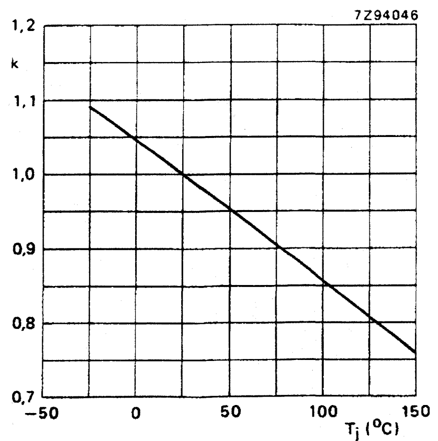


Fig.9

$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25\ °C};$$

$V_{GS(th)}$ at 1 mA; typical values.

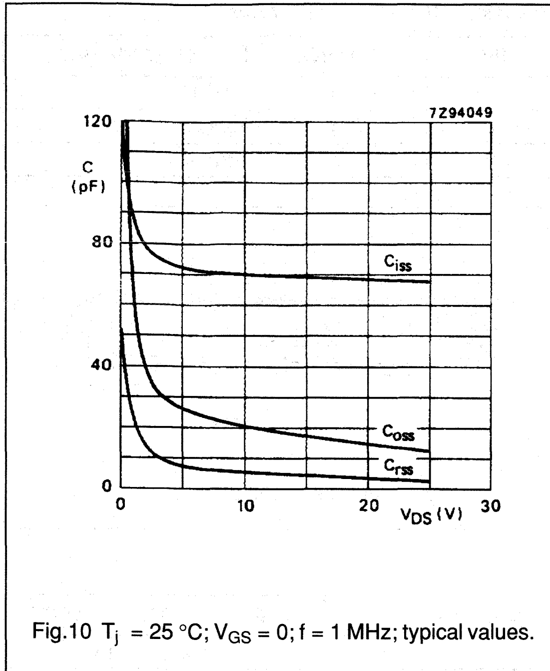


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-channel enhancement mode vertical D-MOS transistor

BST76A

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Line current interrupter in telephone sets
- Relay, high-speed and line transformer drivers.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT54 (TO-92) variant package.

PINNING - SOT54 (TO-92) variant

PIN	SYMBOL	DESCRIPTION
1	s	source
2	g	gate
3	d	drain

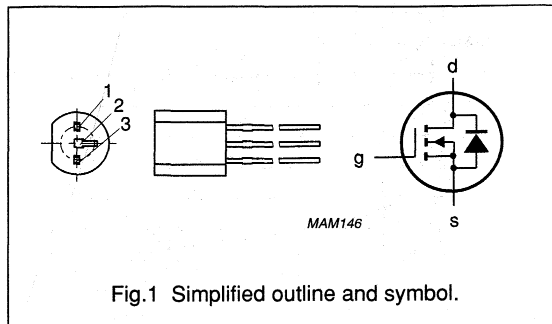


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	180	V
$V_{DS(SM)}$	drain-source voltage	non-repetitive peak; $t_p \leq 2$ mS	–	200	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	300	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	1	W
R_{DSon}	drain-source on-state resistance	$I_D = 15$ mA; $V_{GS} = 3$ V	7	10	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	$I_D = 300$ mA; $V_{DS} = 15$ V	250	–	mS

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	180	V
$V_{DS(SM)}$	drain-source voltage	non-repetitive peak; $t_p \leq 2$ mS	–	200	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	300	mA
I_{DM}	peak drain current		–	800	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	1	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	125	K/W

Note to the Limiting values and Thermal characteristics

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for drain lead minimum 10 mm × 10 mm.

CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = 100$ µA	180	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = V_{GS}$; $I_D = 100$ µA	0.7	–	2.4	V
I_{DSS}	drain-source leakage current	$V_{DS} = 120$ V; $V_{GS} = 0$	–	–	10	µA
I_{GSS}	gate leakage current	$V_{DS} = 0$; $V_{GS} = \pm 20$ V	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 3$ V; $I_D = 15$ mA	–	7	10	Ω
		$V_{GS} = 10$ V; $I_D = 300$ mA	–	6	–	Ω
$\|y_{fs}\|$	forward transfer admittance	$I_D = 300$ mA; $V_{DS} = 15$ V	–	250	–	mS
C_{iss}	input capacitance	$V_{DS} = 10$ V; $V_{GS} = 0$; f = 1 MHz	–	50	65	pF
C_{oss}	output capacitance	$V_{DS} = 10$ V; $V_{GS} = 0$; f = 1 MHz	–	20	30	pF
C_{rss}	reverse transfer capacitance	$V_{DS} = 10$ V; $V_{GS} = 0$; f = 1 MHz	–	6	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$V_{GS} = 0$ to 10 V; $V_{DS} = 50$ V; $I_D = 300$ mA	–	–	10	ns
t_{off}	turn-off time	$V_{GS} = 10$ to 0 V; $V_{DS} = 50$ V; $I_D = 300$ mA	–	–	15	ns

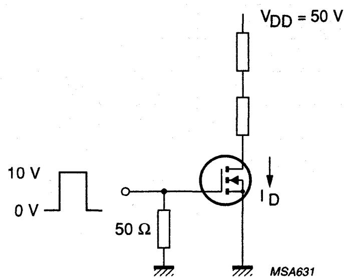


Fig.2 Switching times test circuit.

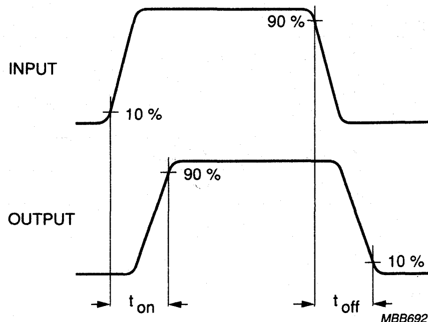


Fig.3 Input and output waveforms.

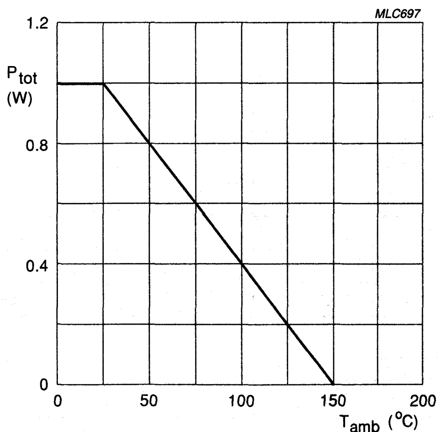
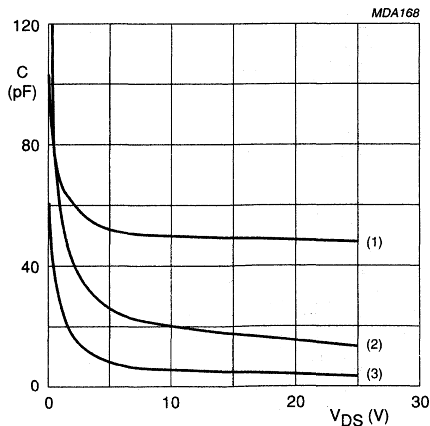


Fig.4 Power derating curve.



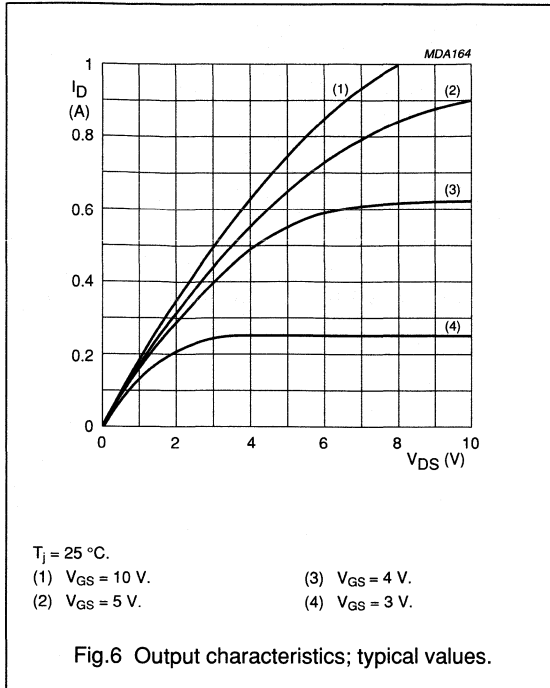
V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

(1) C_{iss}.

(2) C_{oss}.

(3) C_{rss}.

Fig.5 Capacitance as a function of drain-source voltage; typical values.



T_j = 25 °C.

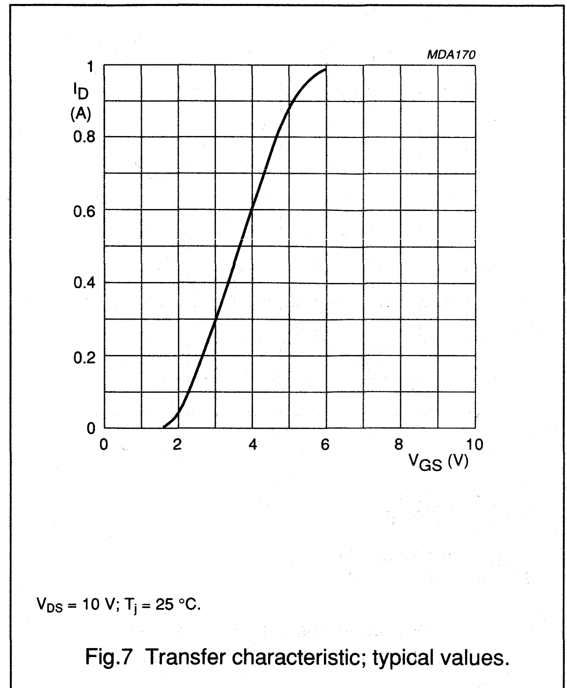
(1) V_{GS} = 10 V.

(2) V_{GS} = 5 V.

(3) V_{GS} = 4 V.

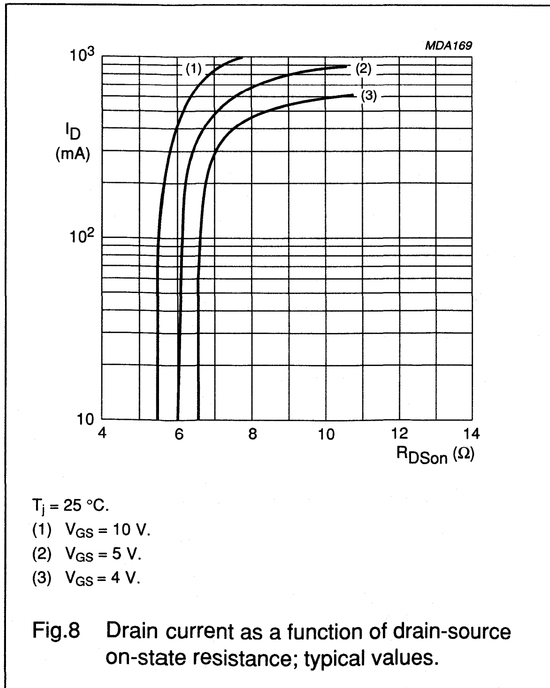
(4) V_{GS} = 3 V.

Fig.6 Output characteristics; typical values.



V_{DS} = 10 V; T_j = 25 °C.

Fig.7 Transfer characteristic; typical values.



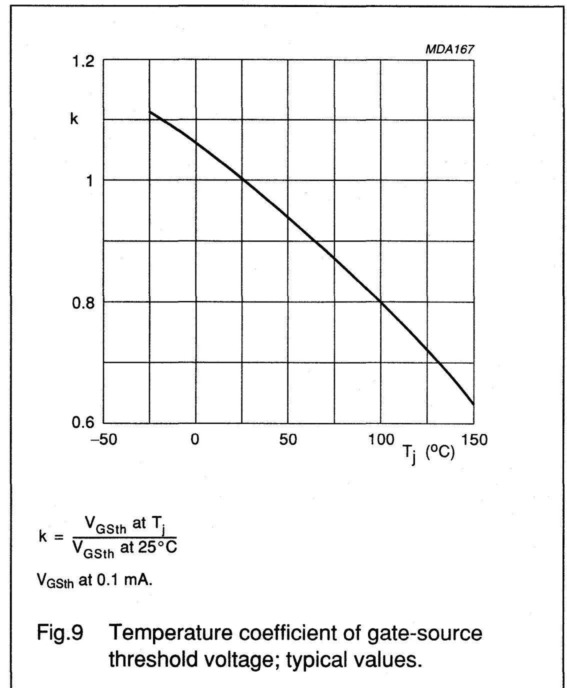
T_j = 25 °C.

(1) V_{GS} = 10 V.

(2) V_{GS} = 5 V.

(3) V_{GS} = 4 V.

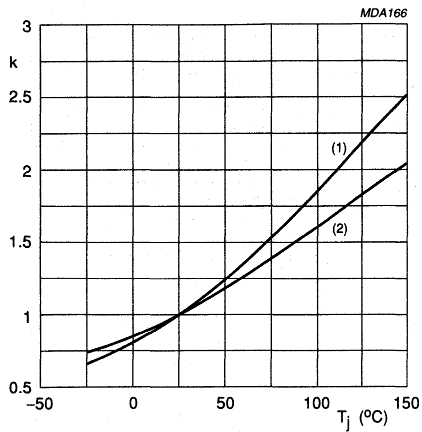
Fig.8 Drain current as a function of drain-source on-state resistance; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25\,°C}$$

V_{GSth} at 0.1 mA.

Fig.9 Temperature coefficient of gate-source threshold voltage; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

(1) I_D = 300 mA; V_{GS} = 10 V.

(2) I_D = 15 mA; V_{GS} = 3 V.

Fig.10 Temperature coefficient of drain-source on-state resistance; typical values.

N-channel enhancement mode vertical D-MOS transistor

BST80

FEATURES

- Low drain-source on-state resistance
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Thin and thick film circuits
- Relay, high-speed and line transformer drivers.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT89 package.

PINNING - SOT89

PIN	SYMBOL	DESCRIPTION
1	s	source
2	d	drain
3	g	gate

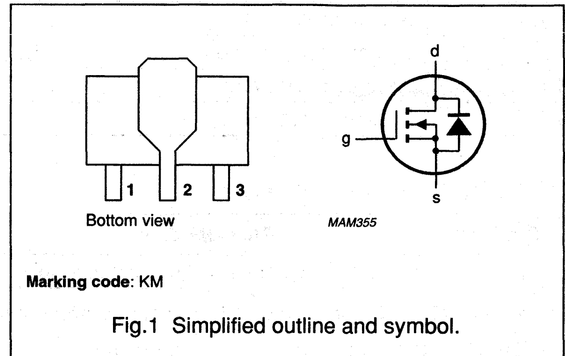


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	80	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	500	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	1	W
R_{DSon}	drain-source on-state resistance	$I_D = 500$ mA; $V_{GS} = 10$ V	2	3	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	$I_D = 500$ mA; $V_{DS} = 15$ V	300	–	mS

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	80	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	500	mA
I_{DM}	peak drain current		–	1	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	1	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	125	K/W

Note to the Limiting values and Thermal characteristics

1. Device mounted on a ceramic substrate; area 2.5 cm^2; thickness 0.7 mm.

CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = 10$ µA	80	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1$ mA	1.5	–	3.5	V
I_{DSS}	drain-source leakage current	$V_{DS} = 60$ V; $V_{GS} = 0$	–	–	1	µA
I_{GSS}	gate leakage current	$V_{DS} = 0$; $V_{GS} = \pm 20$ V	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 500$ mA	–	2	3	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	$I_D = 500$ mA; $V_{DS} = 15$ V	–	300	–	mS
C_{iss}	input capacitance	$V_{DS} = 10$ V; $V_{GS} = 0$; f = 1 MHz	–	45	60	pF
C_{oss}	output capacitance	$V_{DS} = 10$ V; $V_{GS} = 0$; f = 1 MHz	–	30	45	pF
C_{rss}	reverse transfer capacitance	$V_{DS} = 10$ V; $V_{GS} = 0$; f = 1 MHz	–	8	12	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$V_{GS} = 0$ to 10 V; $V_{DD} = 50$ V; $I_D = 500$ mA	–	–	10	ns
t_{off}	turn-off time	$V_{GS} = 10$ to 0 V; $V_{DD} = 50$ V; $I_D = 500$ mA	–	–	15	ns

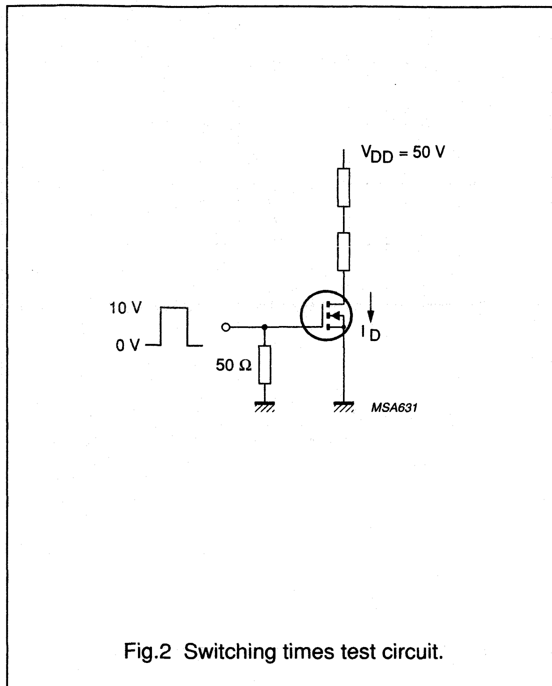


Fig.2 Switching times test circuit.

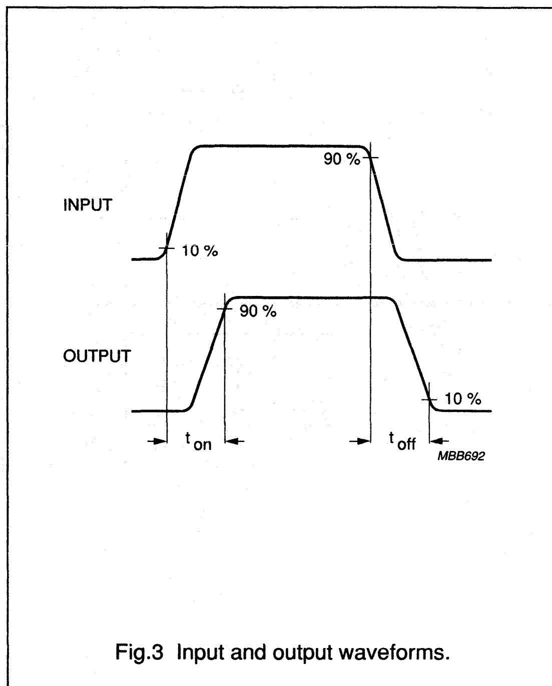


Fig.3 Input and output waveforms.

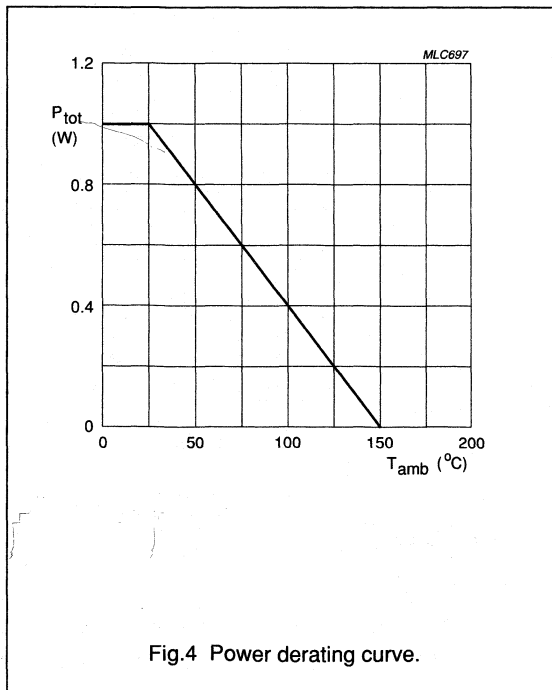
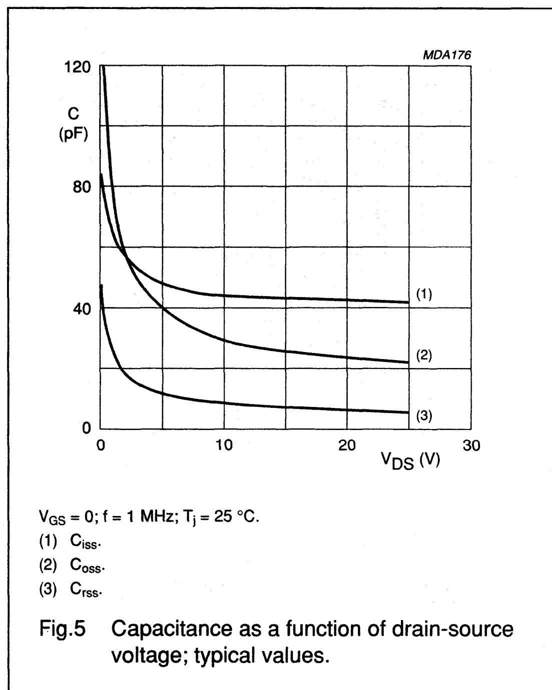


Fig.4 Power derating curve.



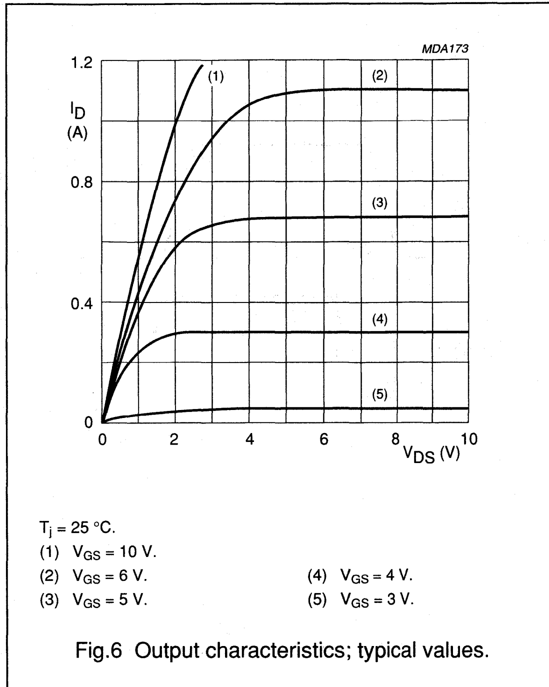
V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

(1) C_{iss}.

(2) C_{oss}.

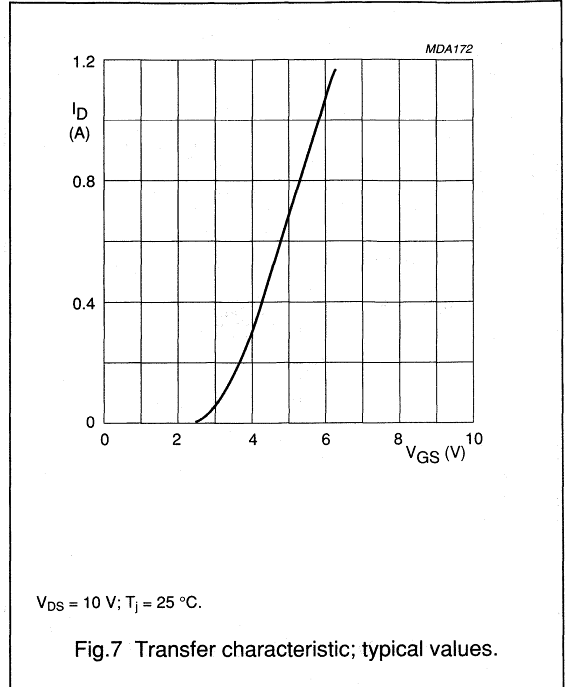
(3) C_{rss}.

Fig.5 Capacitance as a function of drain-source voltage; typical values.



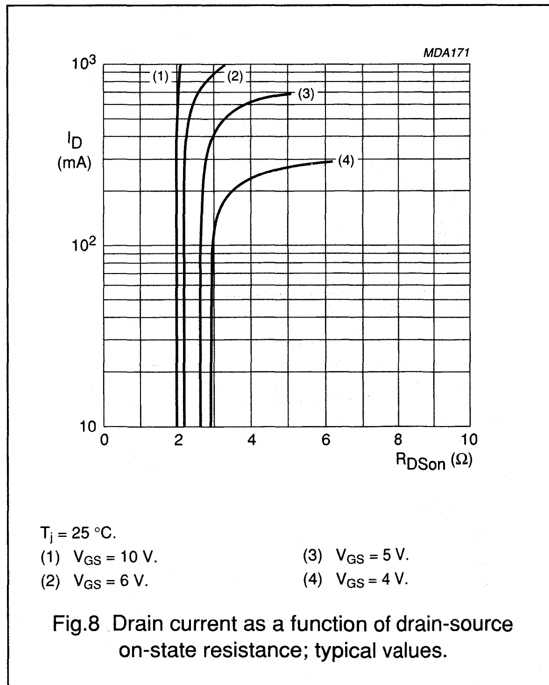
T_j = 25 °C.
(1) V_{GS} = 10 V.
(2) V_{GS} = 6 V.
(3) V_{GS} = 5 V.
(4) V_{GS} = 4 V.
(5) V_{GS} = 3 V.

Fig.6 Output characteristics; typical values.



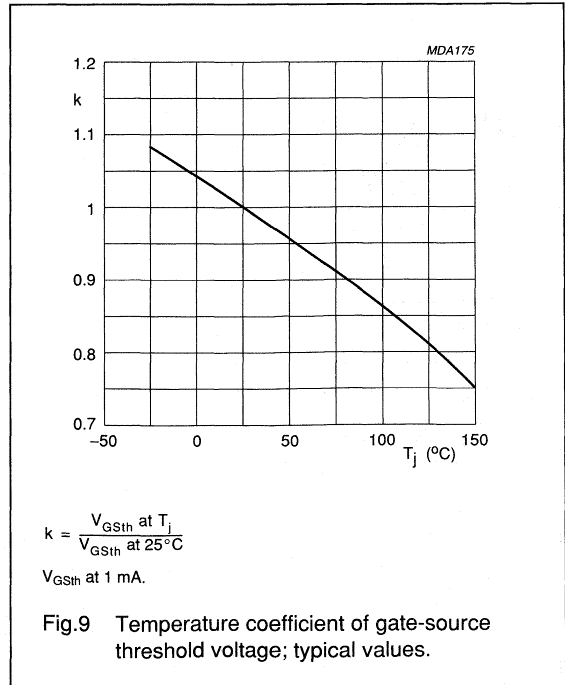
V_{DS} = 10 V; T_j = 25 °C.

Fig.7 Transfer characteristic; typical values.



T_j = 25 °C.
(1) V_{GS} = 10 V.
(2) V_{GS} = 6 V.
(3) V_{GS} = 5 V.
(4) V_{GS} = 4 V.

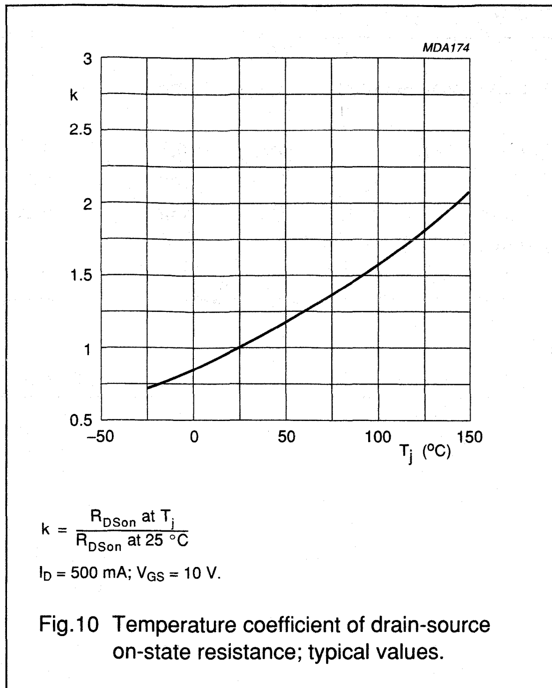
Fig.8 Drain current as a function of drain-source on-state resistance; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at 1 mA.

Fig.9 Temperature coefficient of gate-source threshold voltage; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

I_D = 500 mA; V_{GS} = 10 V.

Fig.10 Temperature coefficient of drain-source on-state resistance; typical values.

N-channel enhancement mode vertical D-MOS transistor

BST82

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in SOT23 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for telephone ringer and for application with relay, high-speed and line-transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low $R_{DS(on)}$

QUICK REFERENCE DATA

Parameter	Symbol		Value	Unit
Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	175	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Drain-source ON-resistance I_D = 150 mA; V_{GS} = 5 V	$R_{DS(on)}$	typ.	7	Ω
		max.	10	Ω
Transfer admittance I_D = 175 mA; V_{DS} = 5 V	$\|Y_{fs}\|$	typ.	150	mS

PINNING - SOT23

1 = gate
2 = source
3 = drain

PIN CONFIGURATION

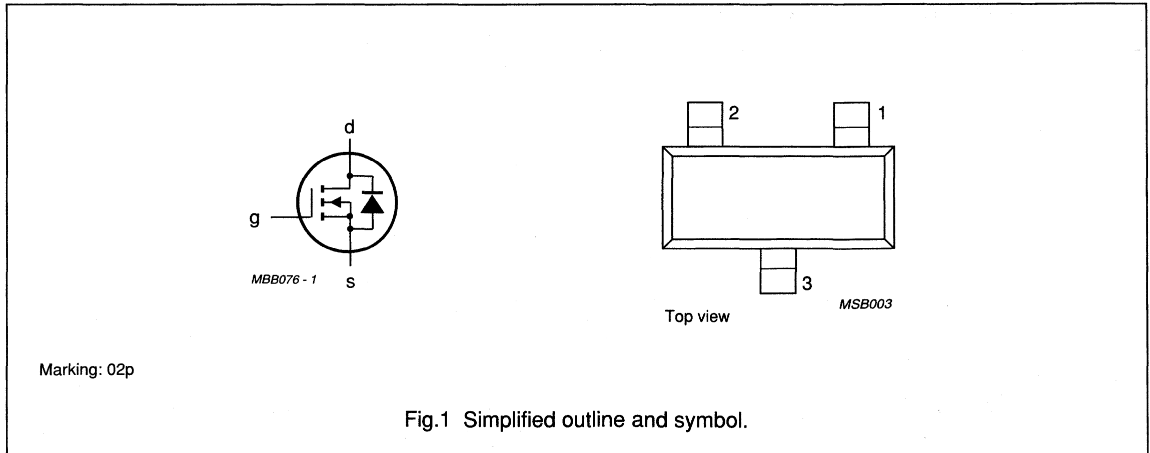


Fig.1 Simplified outline and symbol.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Parameter	Symbol		Value	Unit
Drain-source voltage	V_{DS}	max.	80	V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	175	mA
Drain current (peak)	I_{DM}	max.	600	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	300	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

Parameter	Symbol		Value	Unit
From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	430	K/W

Note

1. Transistors mounted on a ceramic substrate of 7 mm x 5 mm x 0.7 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value	Unit
Drain-source breakdown voltage I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	80	V
Drain-source leakage current V_{DS} = 60 V; V_{GS} = 0	I_{DSS}	max.	1.0	μA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate-source cut-off voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{(P)GS}$	min. max.	1.5 3.5	V V
Drain-source ON-resistance I_D = 150 mA; V_{GS} = 5 V	$R_{DS(on)}$	typ. max.	7 10	Ω Ω
Transfer admittance I_D = 175 mA; V_{DS} = 5 V	$\lvert Y_{fs} \rvert$	typ.	150	mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ. max.	15 30	pF pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ. max.	13 20	pF pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ. max.	3 6	pF pF
Switching times (see Figs 2 and 3) I_D = 175 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ. max.	4 10	ns ns
	t_{off}	typ. max.	4 10	ns ns

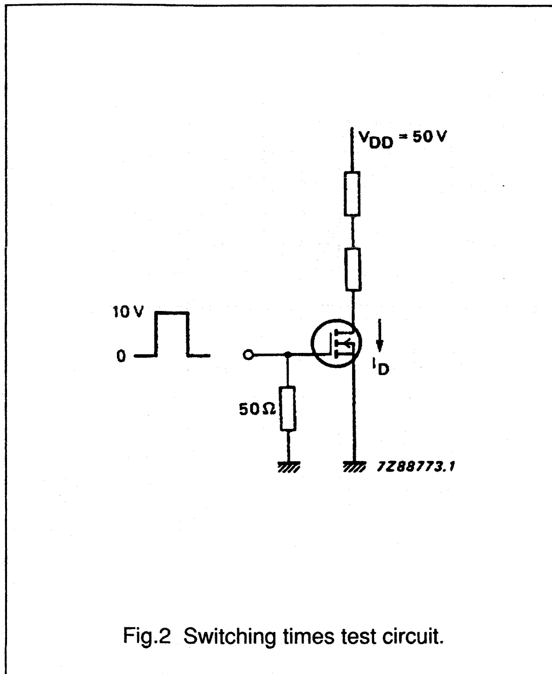


Fig.2 Switching times test circuit.

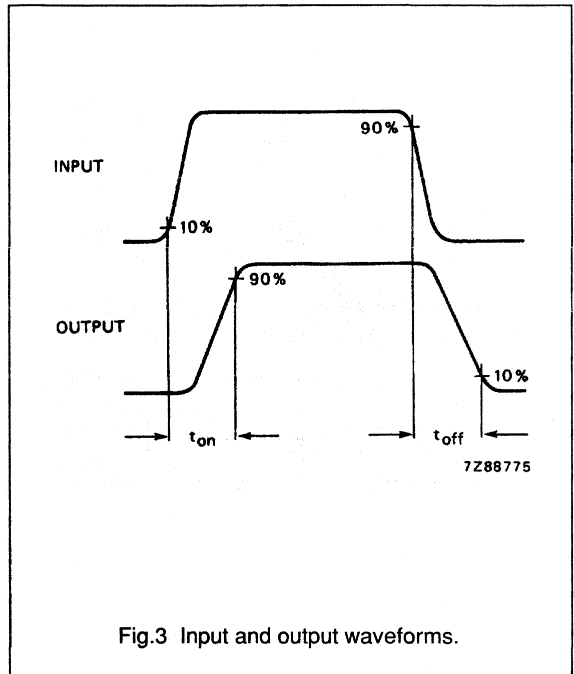


Fig.3 Input and output waveforms.

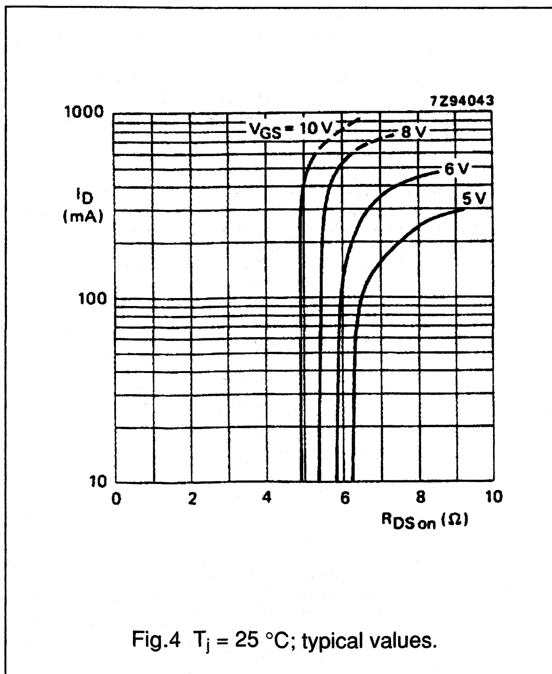


Fig.4 T_j = 25 °C; typical values.

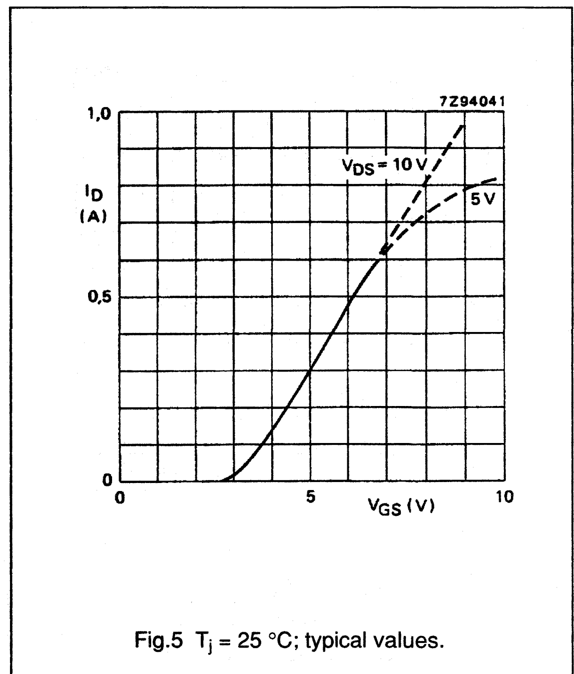


Fig.5 T_j = 25 °C; typical values.

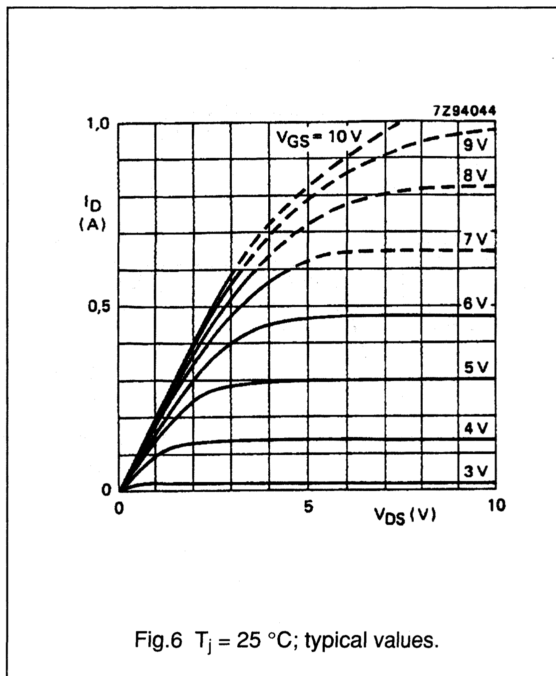


Fig.6 T_j = 25 °C; typical values.

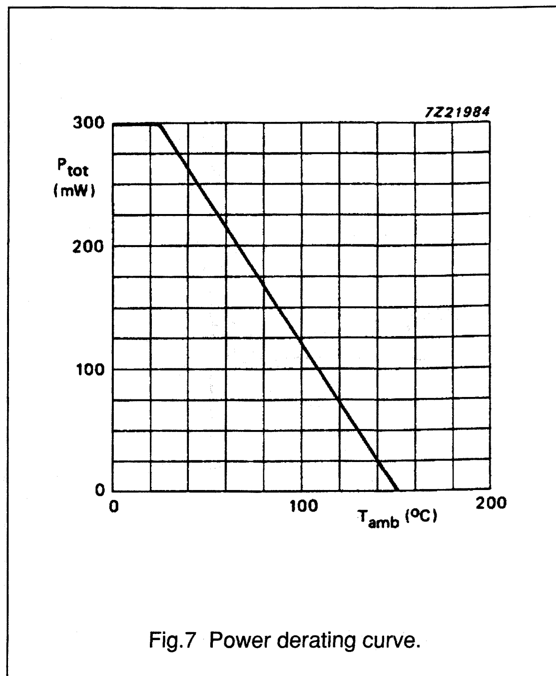


Fig.7 Power derating curve.

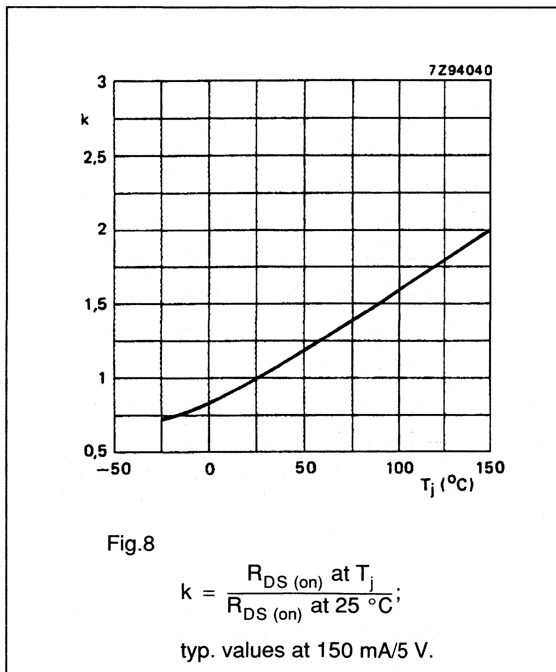


Fig.8

$$k = \frac{R_{DS\,(on)} \text{ at } T_j}{R_{DS\,(on)} \text{ at } 25\ °C};$$

typ. values at 150 mA/5 V.

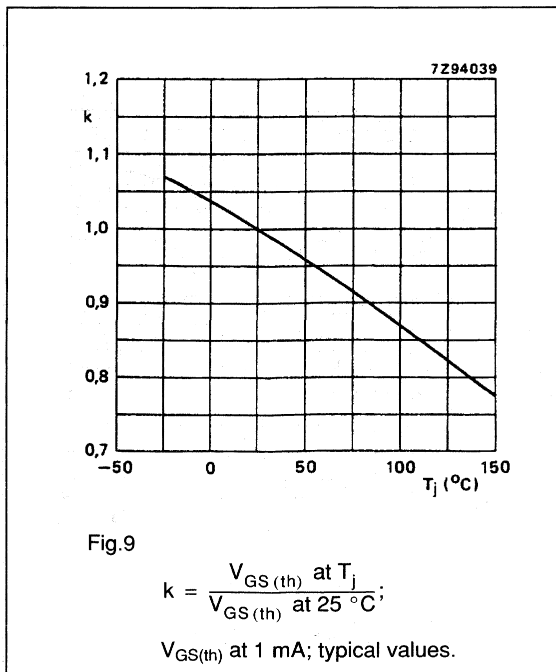


Fig.9

$$k = \frac{V_{GS\,(th)} \text{ at } T_j}{V_{GS\,(th)} \text{ at } 25\ °C};$$

$V_{GS(th)}$ at 1 mA; typical values.

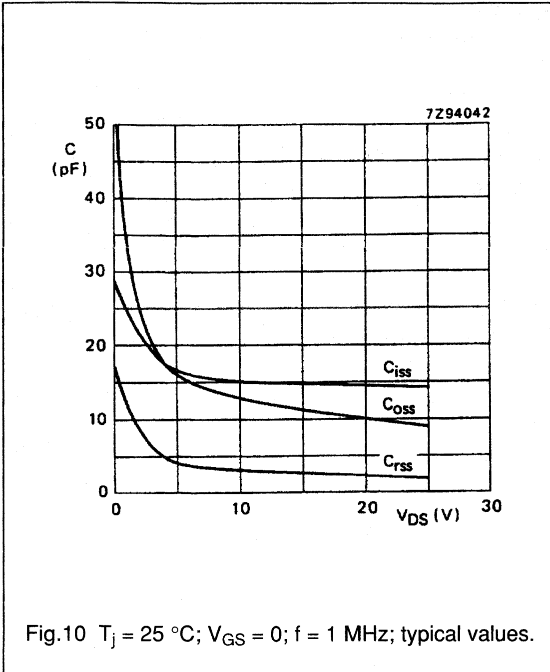


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-channel enhancement mode vertical D-MOS transistor

BST84

DESCRIPTION

N-channel vertical D-MOS transistor in SOT89 envelope and designed for use as line current interrupter in telephone sets and for application in relay, high-speed and line-transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

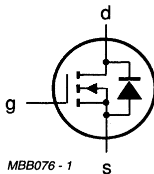
QUICK REFERENCE DATA

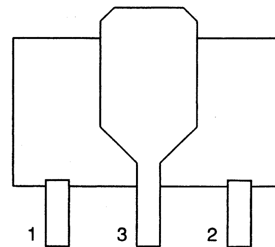
Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance				
I_D = 250 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	6	Ω
		max.	12	Ω
Transfer admittance				
I_D = 250 mA; V_{DS} = 15 V	$\lvert Y_{fs} \rvert$	typ.	250	mS

PINNING - SOT89

1 = source
2 = gate
3 = drain

PIN CONFIGURATION





Marking: KN

Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

BST84

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Drain current (peak)	I_{DM}	max.	800	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

Note

1. Transistor mounted on a ceramic substrate with area of 2.5 cm^2 and thickness of 0.7 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value	Unit
Drain-source breakdown voltage I_D = 100 µA; V_{GS} = 0	$V_{(BR)DSS}$	min.	200	V
Drain-source leakage current V_{DS} = 160 V; V_{GS} = 0	I_{DSS}	max.	10	µA
Gate-source leakage current V_{GS} = 20 V; V_{DS} = 0	I_{GSS}	max.	100	nA
Gate threshold voltage I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.8	V
		max.	2.8	V
Drain-source ON-resistance I_D = 250 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	6	Ω
		max.	12	Ω
Transfer admittance I_D = 250 mA; V_{DS} = 15 V	$\|Y_{fs}\|$	typ.	250	mS
Input capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{iss}	typ.	70	pF
		max.	90	pF
Output capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{oss}	typ.	20	pF
		max.	30	pF
Feedback capacitance at f = 1 MHz V_{DS} = 10 V; V_{GS} = 0	C_{rss}	typ.	5	pF
		max.	10	pF
Switching times (see Figs 2 and 3) I_D = 250 mA; V_{DD} = 50 V; V_{GS} = 0 to 10 V	t_{on}	typ.	4	ns
		max.	10	ns
	t_{off}	typ.	15	ns
		max.	25	ns

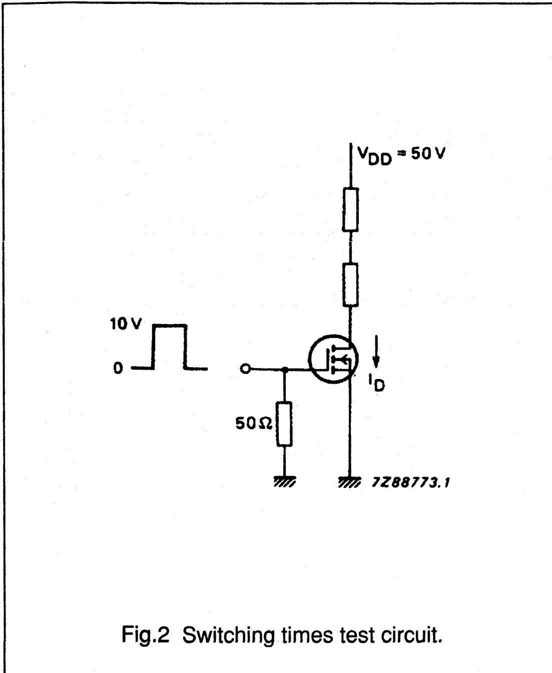


Fig.2 Switching times test circuit.

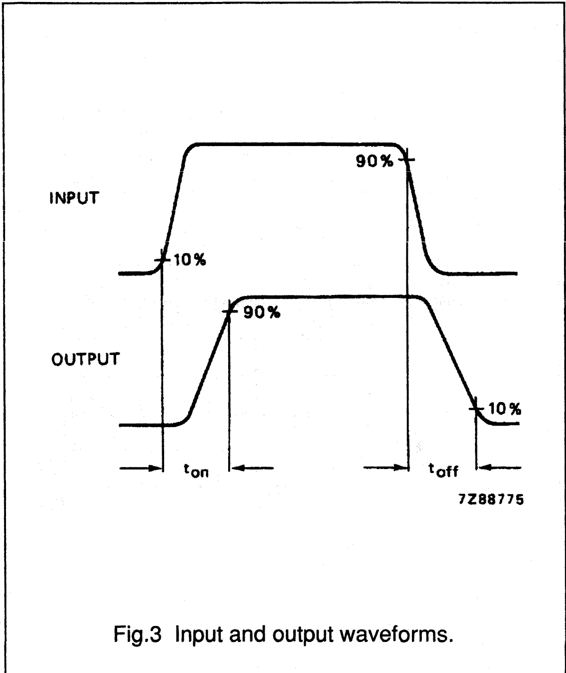


Fig.3 Input and output waveforms.

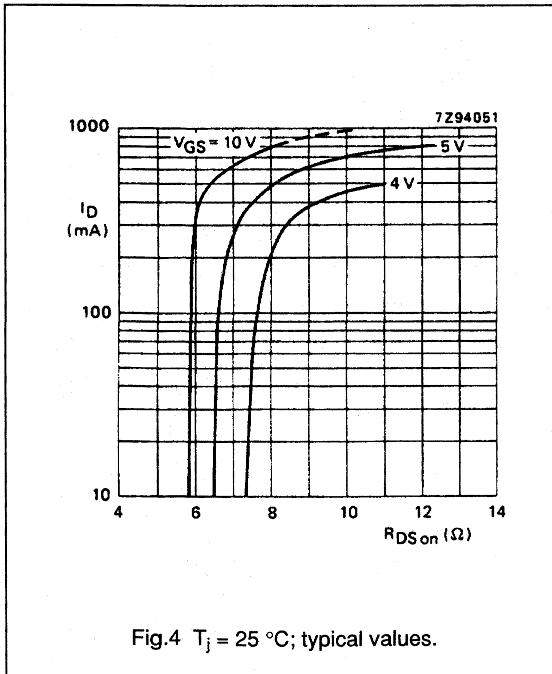


Fig.4 T_j = 25 °C; typical values.

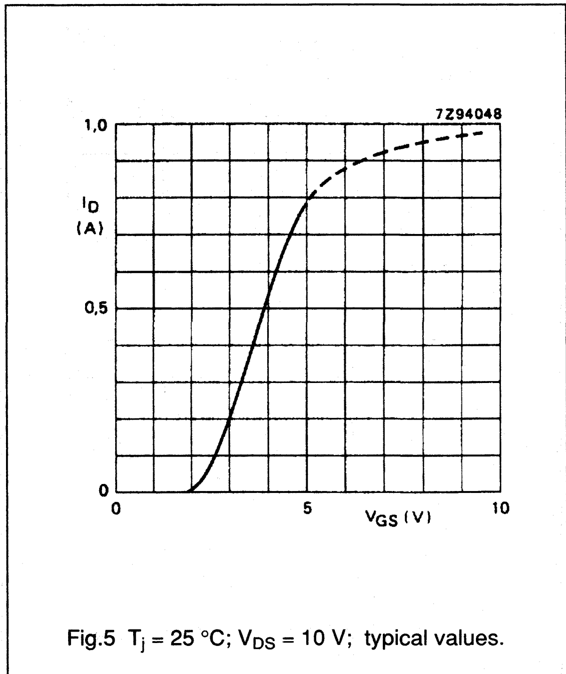


Fig.5 T_j = 25 °C; V_{DS} = 10 V; typical values.

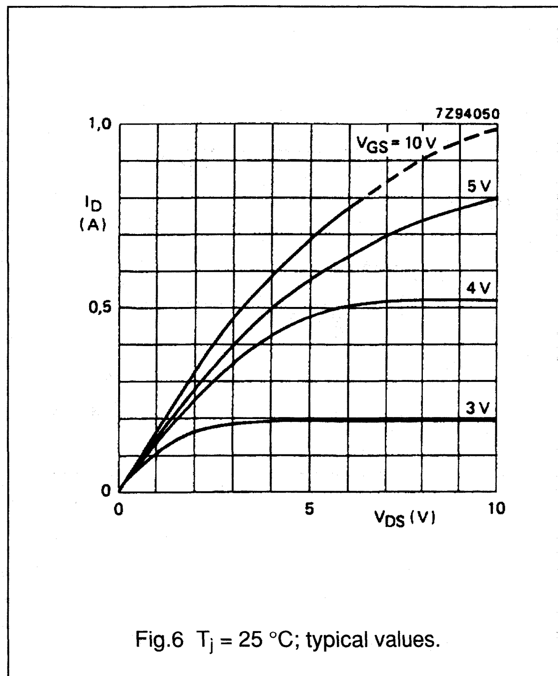


Fig.6 T_j = 25 °C; typical values.

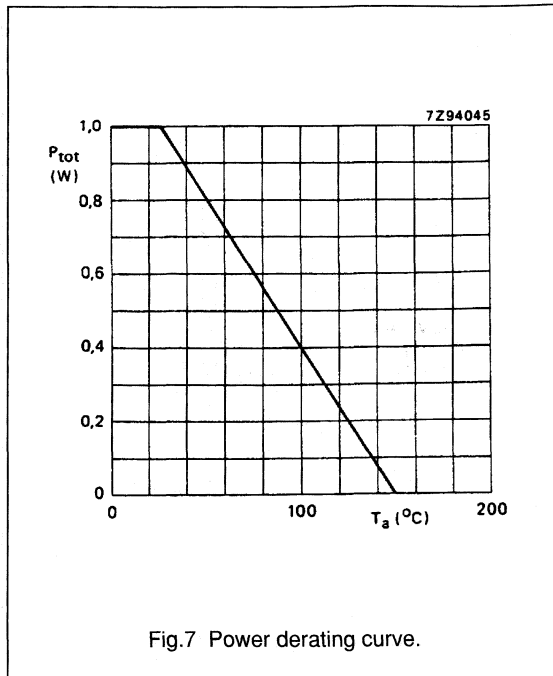


Fig.7 Power derating curve.

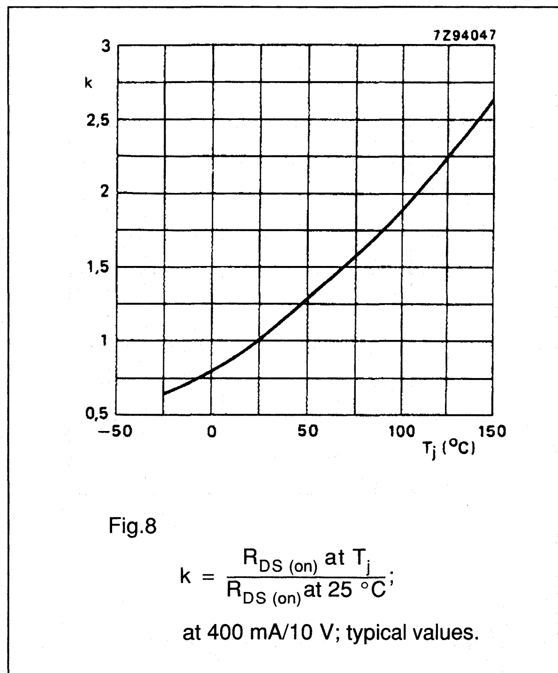


Fig.8

$$k = \frac{R_{DS\,(on)}\ \text{at}\ T_j}{R_{DS\,(on)}\ \text{at}\ 25\ °C};$$

at 400 mA/10 V; typical values.

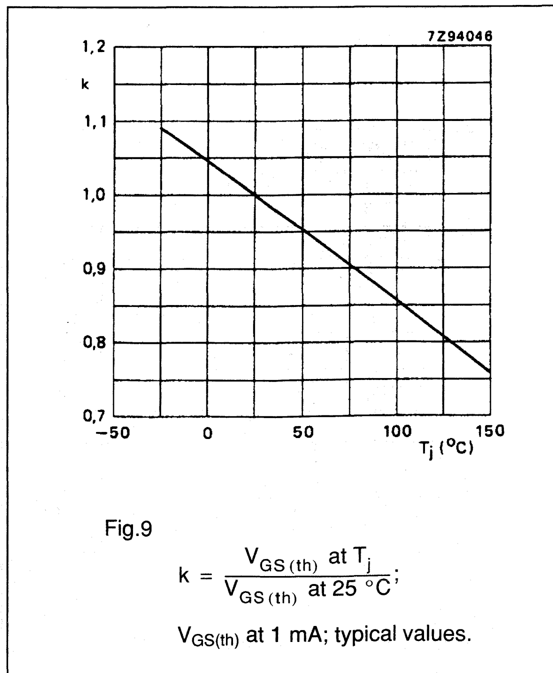


Fig.9

$$k = \frac{V_{GS\,(th)}\ \text{at}\ T_j}{V_{GS\,(th)}\ \text{at}\ 25\ °C};$$

$V_{GS(th)}$ at 1 mA; typical values.

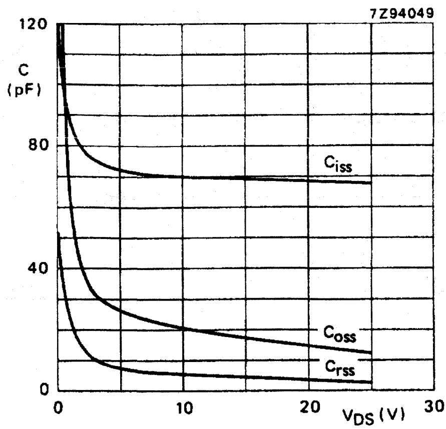


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

N-channel enhancement mode vertical D-MOS transistor

BST86

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in SOT89 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for application with relay, high-speed and line-transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	180	V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance I_D = 15 mA; V_{GS} = 3 V	$R_{DS(on)}$	typ. max.	7 10	Ω Ω
Transfer admittance I_D = 300 mA; V_{DS} = 15 V	$\lvert Y_{fs} \rvert$	typ.	250	mS

PINNING - SOT89

1 = source
2 = drain
3 = gate

PIN CONFIGURATION

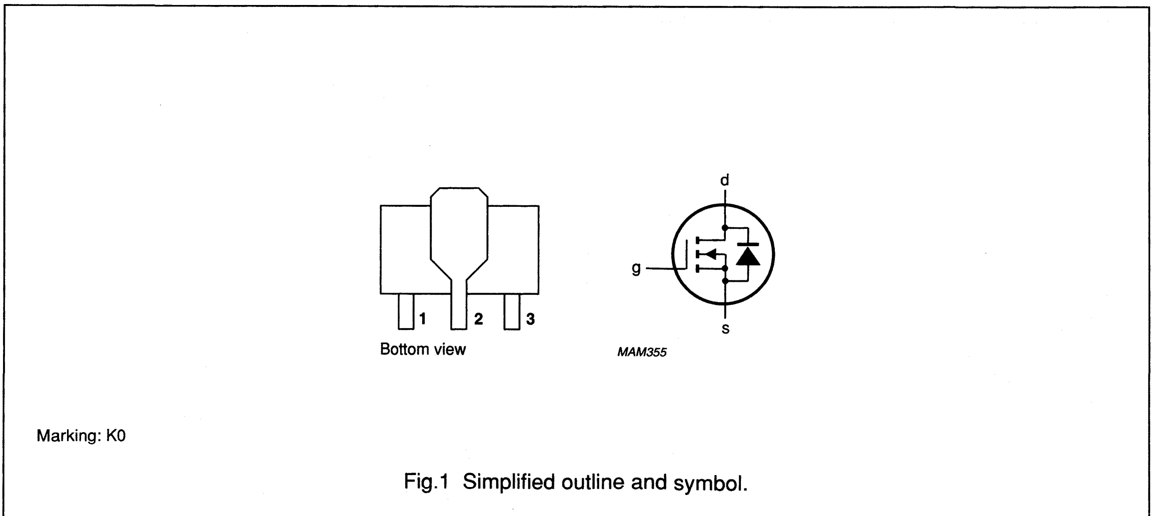


Fig.1 Simplified outline and symbol.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	180	V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	200	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	300	mA
Drain current (peak)	I_{DM}	max.	800	mA
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

Note

1. Transistor mounted on a ceramic substrate of 2.5 cm^2 and thickness of 0.7 mm.

CHARACTERISTICS

$T_j = 25\ °C$ unless otherwise specified

Parameter	Symbol		Value	Unit
Drain-source breakdown voltage				
$I_D = 100\ \mu A$; $V_{GS} = 0$	$V_{(BR)DSS}$	min.	180	V
Drain-source leakage current				
$V_{DS} = 120\ V$; $V_{GS} = 0$	I_{DSS}	max.	10	μA
Gate-source leakage current				
$V_{GS} = 20\ V$; $V_{DS} = 0$	I_{GSS}	max.	100	nA
Gate threshold voltage				
$I_D = 100\ \mu A$; $V_{DS} = V_{GS}$	$V_{GS(th)}$	min.	0.7	V
		max.	2.7	V
Drain-source ON-resistance				
$I_D = 15\ mA$; $V_{GS} = 3\ V$	$R_{DS(on)}$	typ.	7	Ω
		max.	10	Ω
$I_D = 300\ mA$; $V_{GS} = 10\ V$	$R_{DS(on)}$	typ.	6	Ω
Transfer admittance				
$I_D = 300\ mA$; $V_{DS} = 15\ V$	$\lvert Y_{fs} \rvert$	typ.	250	mS
Input capacitance at f = 1 MHz				
$V_{DS} = 10\ V$; $V_{GS} = 0$	C_{iss}	typ.	50	pF
		max.	65	pF
Output capacitance at f = 1 MHz				
$V_{DS} = 10\ V$; $V_{GS} = 0$	C_{oss}	typ.	20	pF
		max.	30	pF
Feedback capacitance at f = 1 MHz				
$V_{DS} = 10\ V$; $V_{GS} = 0$	C_{rss}	typ.	6	pF
		max.	10	pF
Switching times (see as 2 and 3)				
$I_D = 300\ mA$; $V_{DD} = 50\ V$; $V_{GS} = 0$ to $10\ V$	t_{on}	max.	10	ns
	t_{off}	max.	15	ns

N-channel enhancement mode vertical D-MOS transistor

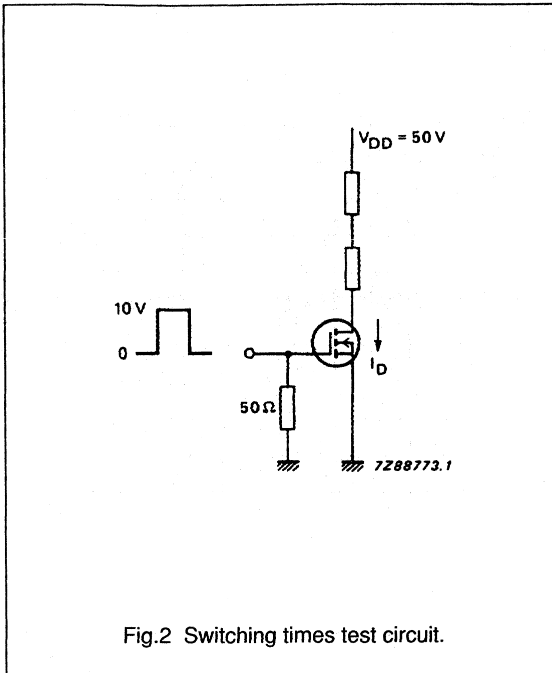


Fig.2 Switching times test circuit.

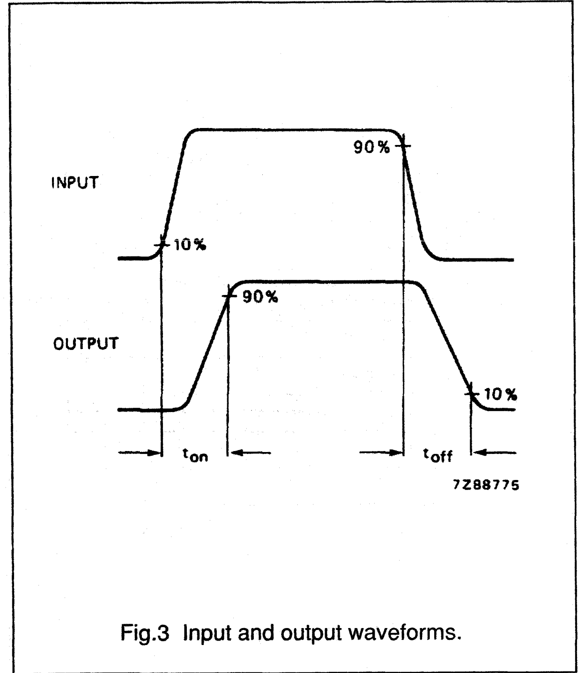


Fig.3 Input and output waveforms.

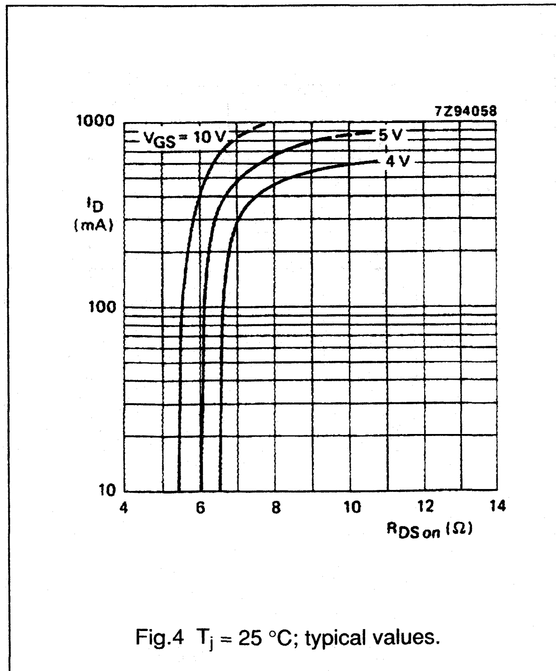


Fig.4 T_j = 25 °C; typical values.

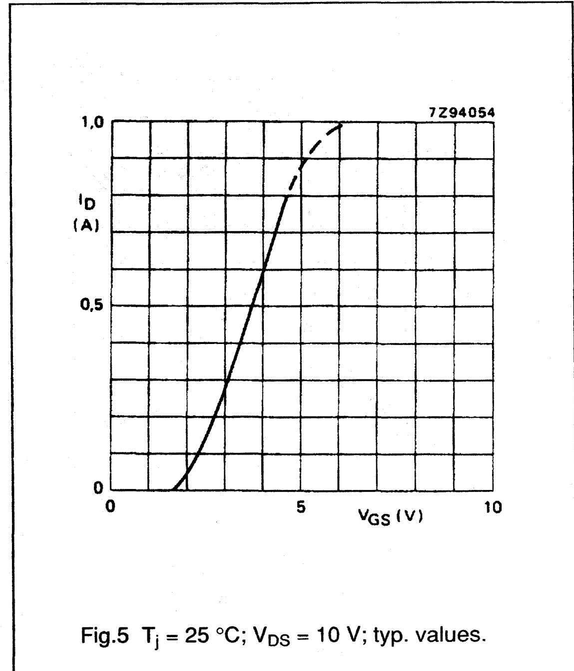


Fig.5 T_j = 25 °C; V_{DS} = 10 V; typ. values.

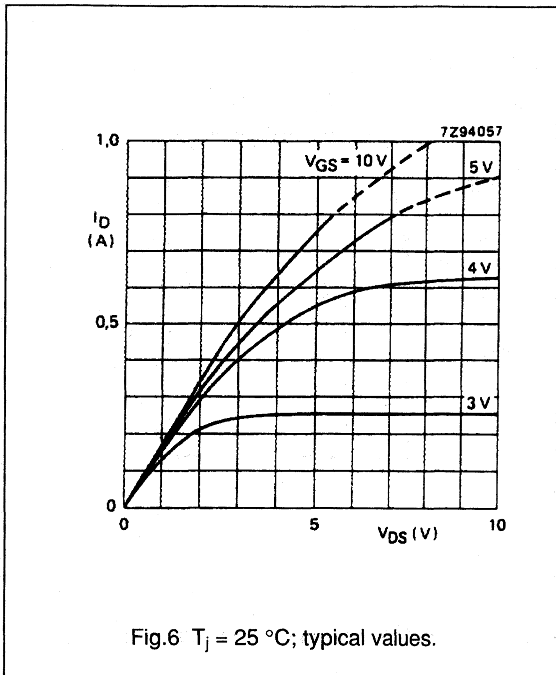


Fig.6 T_j = 25 °C; typical values.

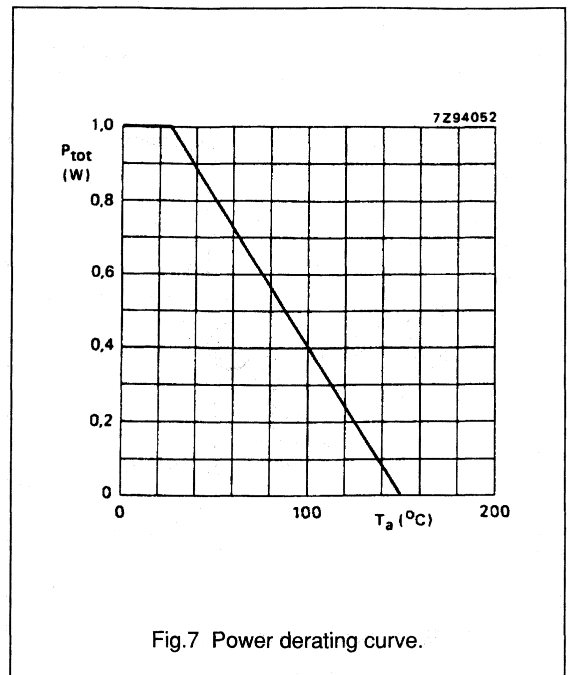


Fig.7 Power derating curve.

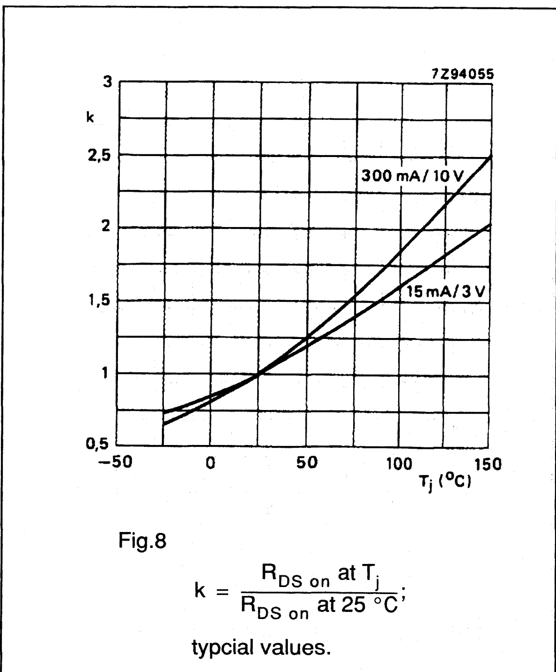


Fig.8

$$k = \frac{R_{DS\ on}\ \text{at}\ T_j}{R_{DS\ on}\ \text{at}\ 25\ °C};$$

typcial values.

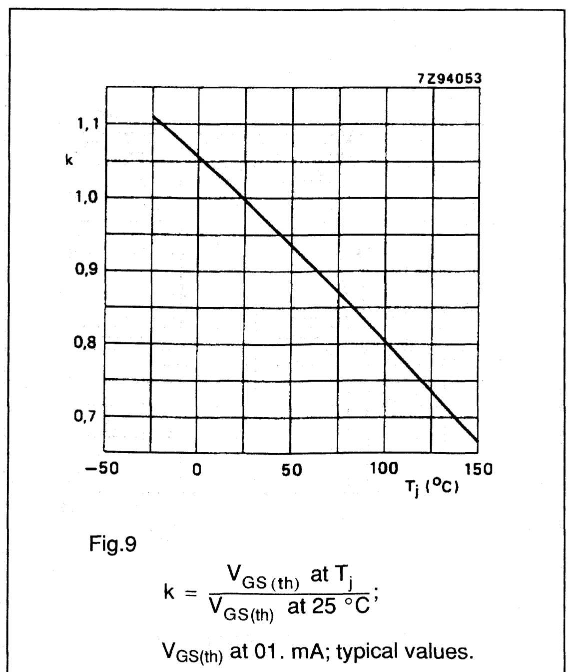


Fig.9

$$k = \frac{V_{GS(th)}\ \text{at}\ T_j}{V_{GS(th)}\ \text{at}\ 25\ °C};$$

$V_{GS(th)}$ at 01. mA; typical values.

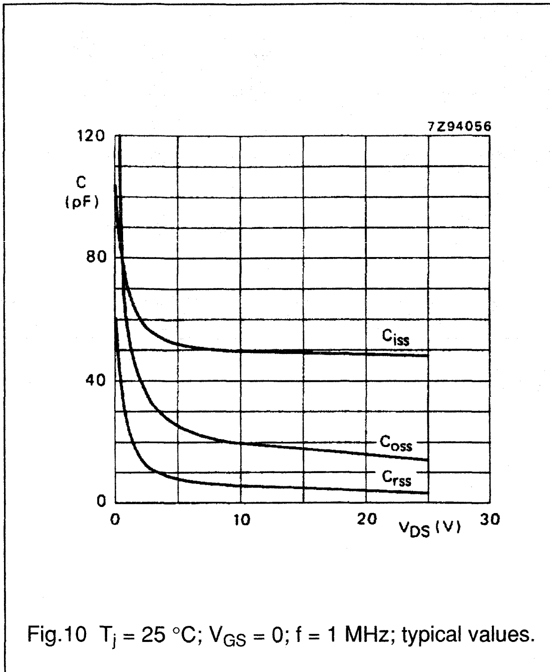


Fig.10 T_j = 25 °C; V_{GS} = 0; f = 1 MHz; typical values.

P-channel enhancement mode vertical D-MOS transistor

BST100

DESCRIPTION

P-channel vertical D-MOS transistor TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

FEATURES

- Very low $R_{DS(on)}$
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0.3	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance				
$-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$R_{DS(on)}$	typ.	4,5	Ω
		max.	6	Ω
Transfer admittance				
$-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\|Y_{fs}\|$	typ.	200	mS

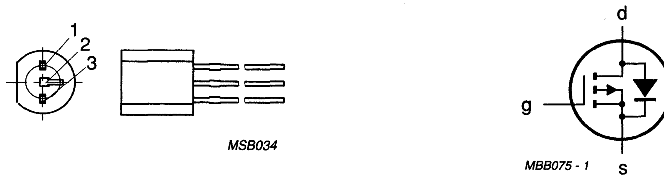
PINNING - TO-92 VARIANT

1 = source

2 = gate

3 = drain

PIN CONFIGURATION



Note: various pinout configurations available.

Fig.1 Simplified outline and symbol.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0.3	A
Drain current (peak)	$-I_{DM}$	max.	0.8	A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

Note

1. Transistor mounted on printed-circuit board, max. lead length 4 mm, mounting pad for drain lead min. 10 mm x 10 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value	Unit
Drain-source breakdown voltage $-I_D$ = 10 µA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	60	V
Drain-source leakage current $-V_{DS}$ = 48 V; V_{GS} = 0	$-I_{DSS}$	max.	1	µA
Gate-source leakage current $-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	100	nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min.	1.5	V
		max.	3.5	V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$R_{DS(on)}$	typ.	4.5	Ω
		max.	6	Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert Y_{fs} \rvert$	typ.	200	mS
Input capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ.	55	pF
		max.	70	pF
Output capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ.	30	pF
		max.	45	pF
Feedback capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ.	8	pF
		max.	12	pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on}	typ.	4	ns
	t_{off}	typ.	20	ns

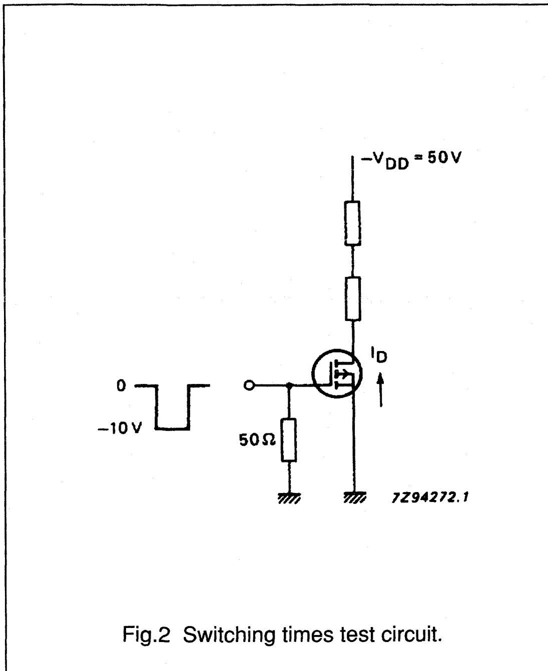


Fig.2 Switching times test circuit.

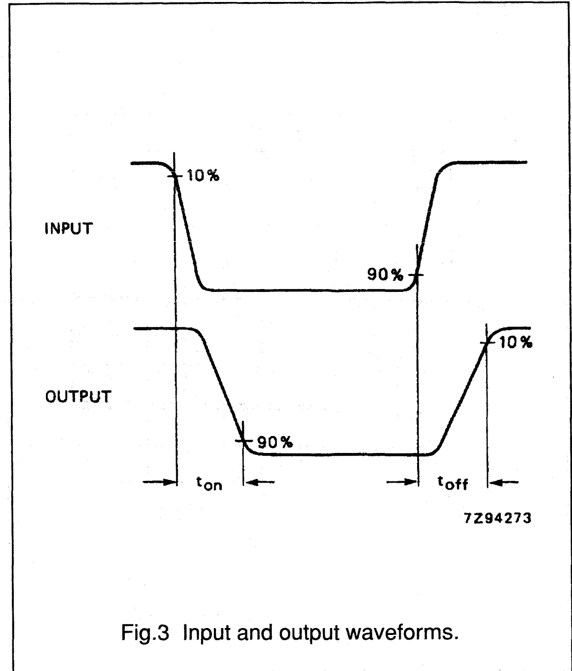


Fig.3 Input and output waveforms.

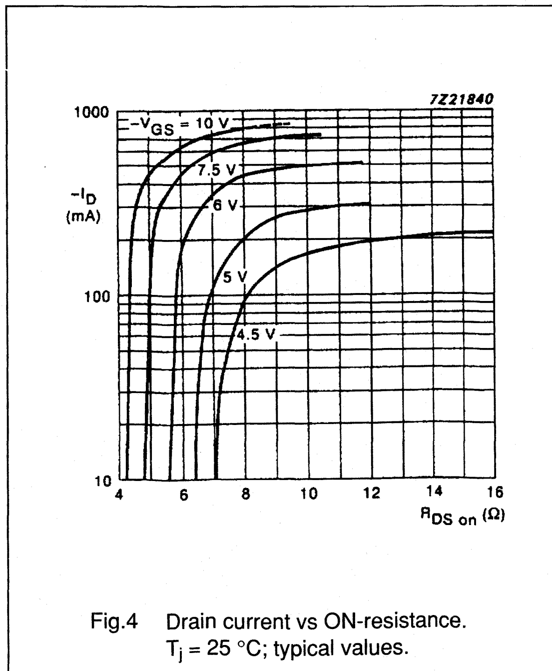


Fig.4 Drain current vs ON-resistance.
T_j = 25 °C; typical values.

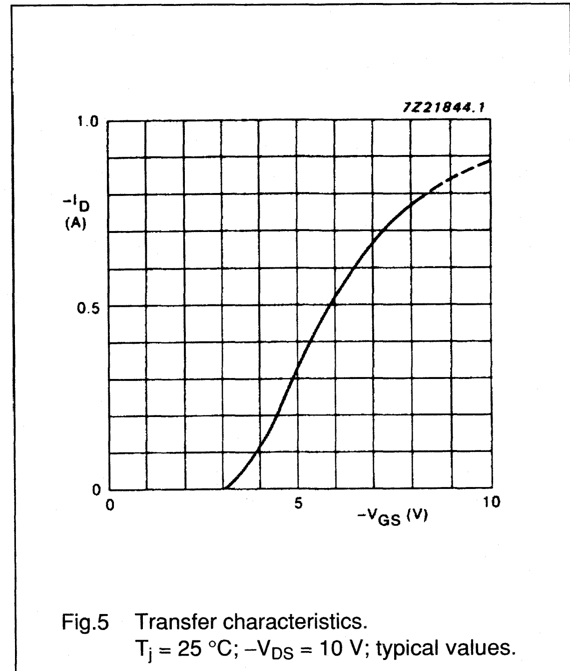


Fig.5 Transfer characteristics.
T_j = 25 °C; $-V_{DS}$ = 10 V; typical values.

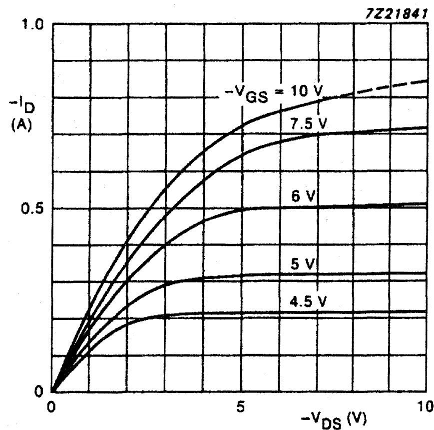


Fig.6 Output characteristics. T_j = 25 °C; typical values.

P-channel enhancement mode vertical D-MOS transistor

BST120

DESCRIPTION

P-channel vertical D-MOS transistor in SOT89 envelope and intended for use in relay, high-speed and line-transformer drivers, using SMD technology.

FEATURES

- Very low $R_{DS(on)}$
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

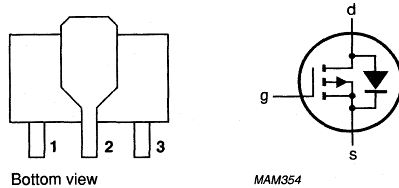
QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0,3	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance				
$-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$R_{DS(on)}$	typ.	4,5	Ω
		max.	6	Ω
Transfer admittance				
$-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert Y_{fs} \rvert$	typ.	200	mS

PINNING - SOT89

1 = source
2 = drain
3 = gate

PIN CONFIGURATION



marking: LM

Fig.1 Simplified outline and symbol.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0.3	A
Drain current (peak)	$-I_{DM}$	max.	0.8	A
Total power dissipation up to T_{amb} = 25 °C (note 1)	P_{tot}	max.	1	W
Storage temperature range	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

Note

1. Transistor mounted on ceramic substrate: area = 2,5 cm^2 and thickness = 0,7 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter	Symbol		Value	Unit
Drain-source breakdown voltage $-I_D$ = 10 μA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	60	V
Drain-source leakage current $-V_{DS}$ = 48 V; V_{GS} = 0	$-I_{DSS}$	max.	1	μA
Gate-source leakage current $-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	100	nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min. max.	1.5 3.5	V V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$R_{DS(on)}$	typ. max.	4.5 6	Ω Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\|Y_{fs}\|$	typ.	200	mS
Input capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ. max.	55 70	pF pF
Output capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ. max.	30 45	pF pF
Feedback capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ. max.	8 12	pF pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on} t_{off}	typ. typ.	4 20	ns ns

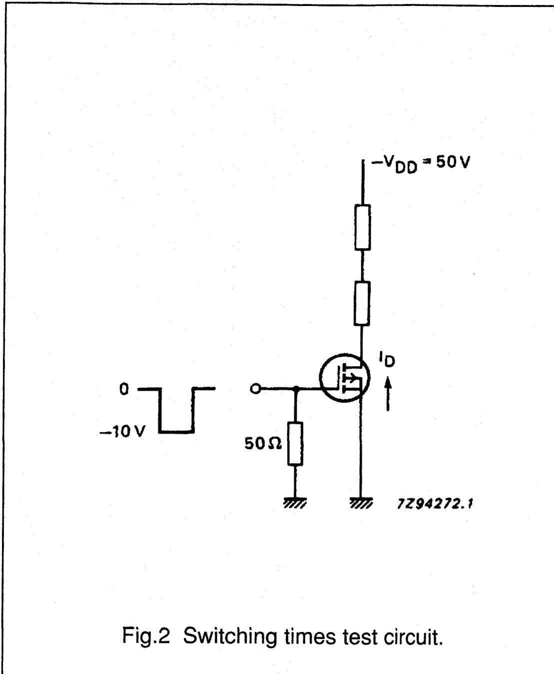


Fig.2 Switching times test circuit.

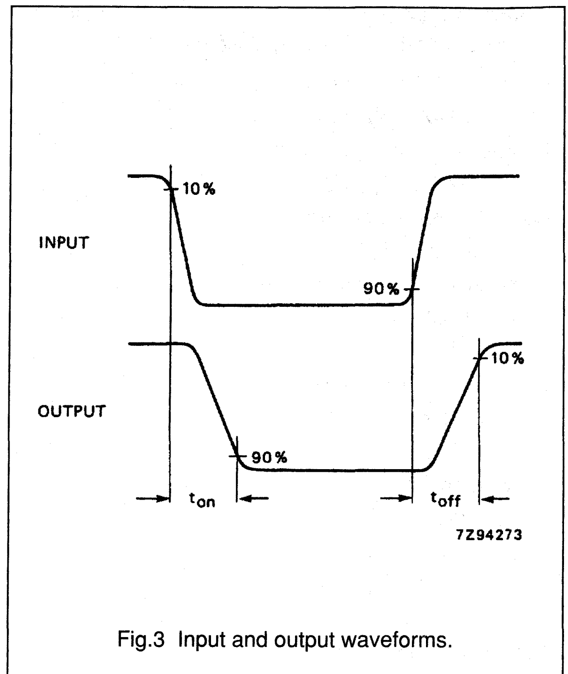


Fig.3 Input and output waveforms.

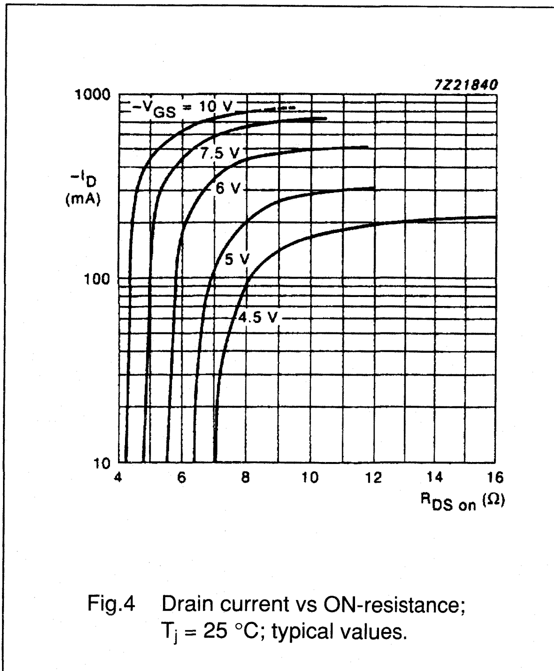


Fig.4 Drain current vs ON-resistance; T_j = 25 °C; typical values.

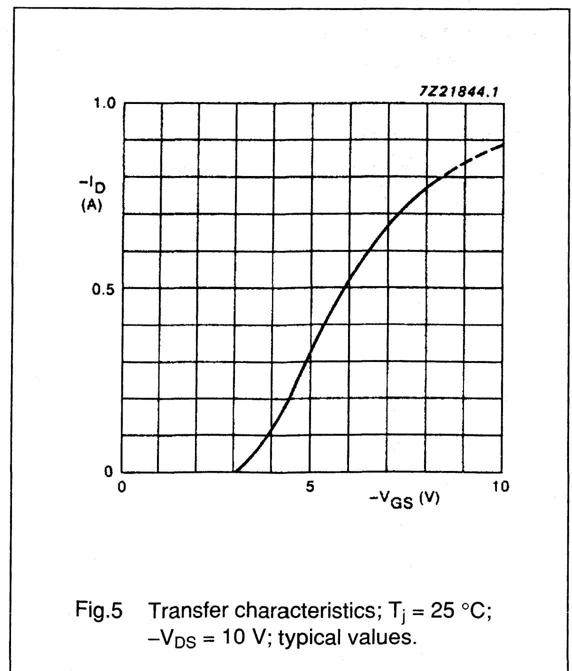


Fig.5 Transfer characteristics; T_j = 25 °C; $-V_{DS}$ = 10 V; typical values.

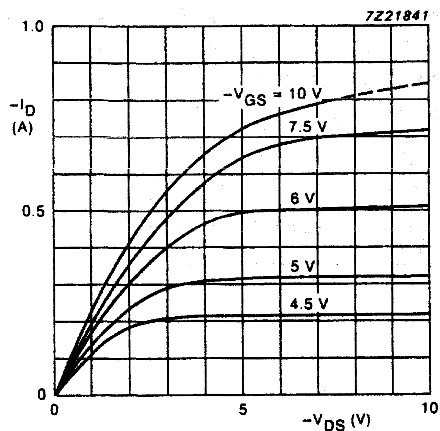


Fig.6 Output characteristics; T_j = 25 °C; typical values.

P-channel enhancement mode vertical D-MOS transistor

BST122

DESCRIPTION

P-channel vertical D-MOS transistor in SOT89 envelope and intended for use in relay, high-speed and line-transformer drivers, using SMD-technology.

FEATURES

- Very low $R_{DS(on)}$
- Direct interface to C-MOS, TTL
- High-speed switching
- No second breakdown

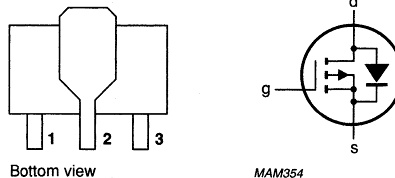
QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0,25	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Drain-source ON-resistance				
$-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$R_{DS(on)}$	max.	10	Ω
		typ.	7.5	Ω
Transfer admittance				
$-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert Y_{fs} \rvert$	typ.	125	mS

PINNING - SOT89

1 = source
2 = drain
3 = gate

PIN CONFIGURATION



Marking: LN

Fig.1 Simplified outline and symbol.

P-channel enhancement mode vertical D-MOS transistor

BST122

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	$-I_D$	max.	0.25	A
Drain current (peak)	$-I_{DM}$	max.	0.5	A
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	1	W
Storage temperature range	T_{stg}	−65 to + 150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	125	K/W

Note

1. Transistor mounted on a ceramic substrate: area = 2,5 cm^2; thickness = 0,7 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter / conditions	Symbol		Value	Unit
Drain-source breakdown voltage $-I_D$ = 10 μA; V_{GS} = 0	$-V_{(BR)DSS}$	min.	60	V
Drain-source leakage current $-V_{DS}$ = 48 V; V_{GS} = 0	$-I_{DSS}$	max.	1	μA
Gate-source leakage current $-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	max.	100	nA
Gate threshold voltage $-I_D$ = 1 mA; V_{DS} = V_{GS}	$-V_{GS(th)}$	min.	1.5	V
		max.	3.5	V
Drain-source ON-resistance $-I_D$ = 200 mA; $-V_{GS}$ = 10 V	$R_{DS(on)}$	max.	10	Ω
		typ.	7.5	Ω
Transfer admittance $-I_D$ = 200 mA; $-V_{DS}$ = 15 V	$\lvert Y_{fs} \rvert$	typ.	125	mS
Input capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{iss}	typ.	30	pF
		max.	45	pF
Output capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{oss}	typ.	20	pF
		max.	30	pF
Feedback capacitance at f = 1 MHz $-V_{DS}$ = 10 V; V_{GS} = 0	C_{rss}	typ.	5	pF
		max.	10	pF
Switching times (see Figs 2 and 3) $-I_D$ = 200 mA; $-V_{DD}$ = 50 V; $-V_{GS}$ = 0 to 10 V	t_{on}	typ.	4	ns
	t_{off}	typ.	10	ns

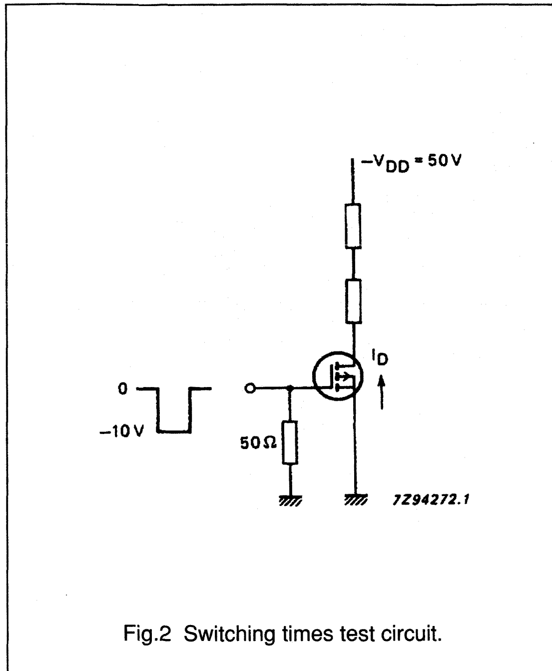


Fig.2 Switching times test circuit.

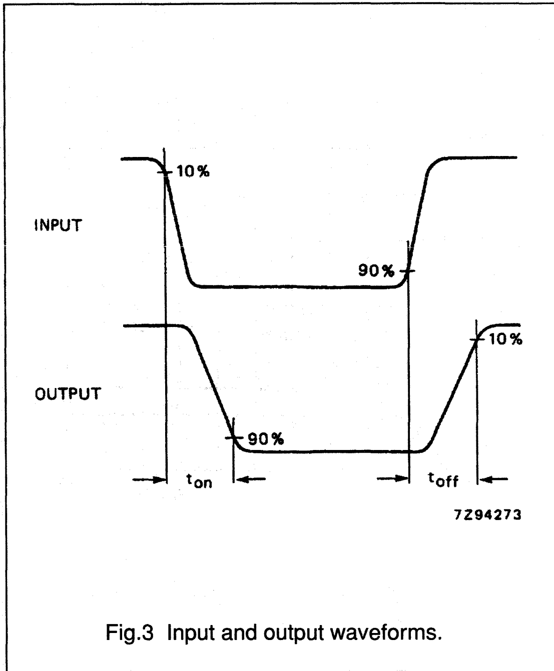


Fig.3 Input and output waveforms.

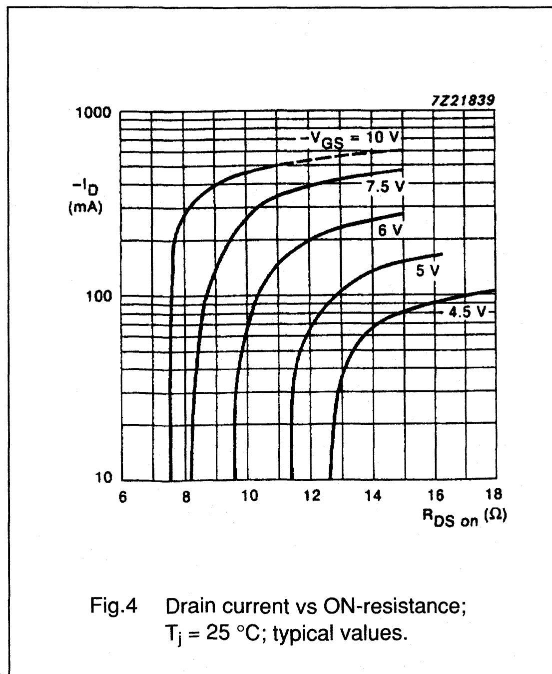


Fig.4 Drain current vs ON-resistance; T_j = 25 °C; typical values.

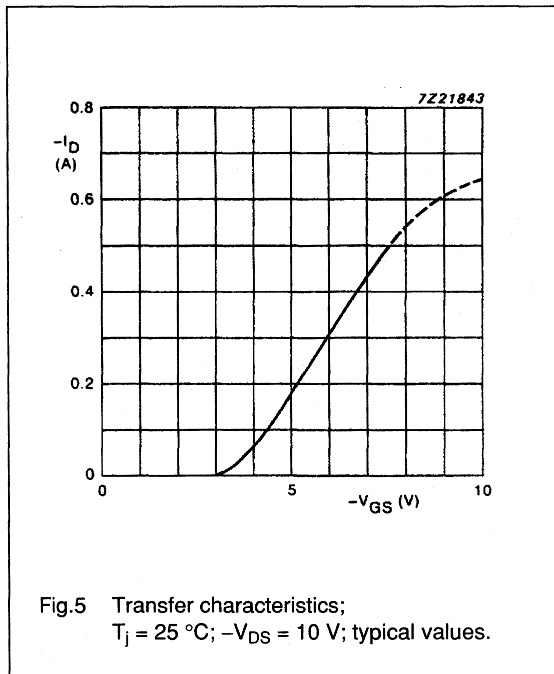


Fig.5 Transfer characteristics; T_j = 25 °C; $-V_{DS}$ = 10 V; typical values.

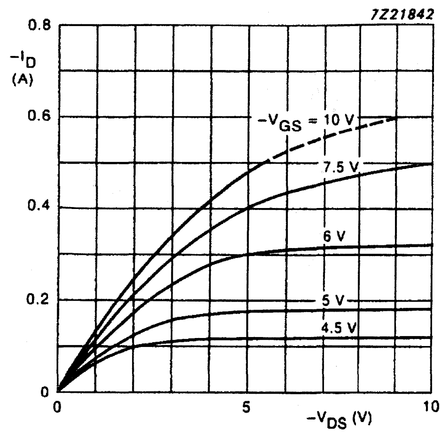


Fig.6 Output characteristics; T_j = 25 °C; typical values.

Complementary enhancement mode MOS transistors

PHC2300

FEATURES

- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Universal line interface in telephone sets
- Relay, high-speed and line transformer drivers.

DESCRIPTION

One N-channel and one P-channel enhancement mode MOS transistor in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

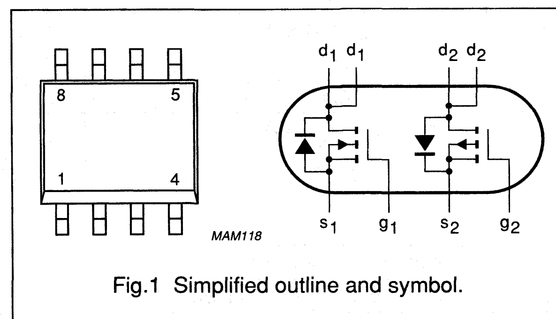


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per channel					
V_{DS}	drain-source voltage (DC)				
	N-channel		–	300	V
	P-channel		–	–300	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage				V
	N-channel	$V_{DS} = V_{GS}$; $I_D = 1$ mA	0.8	2	V
	P-channel	$V_{DS} = V_{GS}$; $I_D = -1$ mA	–0.8	–2	V
I_D	drain current (DC)	$T_s = 80$ °C			
	N-channel		–	350	mA
	P-channel		–	–250	mA
R_{DSon}	drain-source on-state resistance				
	N-channel	$V_{GS} = 10$ V; $I_D = 175$ mA	–	8	Ω
	P-channel	$V_{GS} = -10$ V; $I_D = -125$ mA	–	17	Ω
P_{tot}	total power dissipation	$T_s = 80$ °C	–	2	W

PRELIMINARY
See Philips Semiconductors for Design-in information

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per channel					
V_{DS}	drain-source voltage (DC)				
	N-channel		–	300	V
	P-channel		–	–300	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1			
	N-channel		–	350	mA
	P-channel		–	–250	mA
I_{DM}	peak drain current	note 2			
	N-channel		–	1.4	A
	P-channel		–	–1	A
P_{tot}	total power dissipation	T_s = 80 °C; note 3	–	2	W
		T_{amb} = 25 °C; note 4	–	2	W
		T_{amb} = 25 °C; note 5	–	1	W
		T_{amb} = 25 °C; note 6	–	1.3	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C

Notes

1. T_s is the temperature at the soldering point of the drain leads.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Maximum permissible dissipation per MOS transistor. (So both devices may be loaded up to 2 W at the same time).
4. Maximum permissible dissipation per MOS transistor. Value based on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
5. Maximum permissible dissipation per MOS transistor. Value based on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.
6. Maximum permissible dissipation if only one MOS transistor dissipates. Value based on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	35	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per channel						
$V_{(BR)DSS}$	drain-source breakdown voltage					
	N-channel	V_{GS} = 0; I_D = 10 μA	300	–	–	V
	P-channel	V_{GS} = 0; I_D = −10 μA	−300	–	–	V
V_{GSth}	gate-source threshold voltage					
	N-channel	V_{GS} = V_{DS}; I_D = 1 mA	0.8	–	2	V
	P-channel	V_{GS} = V_{DS}; I_D = −1 mA	−0.8	–	−2	V
I_{DSS}	drain-source leakage current					
	N-channel	V_{GS} = 0; V_{DS} = 240 V	–	–	100	nA
	P-channel	V_{GS} = 0; V_{DS} = −240 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±16 V; V_{DS} = 0				
	N-channel		–	–	±100	nA
	P-channel		–	–	±100	nA
R_{DSon}	drain-source on-state resistance					
	N-channel	V_{GS} = 10 V; I_D = 175 mA	–	–	8	Ω
	P-channel	V_{GS} = −10 V; I_D = − 125 mA	–	–	17	Ω
C_{iss}	input capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	57	–	pF
	P-channel	V_{GS} = 0; V_{DS} = −50 V; f = 1 MHz	–	45	–	pF
C_{oss}	output capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	15	–	pF
	P-channel	V_{GS} = 0; V_{DS} = −50 V; f = 1 MHz	–	15	–	pF
C_{rss}	reverse transfer capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 50 V; f = 1 MHz	–	2.6	–	pF
	P-channel	V_{GS} = 0; V_{DS} = −50 V; f = 1 MHz	–	3	–	pF
Q_G	total gate charge					
	N-channel	V_{GS} = 10 V; V_{DS} = 50 V; I_D = 175 mA	–	2097	–	pC
	P-channel	V_{GS} = −10 V; V_{DS} = −50 V; I_D = −125 mA	–	2137	–	pC
Q_{GS}	gate-source charge					
	N-channel	V_{GS} = 10 V; V_{DS} = 50 V; I_D = 175 mA	–	75	–	pC
	P-channel	V_{GS} = −10 V; V_{DS} = −50 V; I_D = −125 mA	–	68	–	pC
Q_{GD}	gate-drain charge					
	N-channel	V_{GS} = 10 V; V_{DS} = 50 V; I_D = 175 mA	–	527	–	pC
	P-channel	V_{GS} = −10 V; V_{DS} = −50 V; I_D = −125 mA	–	674	–	pC

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switching times						
t_{on}	turn-on time					
	N-channel	V_{GS} = 0 to 10 V; V_{DD} = 50 V; I_D = 175 mA	–	2.5	10	ns
	P-channel	V_{GS} = 0 to −10 V; V_{DD} = −50 V; I_D = −125 mA	–	4	10	ns
t_{off}	turn-off time					
	N-channel	V_{GS} = 10 to 0 V; V_{DD} = 50 V; I_D = 175 mA	–	17	30	ns
	P-channel	V_{GS} = −10 to 0 V; V_{DD} = −50 V; I_D = −125 mA	–	25	35	ns

Complementary enhancement mode MOS transistors

PHC20512

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-state resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

One N-channel and one P-channel enhancement mode MOS transistor in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

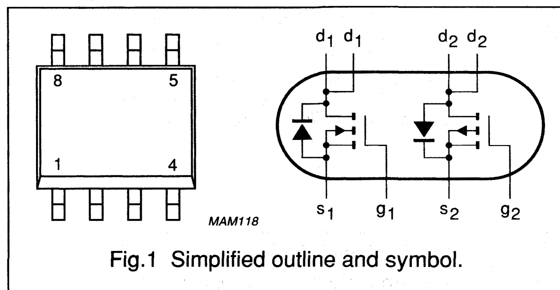


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per channel					
V_{DS}	drain-source voltage (DC)				
	N-channel		–	30	V
	P-channel		–	–30	V
V_{SD}	source-drain diode forward voltage				
	N-channel	I_S = 1.25 A	–	1	V
	P-channel	I_S = –1.25 A	–	–1.3	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage				
	N-channel	$V_{DS} = V_{GS}$; I_D = 1 mA	1	2.8	V
	P-channel	$V_{DS} = V_{GS}$; I_D = –1 mA	–1	–2.8	V
I_D	drain current (DC)	T_s = 80 °C			
	N-channel		–	6.4	A
	P-channel		–	–4	A
R_{DSon}	drain-source on-state resistance				
	N-channel	V_{GS} = 10 V; I_D = 3.2 A	–	0.05	Ω
	P-channel	V_{GS} = –10 V I_D = –2 A	–	0.12	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	3.5	W

PRELIMINARY information
See Philips Semiconductors for Design-in

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per channel					
V_{DS}	drain-source voltage (DC)				
	N-channel		–	30	V
	P-channel		–	–30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1			
	N-channel		–	6.4	A
	P-channel		–	–4	A
I_{DM}	peak drain current	note 2			
	N-channel		–	25	A
	P-channel		–	–16	A
P_{tot}	total power dissipation	T_s = 80 °C; note 3	–	3.5	W
		T_{amb} = 25 °C; note 4	–	2.6	W
		T_{amb} = 25 °C; note 5	–	1.1	W
		T_{amb} = 25 °C; note 6	–	1.5	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–65	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C			
	N-channel		–	3.5	A
	P-channel		–	–2.6	A
I_{SM}	peak pulsed source current	note 2			
	N-channel		–	14	A
	P-channel		–	–10	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 3.5 W at the same time.
4. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
5. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.
6. Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

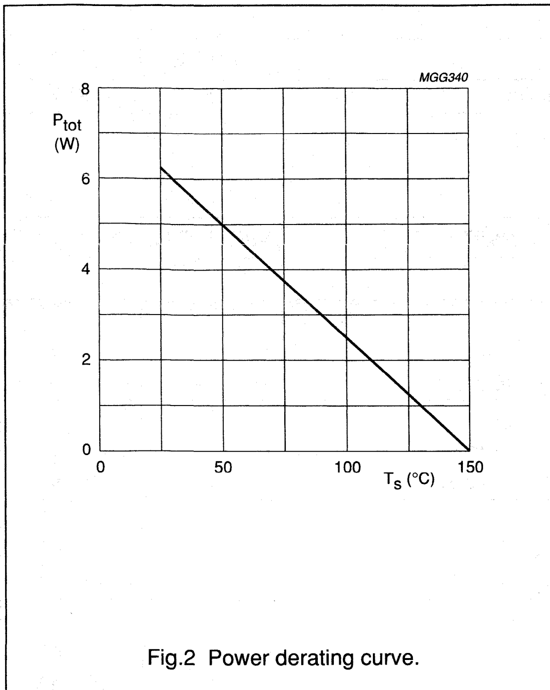
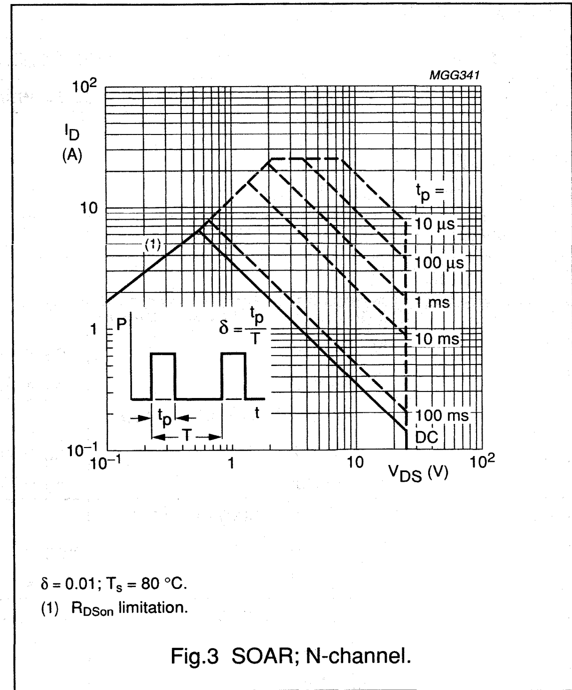


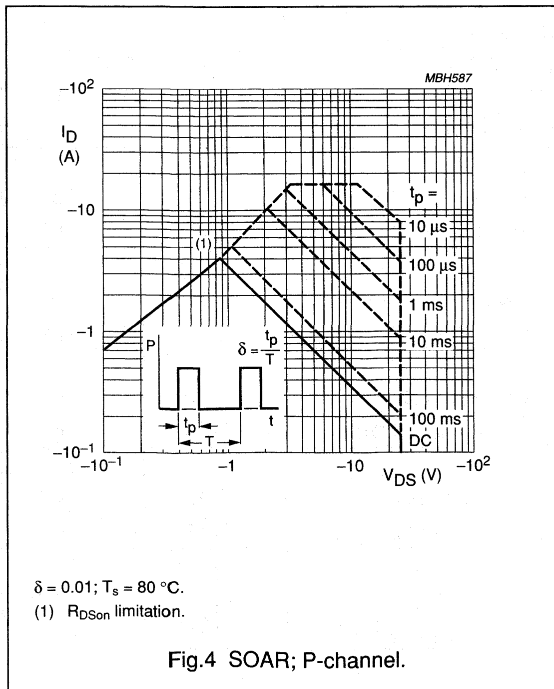
Fig.2 Power derating curve.



$\delta = 0.01$; $T_s = 80$ °C.

(1) R_{DSon} limitation.

Fig.3 SOAR; N-channel.



$\delta = 0.01$; $T_s = 80$ °C.

(1) R_{DSon} limitation.

Fig.4 SOAR; P-channel.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	20	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per channel						
$V_{(BR)DSS}$	drain-source breakdown voltage					
	N-channel	V_{GS} = 0; I_D = 10 μA	30	–	–	V
	P-channel	V_{GS} = 0; I_D = –10 μA	–30	–	–	V
V_{GSth}	gate-source threshold voltage					
	N-channel	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
	P-channel	V_{GS} = V_{DS}; I_D = –1 mA	–1	–	–2.8	V
I_{DSS}	drain-source leakage current					
	N-channel	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
	P-channel	V_{GS} = 0; V_{DS} = –24 V	–	–	–100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0				
	N-channel		–	–	±100	nA
	P-channel		–	–	±100	nA
R_{DSon}	drain-source on-state resistance					
	N-channel	V_{GS} = 4.5 V; I_D = 1.6 A	–	–	0.1	Ω
		V_{GS} = 10 V; I_D = 3.2 A	–	–	0.05	Ω
	P-channel	V_{GS} = –4.5 V; I_D = –1 A	–	–	0.25	Ω
		V_{GS} = –10 V; I_D = –2 A	–	–	0.12	Ω
C_{iss}	input capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	450	–	pF
	P-channel	V_{GS} = 0; V_{DS} = –24 V; f = 1 MHz	–	450	–	pF
C_{oss}	output capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	200	–	pF
	P-channel	V_{GS} = 0; V_{DS} = –24 V; f = 1 MHz	–	200	–	pF
C_{rss}	reverse transfer capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	100	–	pF
	P-channel	V_{GS} = 0; V_{DS} = –24 V; f = 1 MHz	–	100	–	pF
Q_G	total gate charge					
	N-channel	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 3.2 A	–	15	–	nC
	P-channel	V_{GS} = –10 V; V_{DD} = –15 V; I_D = –2 A	–	13	–	nC
Q_{GS}	gate-source charge					
	N-channel	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 3.2 A	–	1	–	nC
	P-channel	V_{GS} = –10 V; V_{DD} = –15 V; I_D = –2 A	–	1	–	nC

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Q_{GD}	gate-drain charge					
	N-channel	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 3.2 A	–	5	–	nC
	P-channel	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −2 A	–	4	–	nC
$t_{d(on)}$	turn-on delay time					
	N-channel	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω	–	7	–	ns
	P-channel	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω	–	6	–	ns
$t_{d(off)}$	turn-off delay time					
	N-channel	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω	–	20	–	ns
	P-channel	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω	–	29	–	ns
t_f	fall time					
	N-channel	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω	–	8	–	ns
	P-channel	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω	–	16	–	ns
t_r	rise time					
	N-channel	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω	–	12	–	ns
	P-channel	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω	–	4	–	ns
t_{on}	turn-on switching time					
	N-channel	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω	–	15	–	ns
	P-channel	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω	–	10	–	ns
t_{off}	turn-off switching time					
	N-channel	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω	–	32	–	ns
	P-channel	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω	–	45	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage					
	N-channel	V_{GD} = 0; I_S = 1.25 A	–	–	1	V
	P-channel	V_{GD} = 0; I_S = −1.25 A	–	–	−1.3	V
t_{rr}	reverse recovery time					
	N-channel	I_S = 1.25 A; di/dt = −100 A/μs	–	45	–	ns
	P-channel	I_S = −1.25 A; di/dt = 100 A/μs	–	75	–	ns

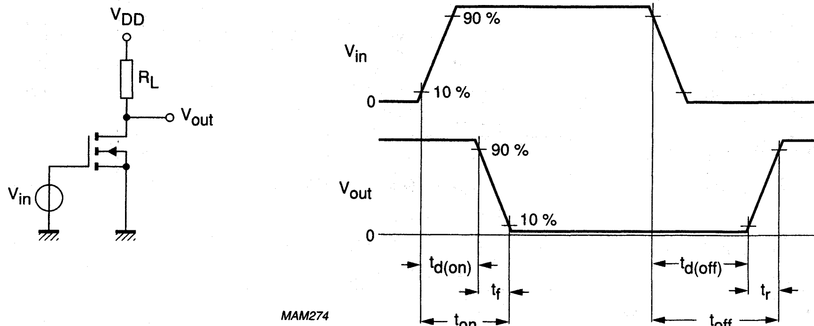


Fig.5 Switching times test circuit with input and output waveforms; N-channel.

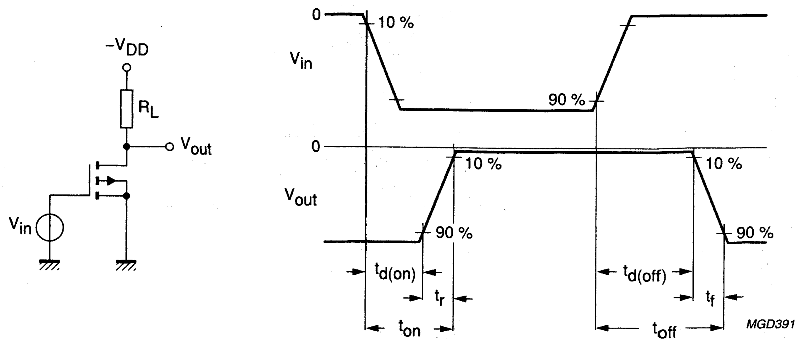
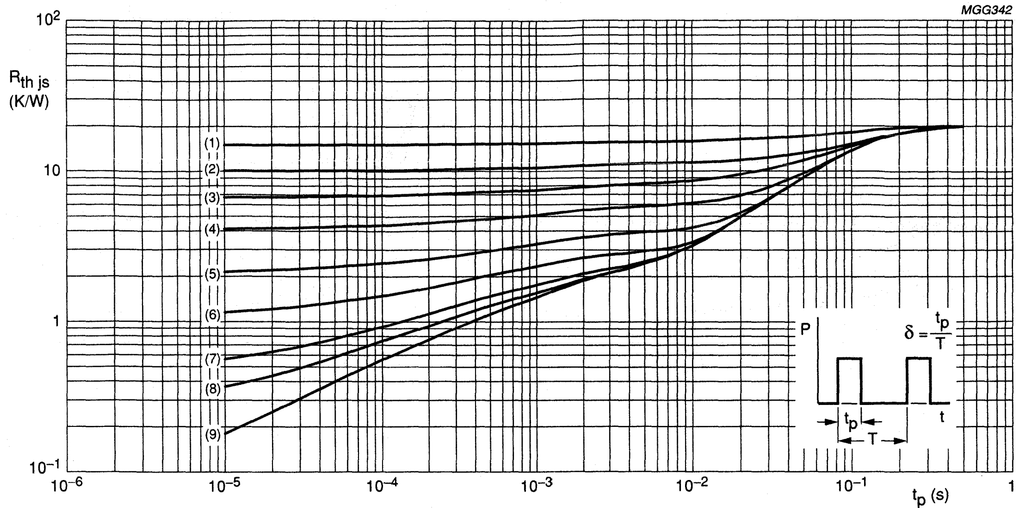


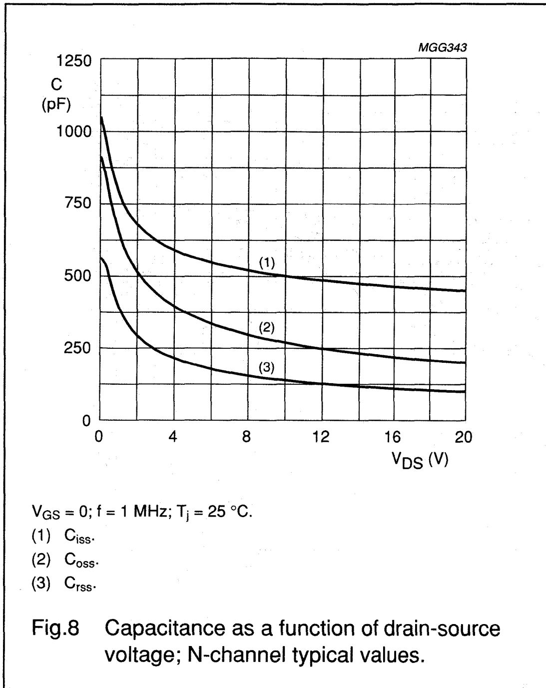
Fig.6 Switching times test circuit with input and output waveforms; P-channel.



(1) $\delta = 0.75$. (2) $\delta = 0.5$. (3) $\delta = 0.33$. (4) $\delta = 0.2$.

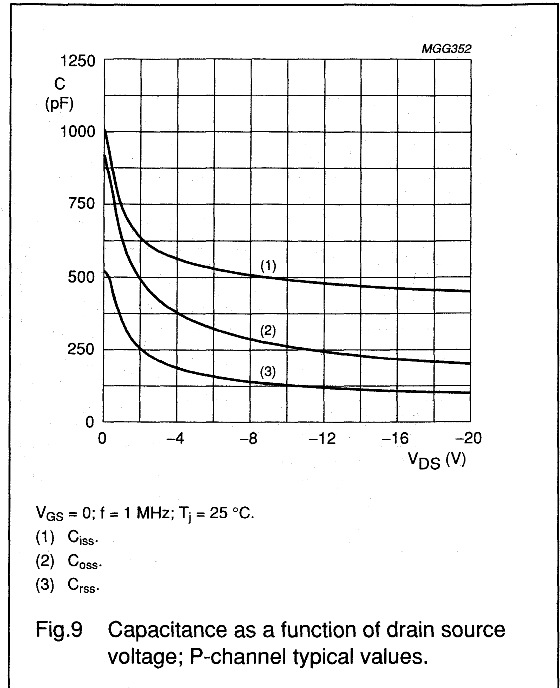
(5) $\delta = 0.1$. (6) $\delta = 0.05$. (7) $\delta = 0.02$. (8) $\delta = 0.01$. (9) $\delta = 0$.

Fig.7 Transient thermal resistance from junction to soldering point as a function of pulse time for N- and P-channels; typical values.



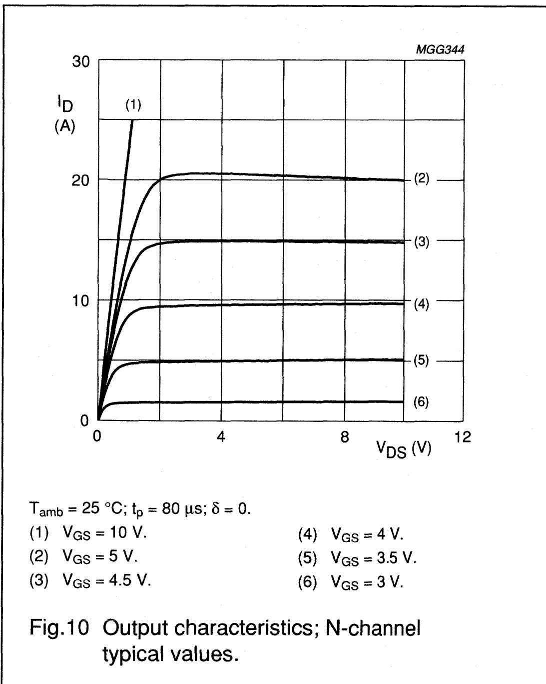
$V_{GS} = 0$; f = 1 MHz; $T_j = 25$ °C.
(1) C_{iss}.
(2) C_{oss}.
(3) C_{rss}.

Fig.8 Capacitance as a function of drain-source voltage; N-channel typical values.



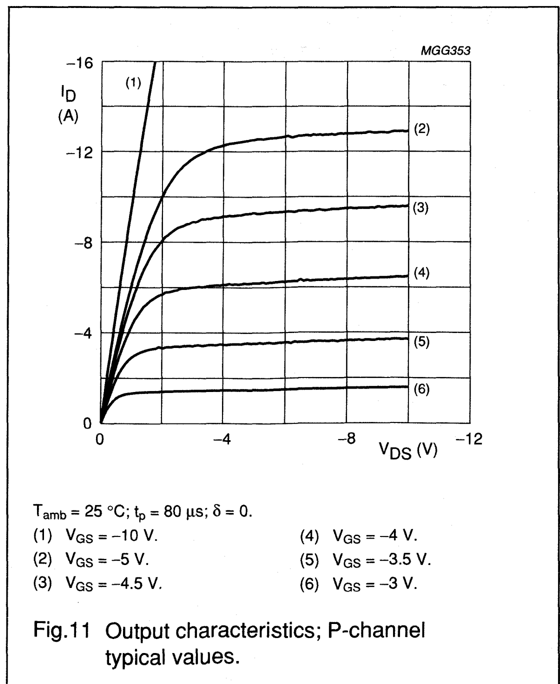
$V_{GS} = 0$; f = 1 MHz; $T_j = 25$ °C.
(1) C_{iss}.
(2) C_{oss}.
(3) C_{rss}.

Fig.9 Capacitance as a function of drain source voltage; P-channel typical values.



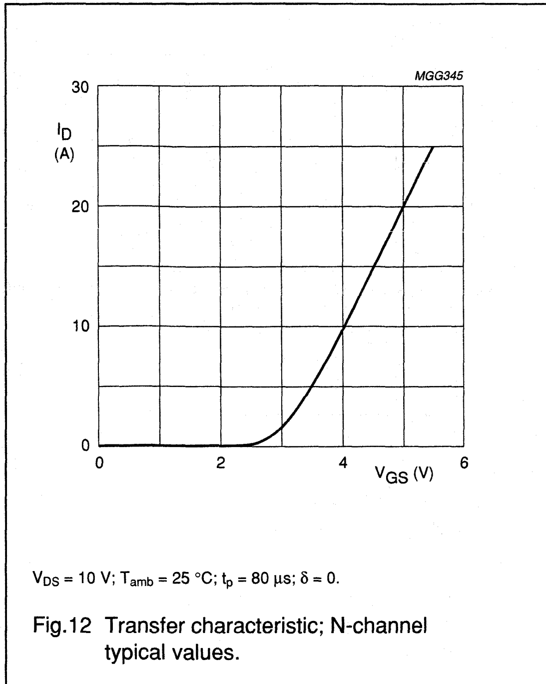
$T_{amb} = 25$ °C; $t_p = 80$ µs; $\delta = 0$.
(1) $V_{GS} = 10$ V.
(2) $V_{GS} = 5$ V.
(3) $V_{GS} = 4.5$ V.
(4) $V_{GS} = 4$ V.
(5) $V_{GS} = 3.5$ V.
(6) $V_{GS} = 3$ V.

Fig.10 Output characteristics; N-channel typical values.



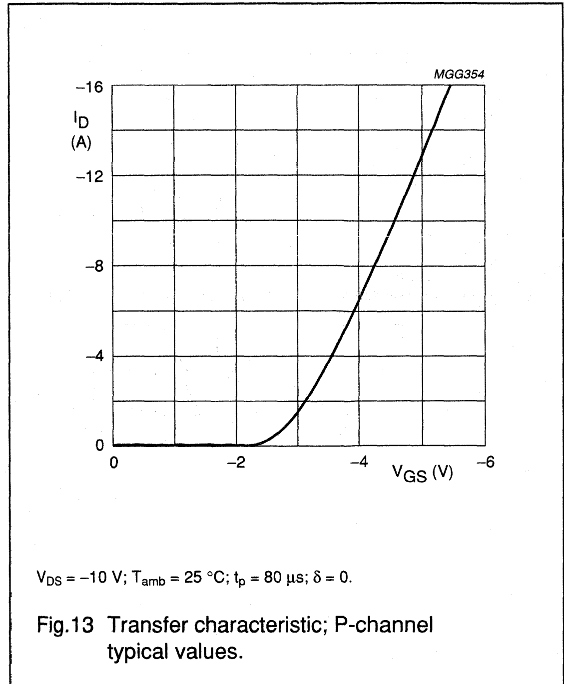
$T_{amb} = 25$ °C; $t_p = 80$ µs; $\delta = 0$.
(1) $V_{GS} = -10$ V.
(2) $V_{GS} = -5$ V.
(3) $V_{GS} = -4.5$ V.
(4) $V_{GS} = -4$ V.
(5) $V_{GS} = -3.5$ V.
(6) $V_{GS} = -3$ V.

Fig.11 Output characteristics; P-channel typical values.



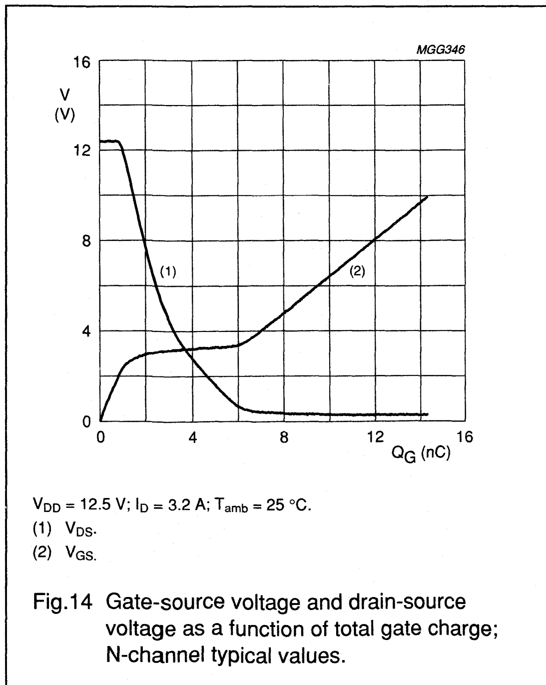
V_{DS} = 10 V; T_{amb} = 25 °C; t_p = 80 μs; δ = 0.

Fig.12 Transfer characteristic; N-channel typical values.



V_{DS} = −10 V; T_{amb} = 25 °C; t_p = 80 μs; δ = 0.

Fig.13 Transfer characteristic; P-channel typical values.

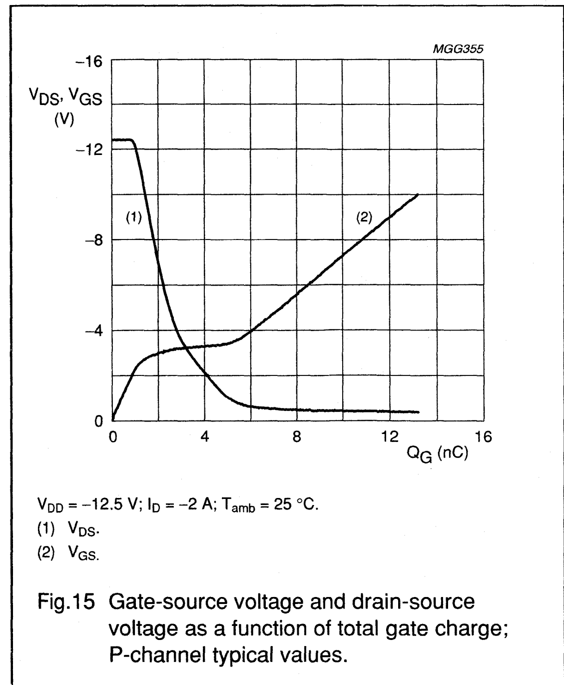


V_{DD} = 12.5 V; I_D = 3.2 A; T_{amb} = 25 °C.

(1) V_{DS}.

(2) V_{GS}.

Fig.14 Gate-source voltage and drain-source voltage as a function of total gate charge; N-channel typical values.

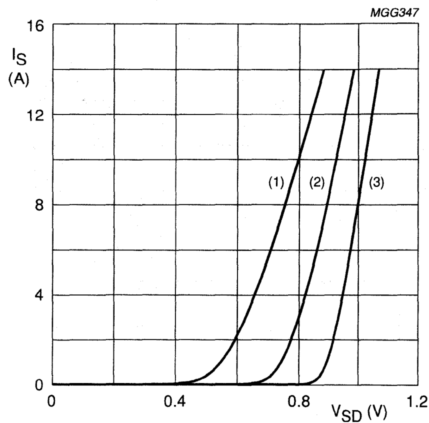


V_{DD} = −12.5 V; I_D = −2 A; T_{amb} = 25 °C.

(1) V_{DS}.

(2) V_{GS}.

Fig.15 Gate-source voltage and drain-source voltage as a function of total gate charge; P-channel typical values.



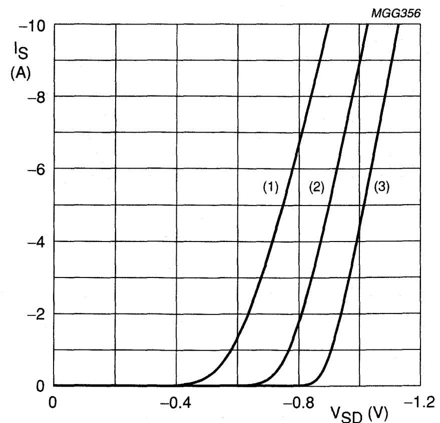
$V_{GD} = 0$.

(1) $T_{amb} = 150$ °C; $t_p = 300$ μs; $\delta = 0$.

(2) $T_{amb} = 25$ °C; $t_p = 300$ μs; $\delta = 0$.

(3) $T_{amb} = -65$ °C; $t_p = 300$ μs; $\delta = 0$.

Fig.16 Source current as a function of source-drain diode forward voltage; N-channel typical values.



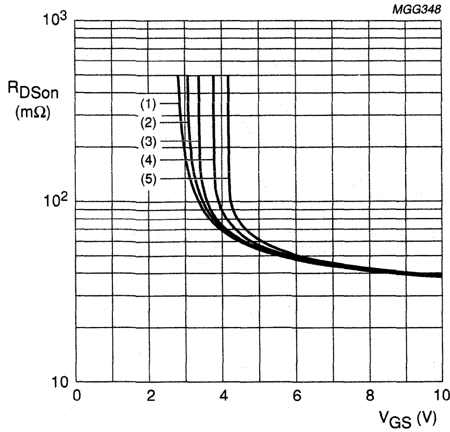
$V_{GD} = 0$.

(1) $T_{amb} = 150$ °C; $t_p = 300$ μs; $\delta = 0$.

(2) $T_{amb} = 25$ °C; $t_p = 300$ μs; $\delta = 0$.

(3) $T_{amb} = -65$ °C; $t_p = 300$ μs; $\delta = 0$.

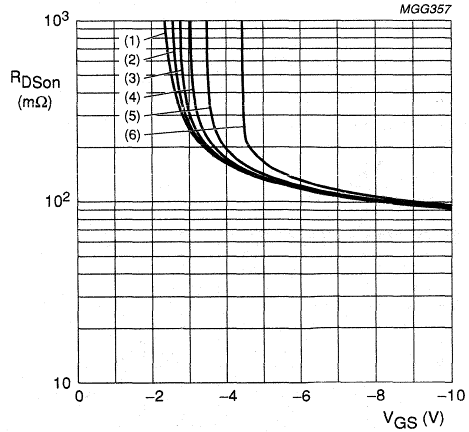
Fig.17 Source current as a function of source-drain diode forward voltage; P-channel typical values.



$V_{DS} \geq I_D \times R_{DSon}$; $T_{amb} = 25$ °C; $t_p = 300$ µs; $\delta = 0$.

(1) $I_D = 0.5$ A.
(2) $I_D = 1.6$ A.
(3) $I_D = 3.2$ A.
(4) $I_D = 6.4$ A.
(5) $I_D = 10$ A.

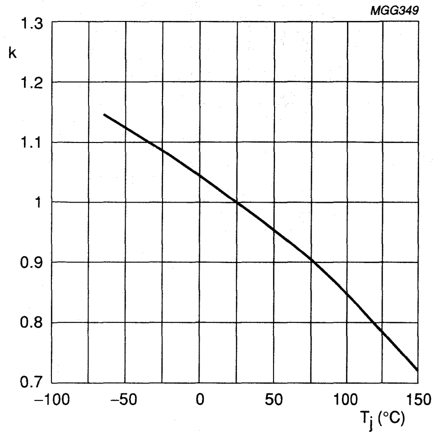
Fig.18 Drain-source on-state resistance as a function of gate-source voltage; N-channel typical values.



$V_{DS} \geq I_D \times R_{DSon}$; $T_{amb} = 25$ °C; $t_p = 300$ µs; $\delta = 0$.

(1) $I_D = 0.1$ A.
(2) $I_D = 0.5$ A.
(3) $I_D = 1$ A.
(4) $I_D = 2$ A.
(5) $I_D = 4$ A.
(6) $I_D = 8$ A.

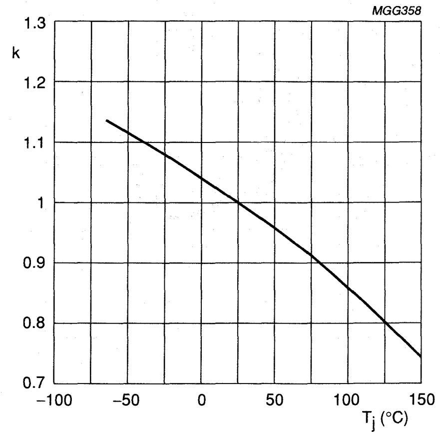
Fig.19 Drain-source on-state resistance as a function of gate-source voltage; P-channel typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; $I_D = 1$ mA.

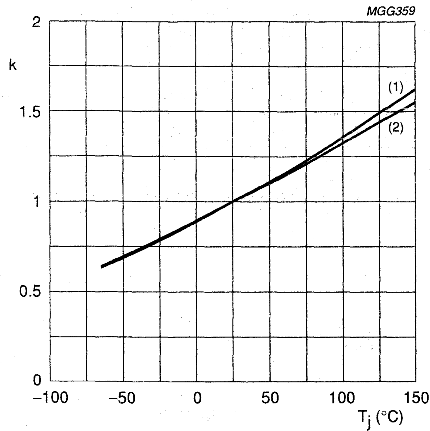
Fig.20 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; N-channel typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; $I_D = -1$ mA.

Fig.21 Temperature coefficient of gate-source threshold voltage as function of junction temperature; P-channel typical values.

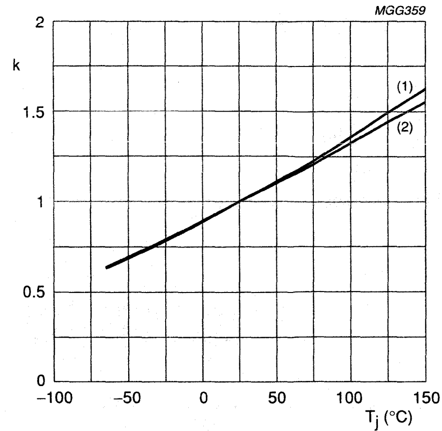


$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$

(1) R_{DSon} at V_{GS} = 10 V; I_D = 3.2 A.

(2) R_{DSon} at V_{GS} = 4.5 V; I_D = 1.6 A.

Fig.22 Temperature coefficient of drain-source on-resistance as a function of junction temperature; N-channel typical values.



$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$

(1) R_{DSon} at V_{GS} = −10 V; I_D = −2 A.

(2) R_{DSon} at V_{GS} = −4.5 V; I_D = −1 A.

Fig.23 Temperature coefficient of drain-source on-resistance as a function of junction temperature; P-channel typical values.

Complementary enhancement mode MOS transistors

PHC21025

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

One N-channel and one P-channel enhancement mode MOS transistor in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

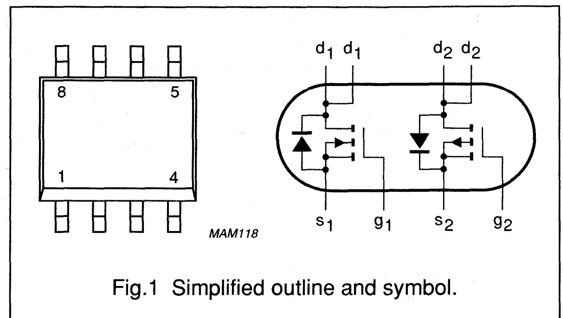


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per channel					
V_{DS}	drain-source voltage (DC)				
	N-channel		–	30	V
	P-channel		–	–30	V
V_{SD}	source-drain diode forward voltage				
	N-channel	I_S = 1.25 A	–	1.2	V
	P-channel	I_S = –1.25 A	–	–1.6	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage				V
	N-channel	$V_{DS} = V_{GS}$; I_D = 1 mA	1	2.8	V
	P-channel	$V_{DS} = V_{GS}$; I_D = –1 mA	–1	–2.8	V
I_D	drain current (DC)				
	N-channel		–	3.5	A
	P-channel		–	–2.3	A
R_{DSon}	drain-source on-state resistance				
	N-channel	V_{GS} = 10 V; I_D = 2.2 A	–	0.1	Ω
	P-channel	V_{GS} = –10 V; I_D = –1 A	–	0.25	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	2	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per channel					
V_{DS}	drain-source voltage (DC)				
	N-channel		–	30	V
	P-channel		–	–30	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)	$T_s \leq 80$ °C			
	N-channel		–	3.5	A
	P-channel		–	–2.3	A
I_{DM}	peak drain current	note 1			
	N-channel		–	14	A
	P-channel		–	–10	A
P_{tot}	total power dissipation	$T_s = 80$ °C; note 2	–	2	W
		$T_{amb} = 25$ °C; note 3	–	2	W
		$T_{amb} = 25$ °C; note 4	–	1	W
		$T_{amb} = 25$ °C; note 5	–	1.3	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C
Source-drain diode					
I_S	source current (DC)	$T_s \leq 80$ °C			
	N-channel		–	1.5	A
	P-channel		–	–1.25	A
I_{SM}	peak pulsed source current	note 1			
	N-channel		–	6	A
	P-channel		–	–5	A

Notes

1. Pulse width and duty cycle limited by maximum junction temperature.
2. Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 2 W at the same time.
3. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.
5. Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

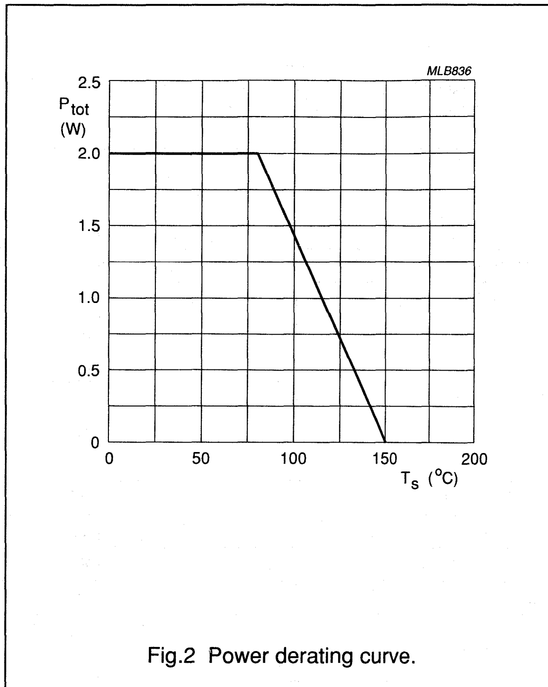
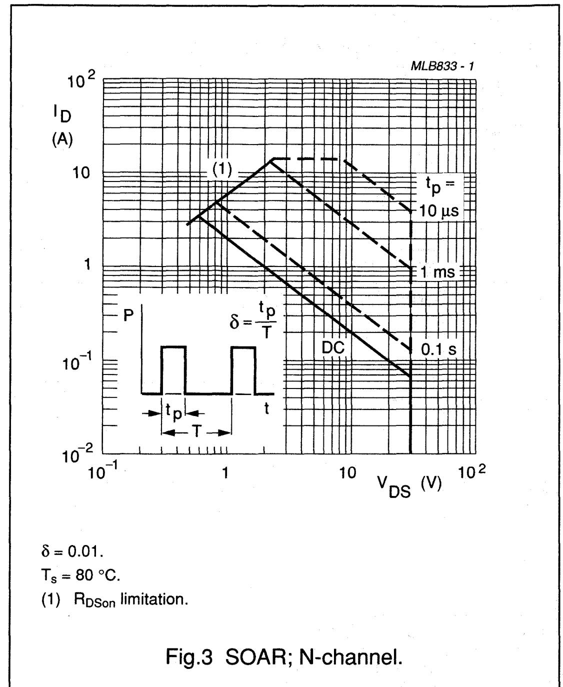
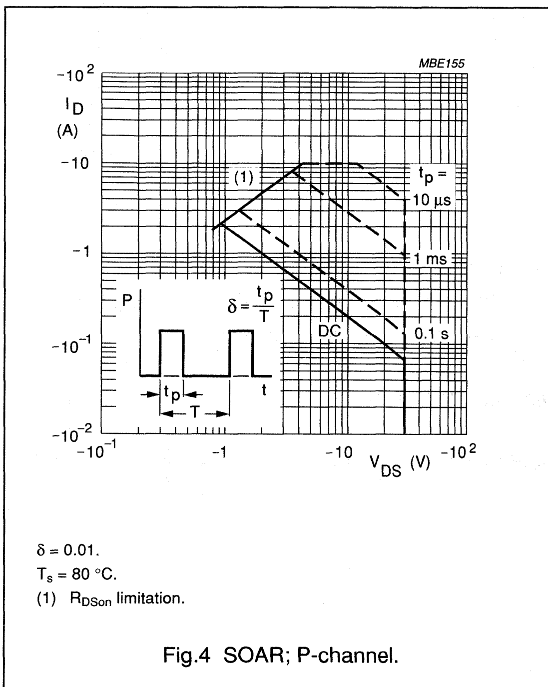


Fig.2 Power derating curve.



$\delta = 0.01$.
$T_s = 80$ °C.
(1) R_{DSon} limitation.

Fig.3 SOAR; N-channel.



$\delta = 0.01$.
$T_s = 80$ °C.
(1) R_{DSon} limitation.

Fig.4 SOAR; P-channel.

THERMAL CHARACTERISTICS

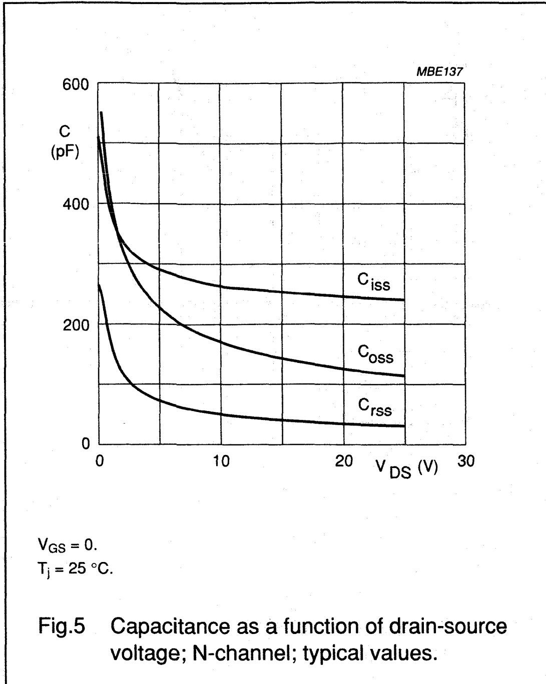
SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	35	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

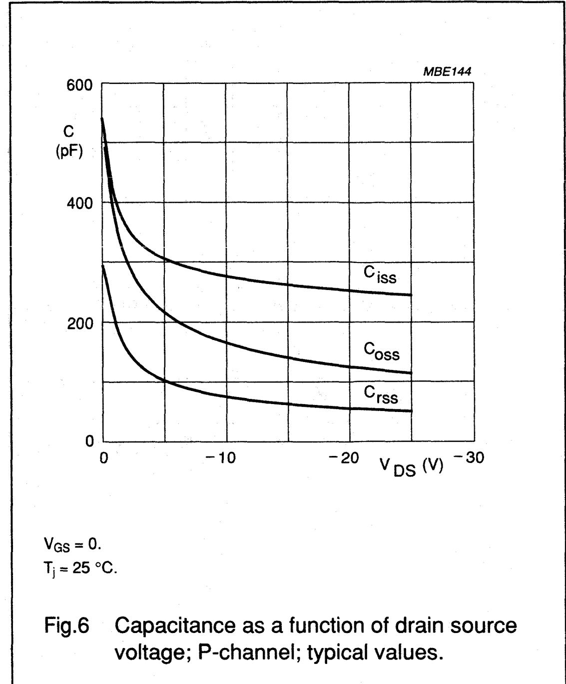
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per channel						
$V_{(BR)DSS}$	drain-source breakdown voltage					
	N-channel	V_{GS} = 0; I_D = 10 μA	30	–	–	V
	P-channel	V_{GS} = 0; I_D = –10 μA	–30	–	–	V
V_{GSth}	gate-source threshold voltage					
	N-channel	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
	P-channel	V_{GS} = V_{DS}; I_D = –1 mA	–1	–	–2.8	V
I_{DSS}	drain-source leakage current					
	N-channel	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
	P-channel	V_{GS} = 0; V_{DS} = –24 V	–	–	–100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0				
	N-channel		–	–	±100	nA
	P-channel		–	–	±100	nA
I_{Don}	on-state drain current					
	N-channel	V_{GS} = 10 V; V_{DS} = 1 V	3.5	–	–	A
		V_{GS} = 4.5 V; V_{DS} = 5 V	2	–	–	A
	P-channel	V_{GS} = –10 V; V_{DS} = –1 V	–2.3	–	–	A
		V_{GS} = –4.5 V; V_{DS} = –5 V	–1	–	–	A
R_{DSon}	drain-source on-state resistance					
	N-channel	V_{GS} = 4.5 V; I_D = 1 A	–	0.11	0.2	Ω
		V_{GS} = 10 V; I_D = 2.2 A	–	0.08	0.1	Ω
	P-channel	V_{GS} = –4.5 V; I_D = – 0.5 A	–	0.33	0.4	Ω
		V_{GS} = –10 V; I_D = –1 A	–	0.22	0.25	Ω
$\|y_{fs}\|$	forward transfer admittance					
	N-channel	V_{DS} = 20 V; I_D = 2.2 A	2	4.5	–	S
	P-channel	V_{DS} = –20 V; I_D = –1 A	1	2	–	S
C_{iss}	input capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	250	–	pF
	P-channel	V_{GS} = 0; V_{DS} = –20 V; f = 1 MHz	–	250	–	pF
C_{oss}	output capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	140	–	pF
	P-channel	V_{GS} = 0; V_{DS} = –20 V; f = 1 MHz	–	140	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{rss}	reverse transfer capacitance					
	N-channel	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	50	–	pF
	P-channel	V_{GS} = 0; V_{DS} = –20 V; f = 1 MHz	–	50	–	pF
Q_G	total gate charge					
	N-channel	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	10	30	nC
	P-channel	V_{GS} = –10 V; V_{DS} = –15 V; I_D = –2.3 A	–	10	25	nC
Q_{GS}	gate-source charge					
	N-channel	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	1	–	nC
	P-channel	V_{GS} = –10 V; V_{DS} = –15 V; I_D = –2.3 A	–	1	–	nC
Q_{GD}	gate-drain charge					
	N-channel	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	2.5	–	nC
	P-channel	V_{GS} = –10 V; V_{DS} = –15 V; I_D = –2.3 A	–	3	–	nC
Switching times						
t_{on}	turn-on time					
	N-channel	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 1 A; R_L = 20 Ω	–	15	40	ns
	P-channel	V_{GS} = 0 to –10 V; V_{DD} = –20 V; I_D = –1 A; R_L = 20 Ω	–	20	80	ns
t_{off}	turn-off time					
	N-channel	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_L = 20 Ω	–	25	140	ns
	P-channel	V_{GS} = –10 to 0 V; V_{DD} = –20 V; I_D = –1 A; R_L = 20 Ω	–	50	140	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage					
	N-channel	V_{GD} = 0; I_S = 1.25 A	–	–	1.2	V
	P-channel	V_{GD} = 0; I_S = –1.25 A	–	–	–1.6	V
t_{rr}	reverse recovery time					
	N-channel	I_S = 1.25 A; di/dt = 100 A/µs	–	35	100	ns
	P-channel	I_S = –1.25 A; di/dt = 100 A/µs	–	150	200	ns



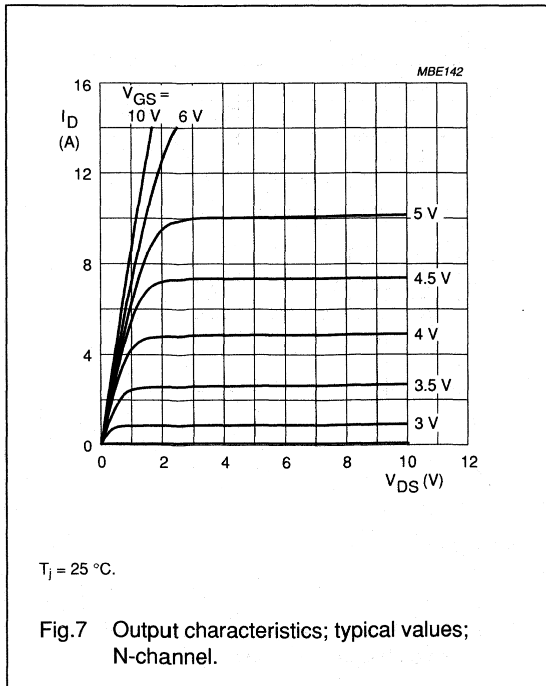
V_{GS} = 0.
T_j = 25 °C.

Fig.5 Capacitance as a function of drain-source voltage; N-channel; typical values.



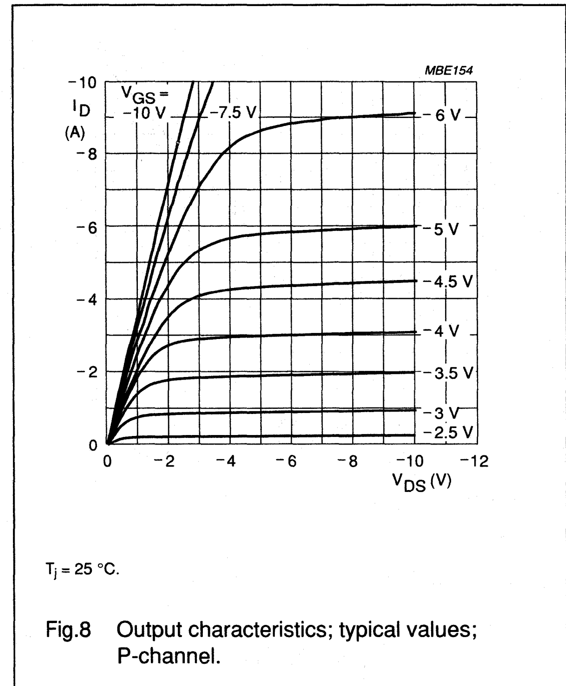
V_{GS} = 0.
T_j = 25 °C.

Fig.6 Capacitance as a function of drain source voltage; P-channel; typical values.



T_j = 25 °C.

Fig.7 Output characteristics; typical values; N-channel.

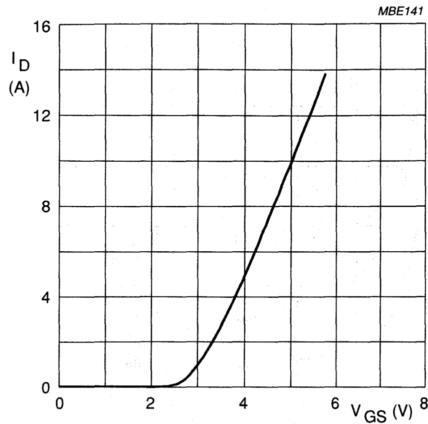


T_j = 25 °C.

Fig.8 Output characteristics; typical values; P-channel.

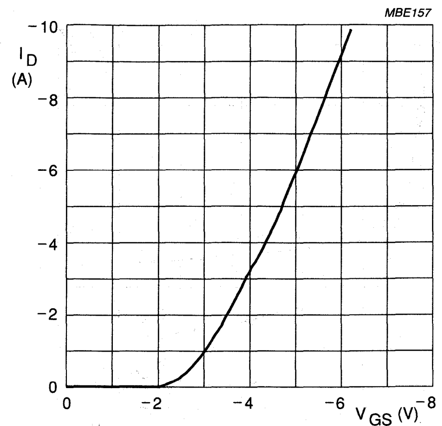
Complementary enhancement mode MOS transistors

PHC21025



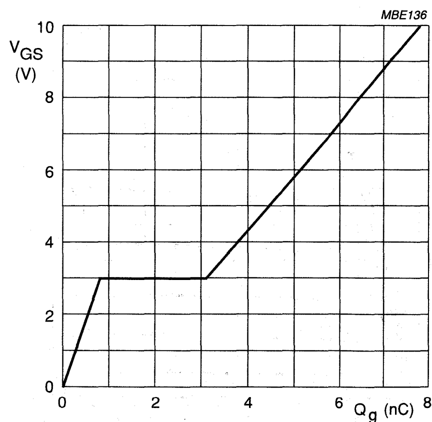
V_{DS} = 10 V.
T_j = 25 °C.

Fig.9 Transfer characteristic; typical values; N-channel.



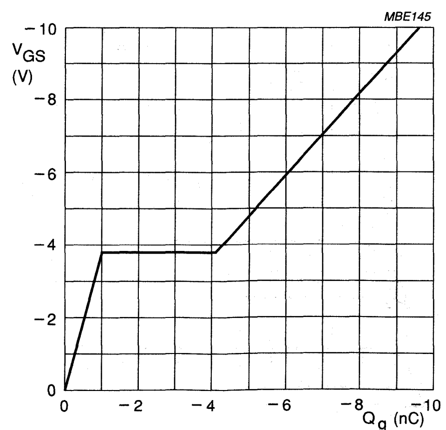
V_{DS} = −10 V.
T_j = 25 °C.

Fig.10 Transfer characteristic; typical values; P-channel.



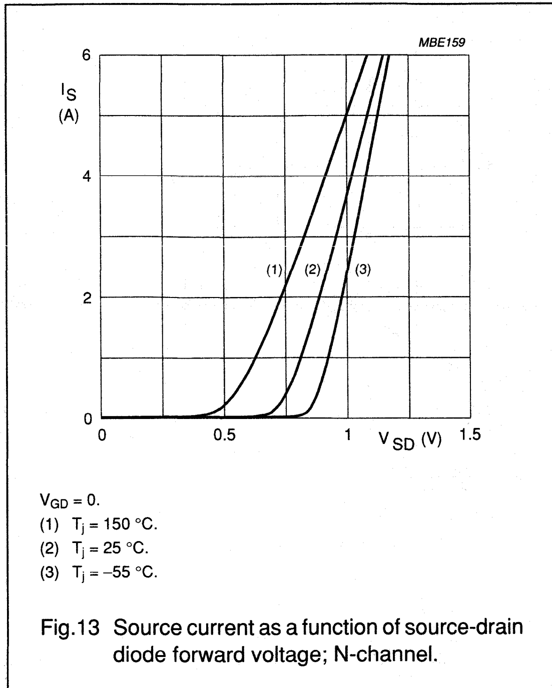
V_{DD} = 15 V.
I_D = 3.5 A.

Fig.11 Gate-source voltage as a function of total gate charge; N-channel.



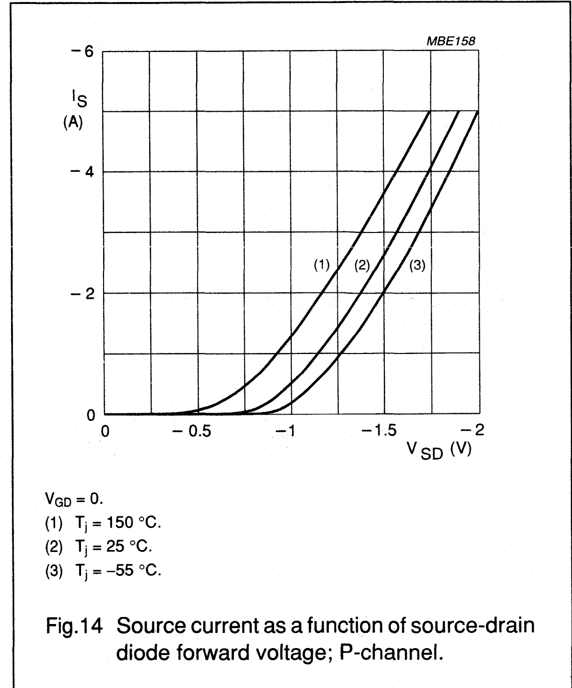
V_{DD} = −15 V.
I_D = −2.3 A.

Fig.12 Gate-source voltage as a function of total gate charge; P-channel.



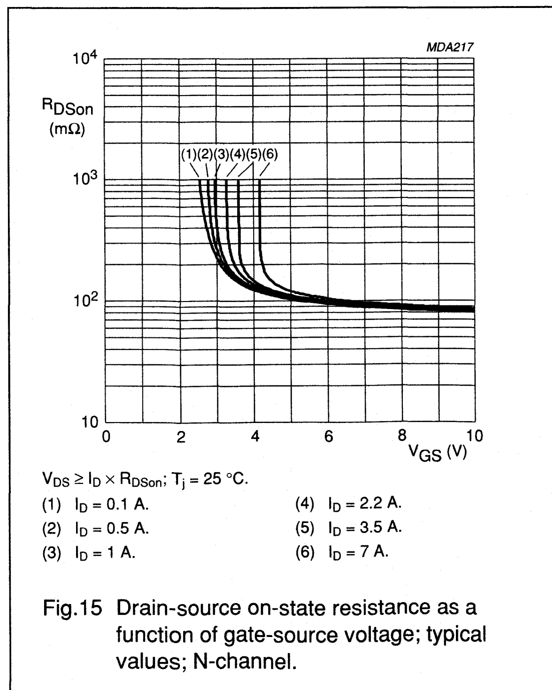
V_{GD} = 0.
(1) T_j = 150 °C.
(2) T_j = 25 °C.
(3) T_j = −55 °C.

Fig.13 Source current as a function of source-drain diode forward voltage; N-channel.



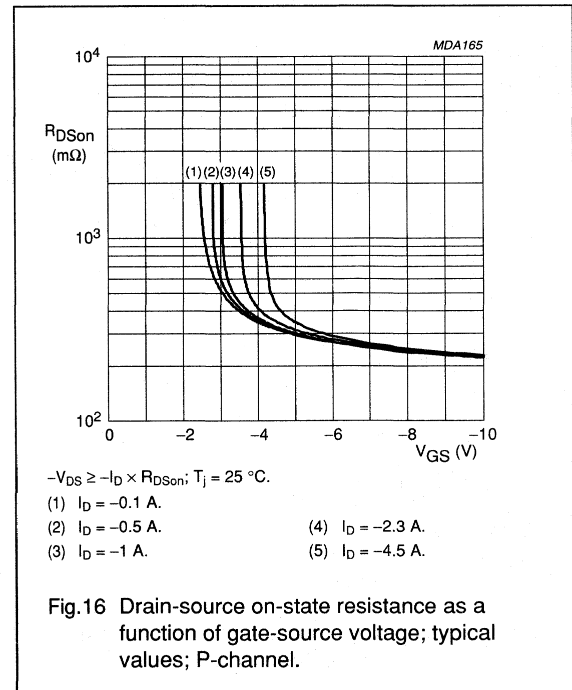
V_{GD} = 0.
(1) T_j = 150 °C.
(2) T_j = 25 °C.
(3) T_j = −55 °C.

Fig.14 Source current as a function of source-drain diode forward voltage; P-channel.



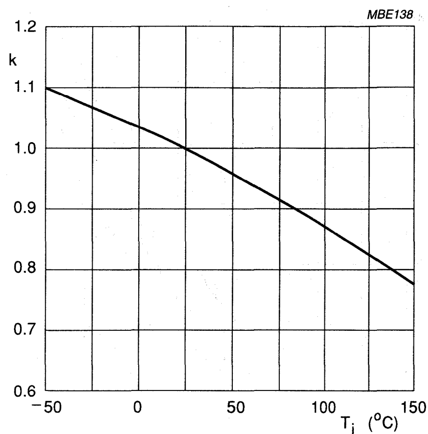
$V_{DS} \geq I_D \times R_{DSon}$; T_j = 25 °C.
(1) I_D = 0.1 A.
(2) I_D = 0.5 A.
(3) I_D = 1 A.
(4) I_D = 2.2 A.
(5) I_D = 3.5 A.
(6) I_D = 7 A.

Fig.15 Drain-source on-state resistance as a function of gate-source voltage; typical values; N-channel.



$-V_{DS} \geq -I_D \times R_{DSon}$; T_j = 25 °C.
(1) I_D = −0.1 A.
(2) I_D = −0.5 A.
(3) I_D = −1 A.
(4) I_D = −2.3 A.
(5) I_D = −4.5 A.

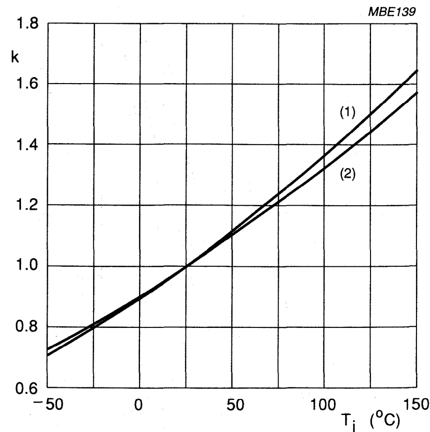
Fig.16 Drain-source on-state resistance as a function of gate-source voltage; typical values; P-channel.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25\,°C}$$

Typical V_{GSth} at I_D = 1 mA; V_{DS} = V_{GS} = V_{GSth}.

Fig.17 Temperature coefficient of gate-source threshold voltage; N and P-channels.



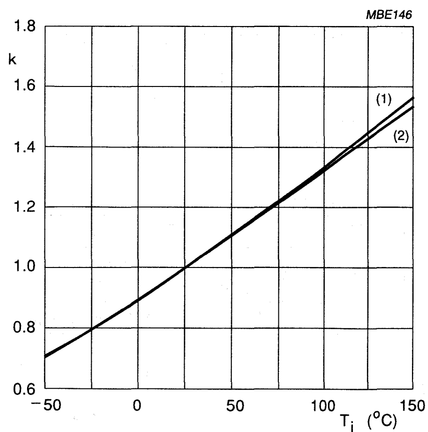
$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\,°C}$$

Typical R_{DSon} at:

(1) I_D = 2.2 A; V_{GS} = 10 V.

(2) I_D = 1 A; V_{GS} = 4.5 V.

Fig.18 Temperature coefficient of drain-source on-resistance; N-channel.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\,°C}$$

Typical R_{DSon} at:

(1) I_D = −1 A; V_{GS} = −10 V.

(2) I_D = −0.5 A; V_{GS} = −4.5 V.

Fig.19 Temperature coefficient of drain-source on-resistance; P-channel.

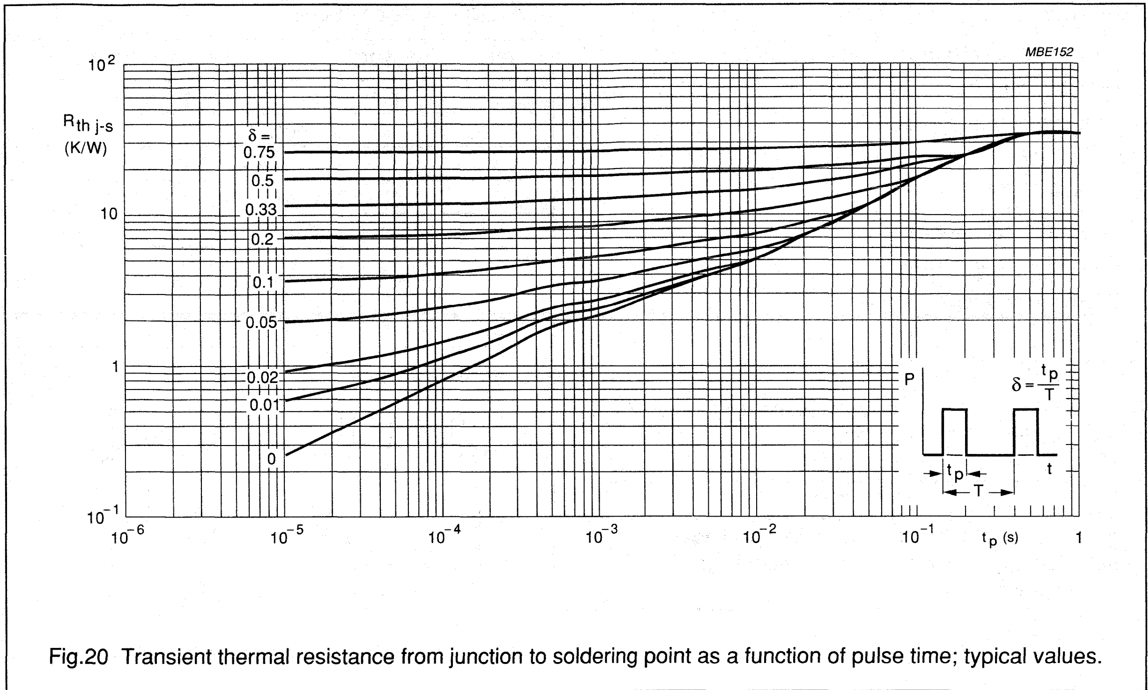


Fig.20 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

N-channel enhancement mode MOS transistor

PHN103

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-state resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

N-channel enhancement mode MOS transistor in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	n.c	not connected
2	s	source
3	s	source
4	g	gate
5	d	drain
6	d	drain
7	d	drain
8	d	drain

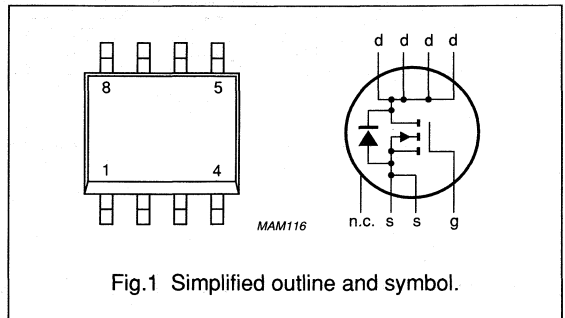


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{SD}	source-drain diode forward voltage	I_S = 1.25 A	–	1	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; $V_{DS} = V_{GS}$	1	2.8	V
I_D	drain current (DC)	T_s = 80 °C	–	8.5	A
R_{DSon}	drain-source on-state resistance	I_D = 5.5 A; V_{GS} = 10 V	–	0.03	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	4	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	8.5	A
I_{DM}	peak drain current	note 2	–	35	A
P_{tot}	total power dissipation	T_s = 80 °C	–	4	W
		T_{amb} = 25 °C; note 3	–	2.7	W
		T_{amb} = 25 °C; note 4	–	1.15	W
T_{stg}	storage temperature		−65	+150	°C
T_j	operating junction temperature		−65	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	5	A
I_{SM}	peak pulsed source current	note 2	–	20	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	17.5	K/W

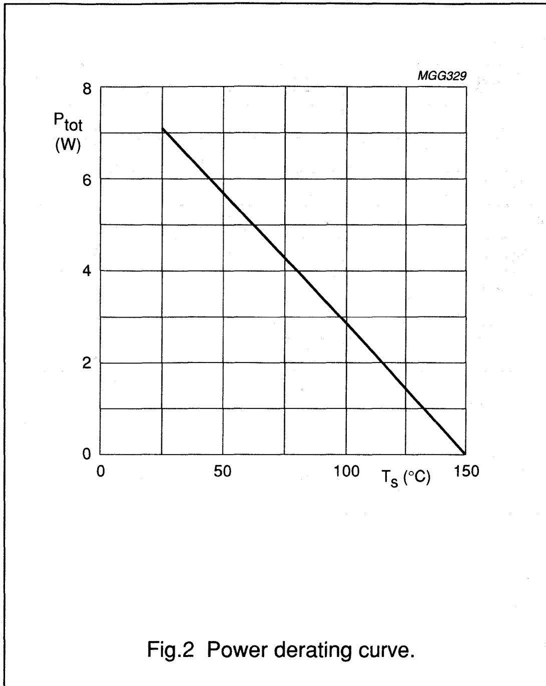
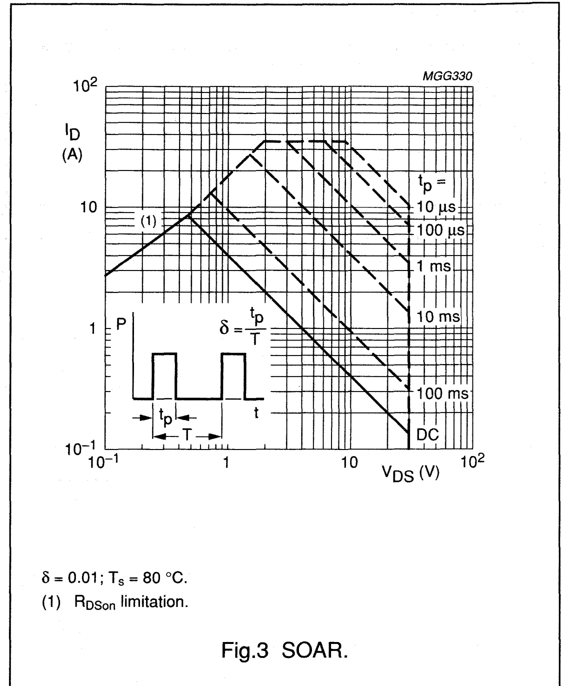


Fig.2 Power derating curve.



$\delta = 0.01$; $T_s = 80$ °C.

(1) R_{DSon} limitation.

Fig.3 SOAR.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 2.75 A	–	–	0.05	Ω
		V_{GS} = 10 V; I_D = 5.5 A	–	–	0.03	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	750	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	520	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	200	–	pF
Q_G	total gate charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 4 A	–	25	40	nC
Q_{GS}	gate-source charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 4 A	–	3	–	nC
Q_{GD}	gate-drain charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 4 A	–	7.5	–	nC
Switching times (see Fig.4)						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	7	–	ns
t_r	rise time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	10	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	17	35	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	35	–	ns
t_f	fall time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	40	–	ns
t_{off}	turn-off switching time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	75	150	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 1.25 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 1.25 A; di/dt = 100 A/μs	–	70	–	ns

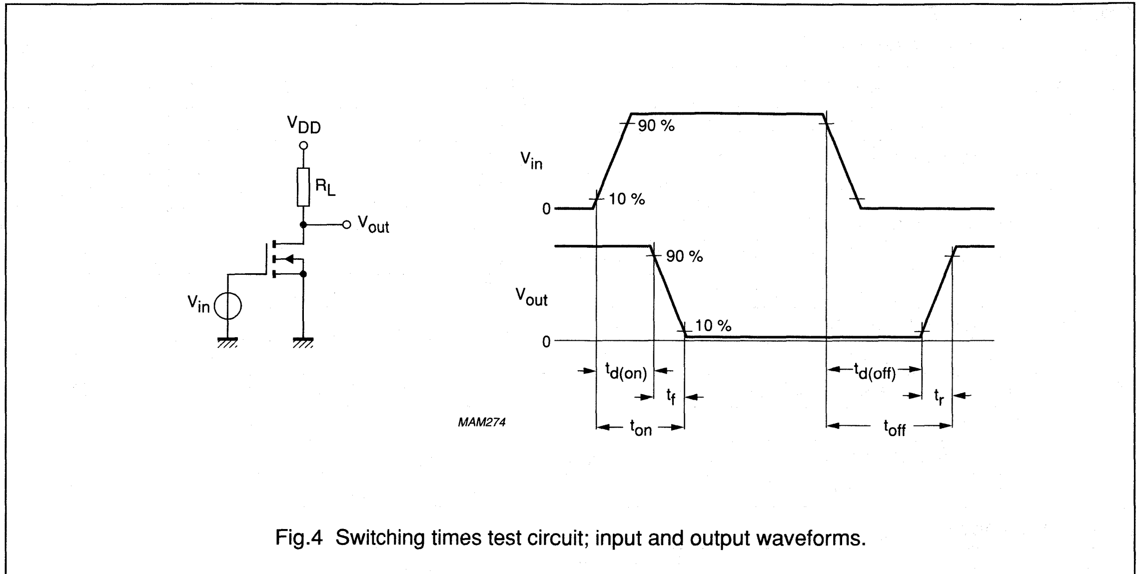


Fig.4 Switching times test circuit; input and output waveforms.

MGG331

$R_{th\ j-s}$ (K/W)

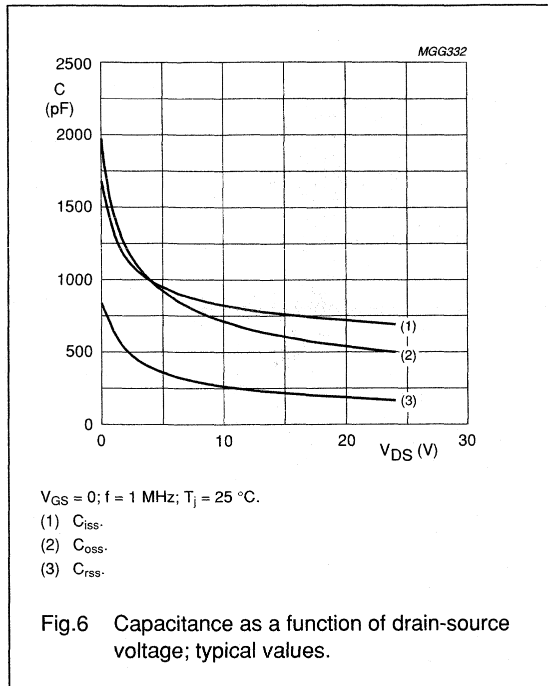
t_p (s)

$\delta = \frac{t_p}{T}$

(1) δ = 0.75. (2) δ = 0.5. (3) δ = 0.33. (4) δ = 0.2.

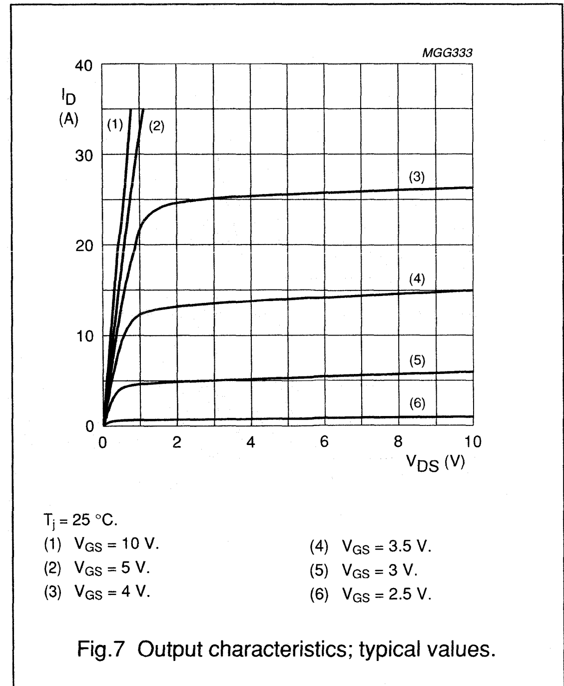
(5) δ = 0.1. (6) δ = 0.05. (7) δ = 0.02. (8) δ = 0.01. (9) δ = 0.

Fig.5 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.



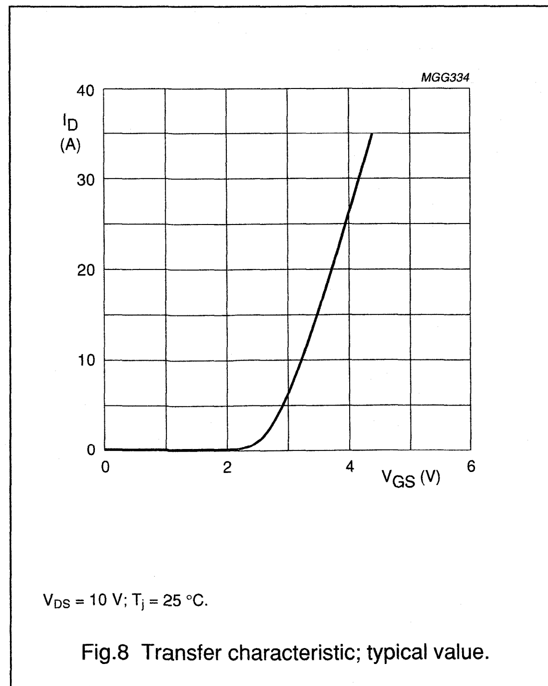
$V_{GS} = 0$; f = 1 MHz; $T_j = 25$ °C.
(1) C_{iss}.
(2) C_{oss}.
(3) C_{rss}.

Fig.6 Capacitance as a function of drain-source voltage; typical values.



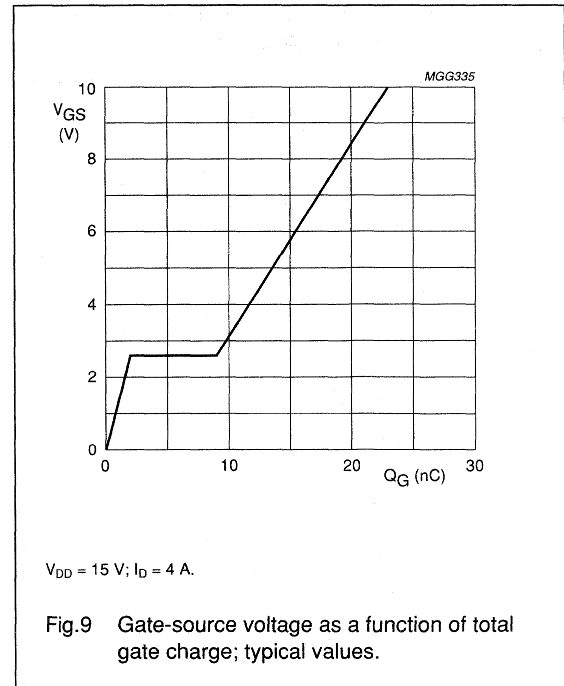
$T_j = 25$ °C.
(1) $V_{GS} = 10$ V.
(2) $V_{GS} = 5$ V.
(3) $V_{GS} = 4$ V.
(4) $V_{GS} = 3.5$ V.
(5) $V_{GS} = 3$ V.
(6) $V_{GS} = 2.5$ V.

Fig.7 Output characteristics; typical values.



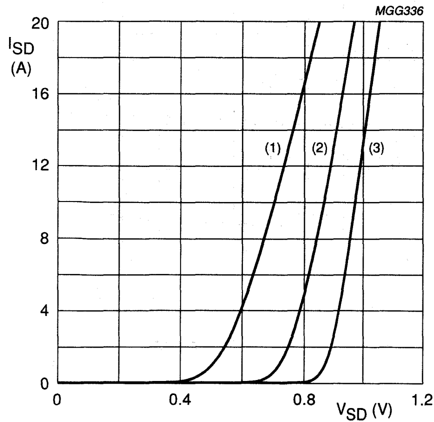
$V_{DS} = 10$ V; $T_j = 25$ °C.

Fig.8 Transfer characteristic; typical value.



$V_{DD} = 15$ V; $I_D = 4$ A.

Fig.9 Gate-source voltage as a function of total gate charge; typical values.



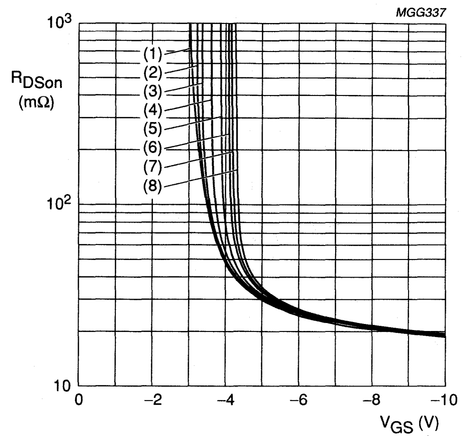
$V_{GD} = 0$.

(1) $T_j = 150$ °C.

(2) $T_j = 25$ °C.

(3) $T_j = -65$ °C.

Fig.10 Source current as a function of source-drain diode forward voltage; typical values.



$V_{DS} \geq I_D \times R_{DSon}$; $T_j = 25$ °C.

(1) $I_D = 0.1$ A.

(2) $I_D = 0.5$ A.

(3) $I_D = 1.0$ A.

(4) $I_D = 2.75$ A.

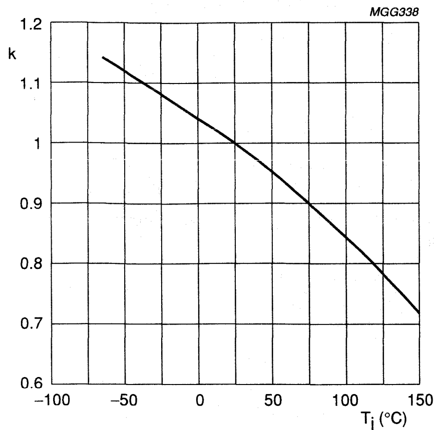
(5) $I_D = 5.5$ A.

(6) $I_D = 8.5$ A.

(7) $I_D = 10$ A.

(8) $I_D = 12$ A.

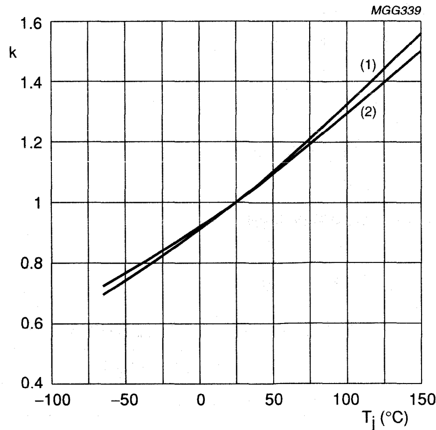
Fig.11 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25 °C}$$

V_{GSth} at $V_{DS} = V_{GS}$; $I_D = 1$ mA.

Fig.12 Temperature coefficient of gate-source threshold voltage; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25 °C}$$

(1) R_{DSon} at $V_{GS} = 10$ V; $I_D = 5.5$ A.

(2) R_{DSon} at $V_{GS} = 4.5$ V; $I_D = 2.75$ A.

Fig.13 Temperature coefficient of drain-source on-state resistance; typical values.

N-channel enhancement mode MOS transistor

PHN110

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	n.c	not connected
2	s	source
3	s	source
4	g	gate
5	d	drain
6	d	drain
7	d	drain
8	d	drain

DESCRIPTION

N-channel enhancement mode MOS transistor in an 8-pin plastic SOT96-1 (SO8) package.

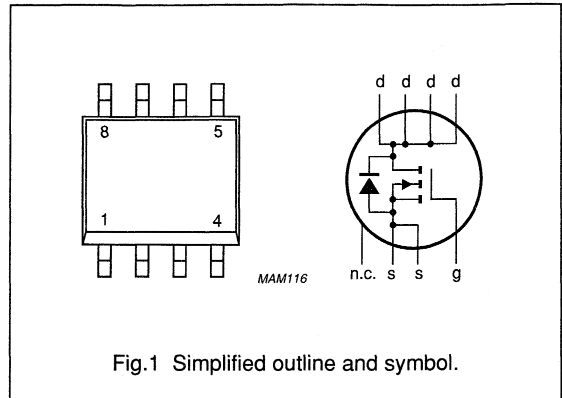


Fig.1 Simplified outline and symbol.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{SD}	source-drain diode forward voltage	I_S = 1.25 A	–	1.2	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; $V_{DS} = V_{GS}$	1	2.8	V
I_D	drain current (DC)	T_s = 80 °C	–	4	A
R_{DSon}	drain-source on-state resistance	I_D = 2.2 A; V_{GS} = 10 V	–	0.1	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	2.8	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	4	A
I_{DM}	peak drain current	note 2	–	16	A
P_{tot}	total power dissipation	T_s = 80 °C	–	2.8	W
		T_{amb} = 25 °C; note 3	–	2.4	W
		T_{amb} = 25 °C; note 4	–	1.1	W
T_{stg}	storage temperature		−65	+150	°C
T_j	operating junction temperature		−65	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	3.5	A
I_{SM}	peak pulsed source current	note 2	–	14	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Value based on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Value based on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

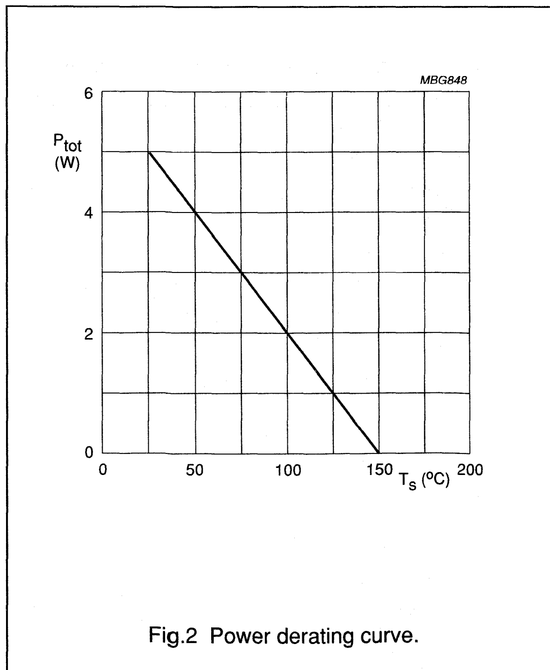
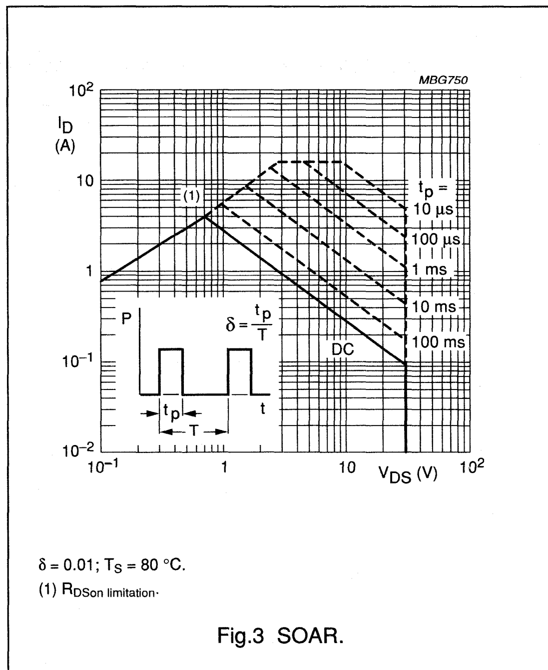


Fig.2 Power derating curve.



δ = 0.01; T_S = 80 °C.

(1) R_{DSon} limitation.

Fig.3 SOAR.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	25	K/W

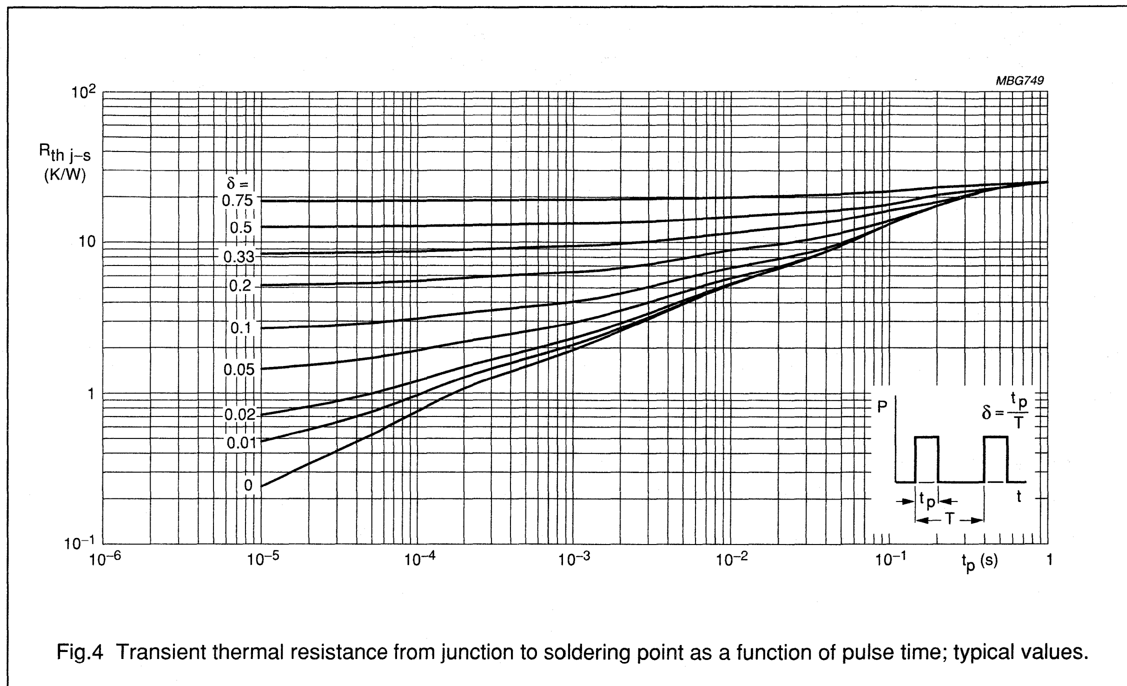
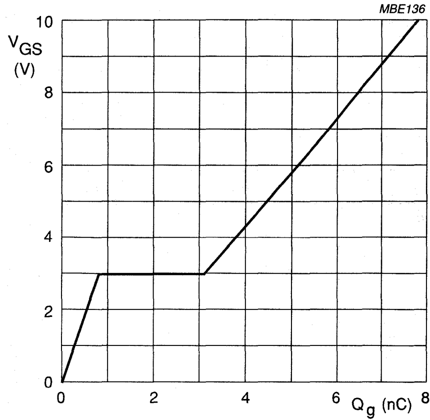


Fig.4 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

CHARACTERISTICS

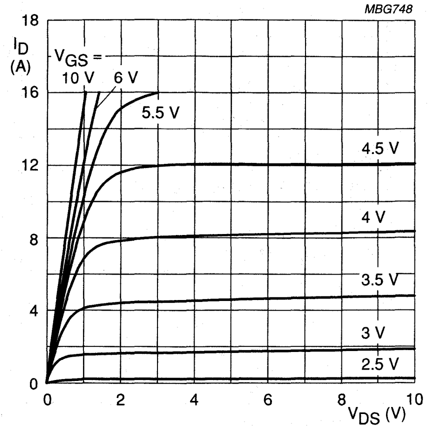
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 1 A	–	0.11	0.2	Ω
		V_{GS} = 10 V; I_D = 2 A	–	0.08	0.1	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	250	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	140	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	50	–	pF
Q_g	total gate charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 2 A	–	10	30	nC
Q_{gs}	gate-source charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 2 A	–	1	–	nC
Q_{gd}	gate-drain charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 2 A	–	2.5	–	nC
Switching times (see Fig.11)						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	4.5	–	ns
t_f	fall time		–	3.5	–	ns
t_{on}	turn-on switching time		–	8	16	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	15	–	ns
t_r	rise time		–	10	–	ns
t_{off}	turn-off switching time		–	25	50	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 1.25 A	–	–	1.2	V
t_{rr}	reverse recovery time	I_S = 1.25 A; di/dt = −100 A/μs	–	35	100	ns



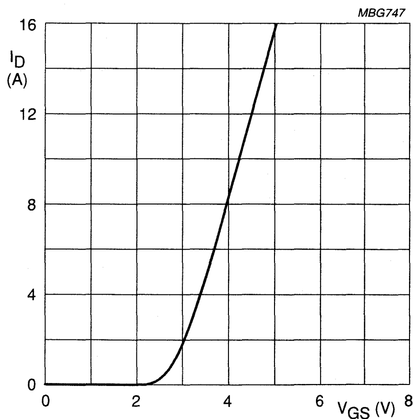
V_{DD} = 15 V: I_D = 2 A.

Fig.5 Gate-source voltage as a function of total gate charge; typical values.



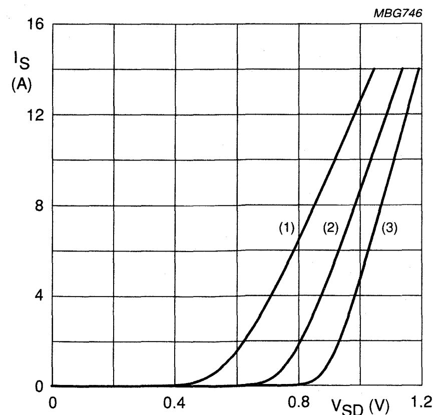
T_j = 25 °C.

Fig.6 Output characteristics; typical values.



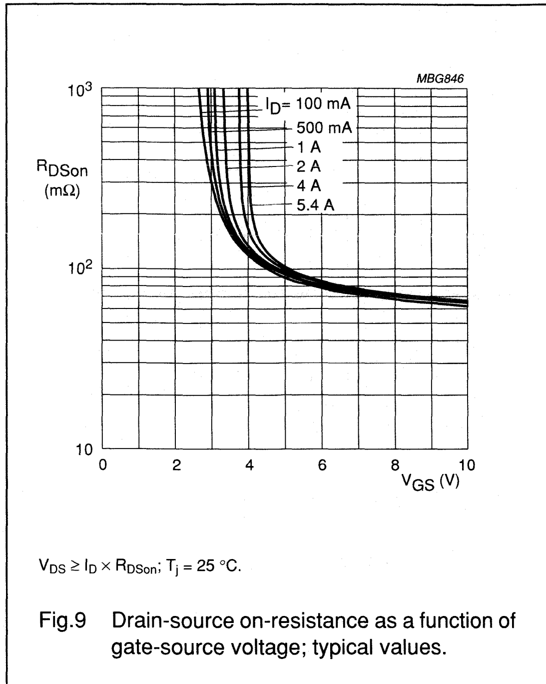
V_{DS} = 10 V; T_j = 25 °C.

Fig.7 Transfer characteristics; typical values.



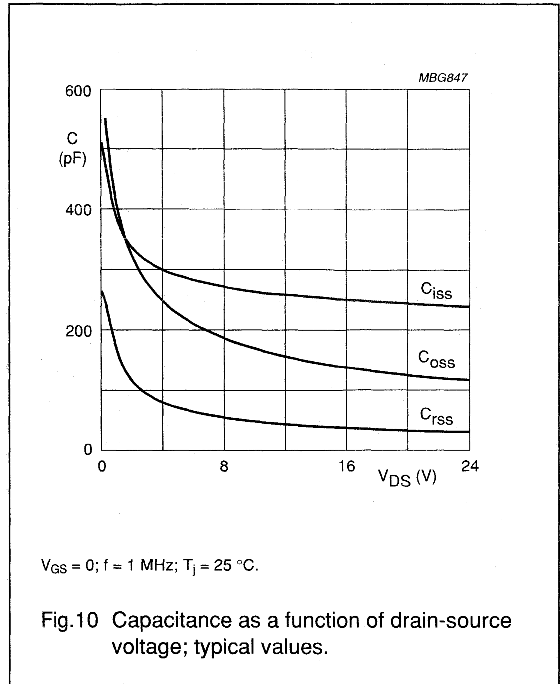
V_{GD} = 0.
(1) T_j = 150 °C.
(2) T_j = 25 °C.
(3) T_j = −65 °C.

Fig.8 Source current as a function of source-drain diode forward voltage; typical values.



$V_{DS} \geq I_D \times R_{DSon}$; T_j = 25 °C.

Fig.9 Drain-source on-resistance as a function of gate-source voltage; typical values.



V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.10 Capacitance as a function of drain-source voltage; typical values.

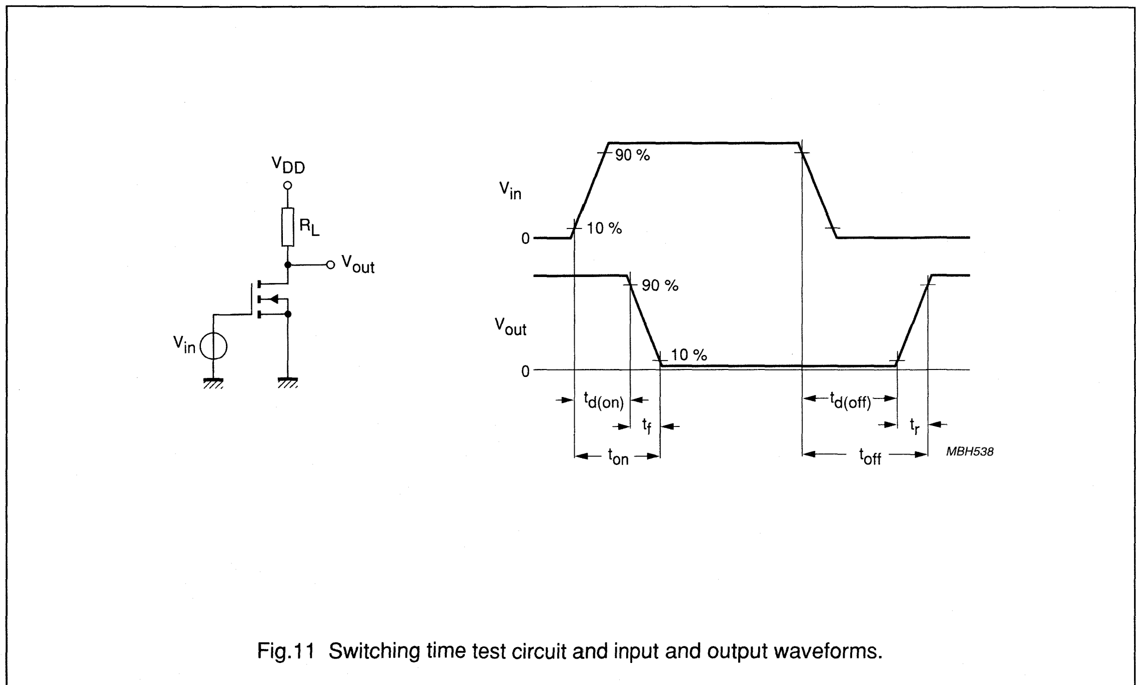
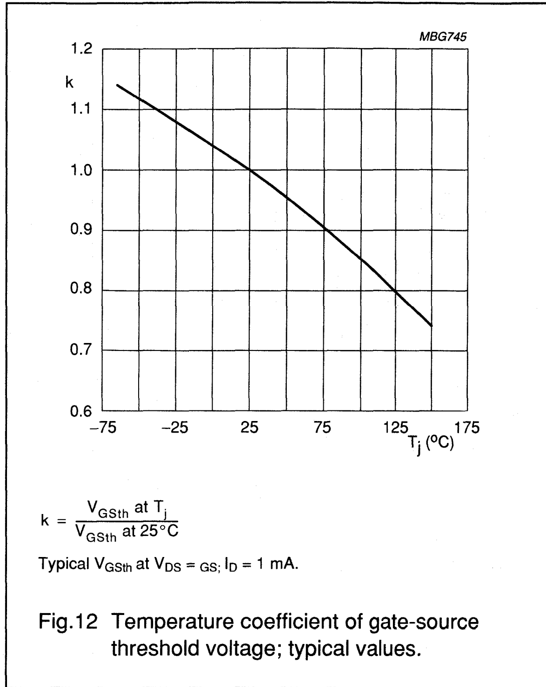


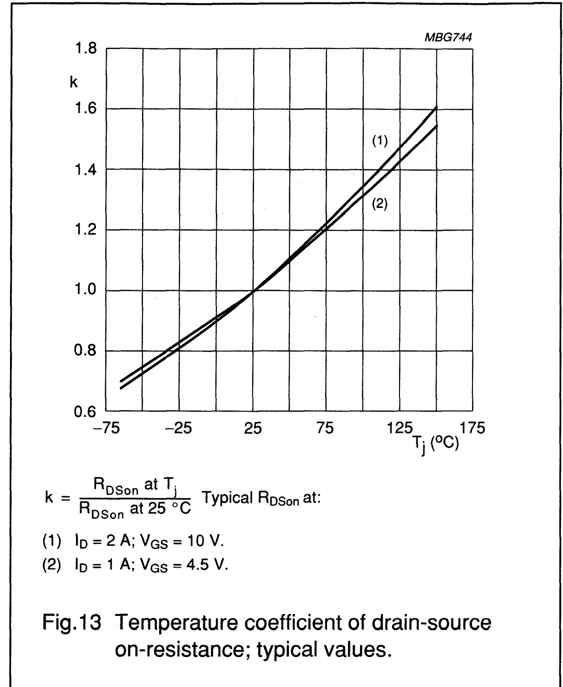
Fig.11 Switching time test circuit and input and output waveforms.



$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$

Typical V_{GSth} at $V_{DS} = _{GS}$; $I_D = 1$ mA.

Fig.12 Temperature coefficient of gate-source threshold voltage; typical values.



$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$ Typical R_{DSon} at:

(1) $I_D = 2$ A; $V_{GS} = 10$ V.
(2) $I_D = 1$ A; $V_{GS} = 4.5$ V.

Fig.13 Temperature coefficient of drain-source on-resistance; typical values.

Dual N-channel enhancement mode MOS transistor

PHN205

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-state resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

Two N-channel enhancement mode MOS transistors in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

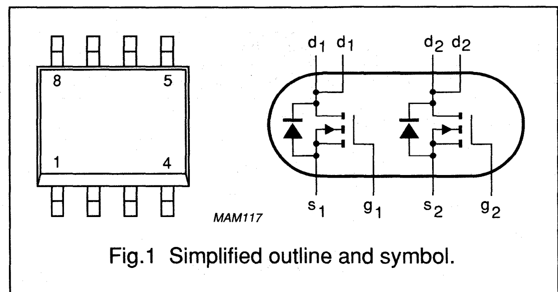


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per N-channel					
V_{DS}	drain-source voltage (DC)		–	30	V
V_{SD}	source-drain diode forward voltage	I_S = 1.25 A	–	1	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}	1	2.8	V
I_D	drain current (DC)	T_s = 80 °C	–	6.4	A
R_{DSon}	drain-source on-state resistance	I_D = 3.2 A; V_{GS} = 10 V	–	50	mΩ
P_{tot}	total power dissipation	T_s = 80 °C	–	3.5	W

PRELIMINARY
See Philips Semiconductors for Design-in information

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per N-channel					
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	6.4	A
I_{DM}	peak drain current	note 2	–	25	A
P_{tot}	total power dissipation	T_s = 80 °C; note 3	–	3.5	W
		T_{amb} = 25 °C; note 4	–	2.6	W
		T_{amb} = 25 °C; note 5	–	1.1	W
		T_{amb} = 25 °C; note 6	–	1.5	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–65	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	3.5	A
I_{SM}	peak pulsed source current	note 2	–	14	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 3.5 W at the same time.
4. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
5. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.
6. Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	20	K/W

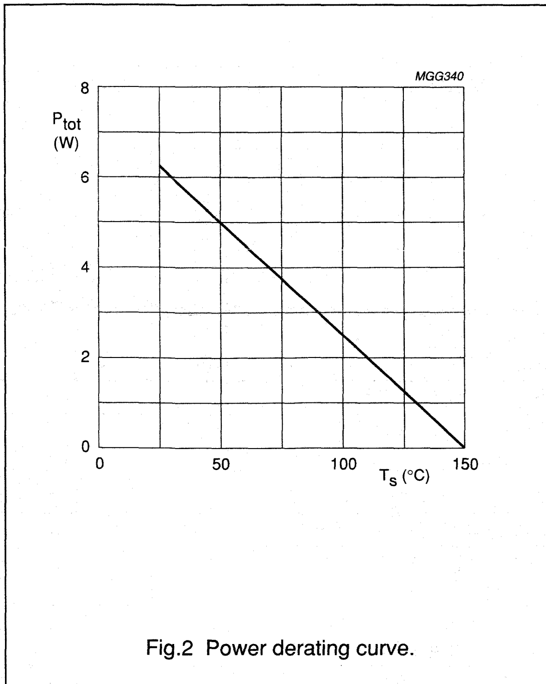
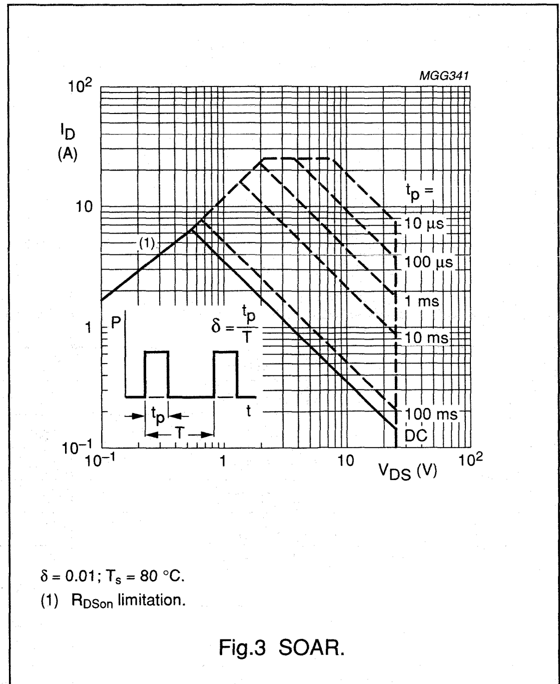


Fig.2 Power derating curve.



δ = 0.01; T_s = 80 °C.

(1) R_{DSon} limitation.

Fig.3 SOAR.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per N-channel						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 1.6 A	–	–	0.1	Ω
		V_{GS} = 10 V; I_D = 3.2 A	–	–	0.05	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	450	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	200	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	100	–	pF
Q_G	total gate charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 3.2 A	–	15	–	nC
Q_{GS}	gate-source charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 3.2 A	–	1	–	nC
Q_{GD}	gate-drain charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 3.2 A	–	5	–	nC
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω; see Fig.4	–	7	–	ns
t_f	fall time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω; see Fig.4	–	8	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω; see Fig.4	–	15	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω; see Fig.4	–	20	–	ns
t_r	rise time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω; see Fig.4	–	12	–	ns
t_{off}	turn-off switching time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω; see Fig.4	–	32	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 1.25 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 1.25 A; di/dt = −100 A/μs	–	45	–	ns

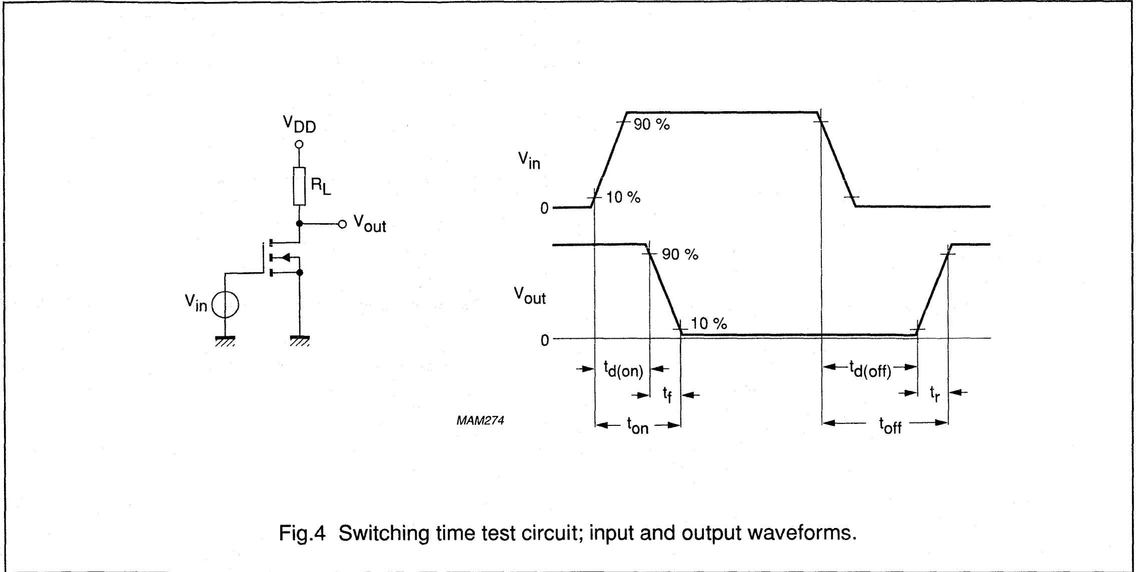


Fig.4 Switching time test circuit; input and output waveforms.

MGG342

$R_{th\ js}$ (K/W)

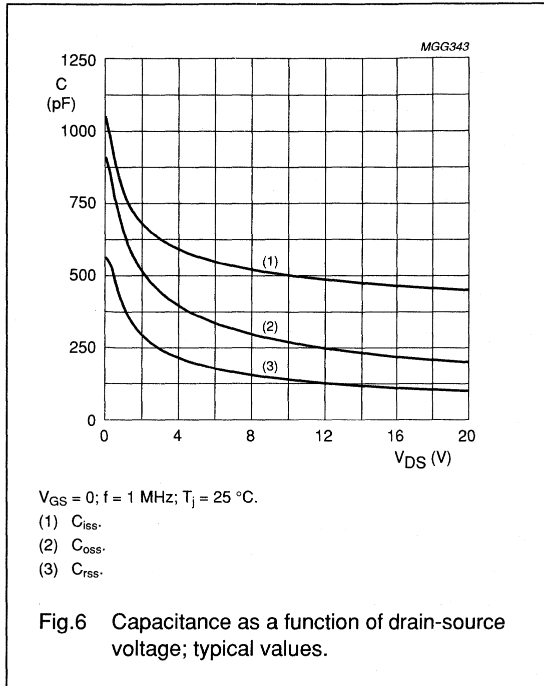
t_p (s)

$\delta = \frac{t_p}{T}$

(1) $\delta = 0.75$. (2) $\delta = 0.5$. (3) $\delta = 0.33$. (4) $\delta = 0.2$.

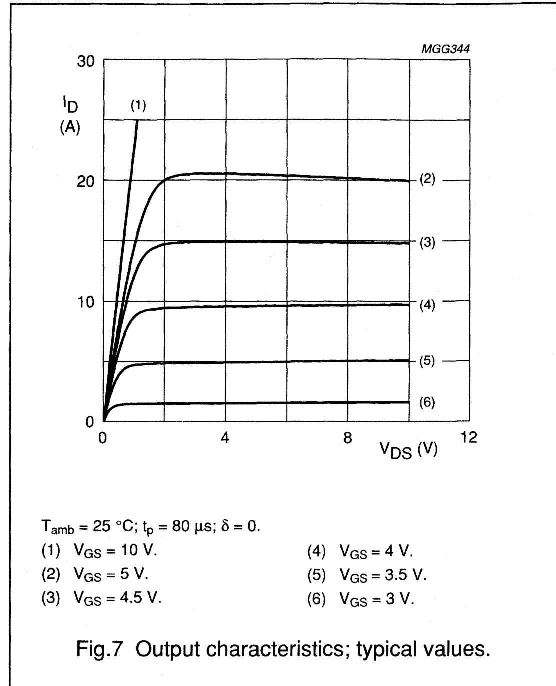
(5) $\delta = 0.1$. (6) $\delta = 0.05$. (7) $\delta = 0.02$. (8) $\delta = 0.01$. (9) $\delta = 0$.

Fig.5 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.



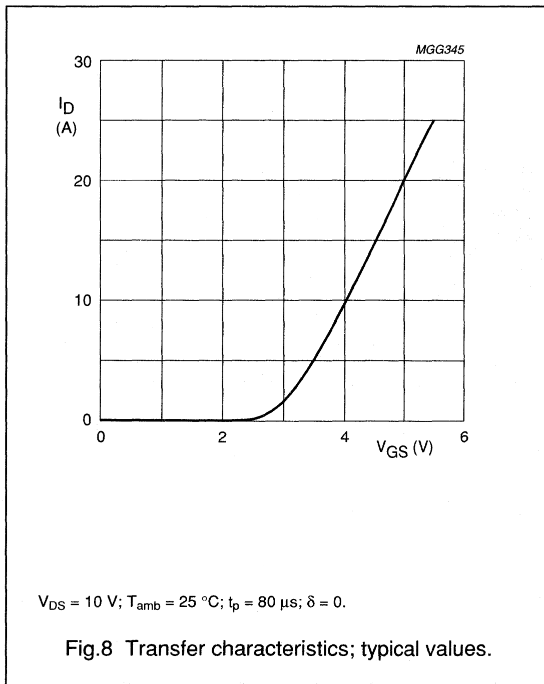
V_{GS} = 0; f = 1 MHz; T_j = 25 °C.
(1) C_{iss}.
(2) C_{oss}.
(3) C_{rss}.

Fig.6 Capacitance as a function of drain-source voltage; typical values.



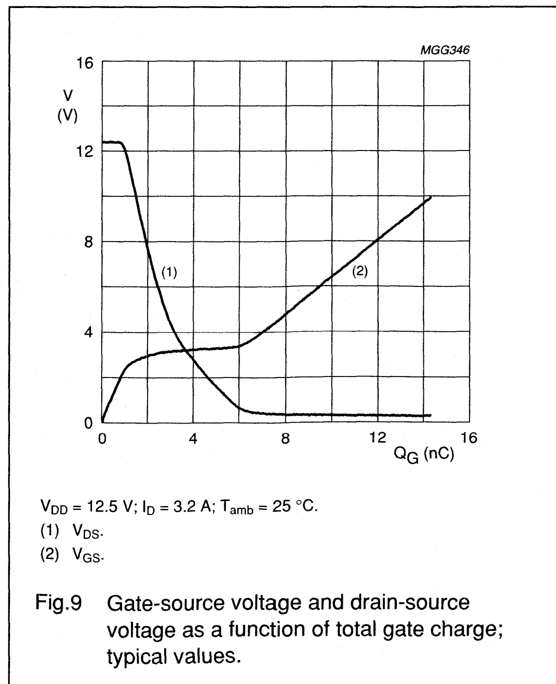
T_{amb} = 25 °C; t_p = 80 µs; δ = 0.
(1) V_{GS} = 10 V.
(2) V_{GS} = 5 V.
(3) V_{GS} = 4.5 V.
(4) V_{GS} = 4 V.
(5) V_{GS} = 3.5 V.
(6) V_{GS} = 3 V.

Fig.7 Output characteristics; typical values.



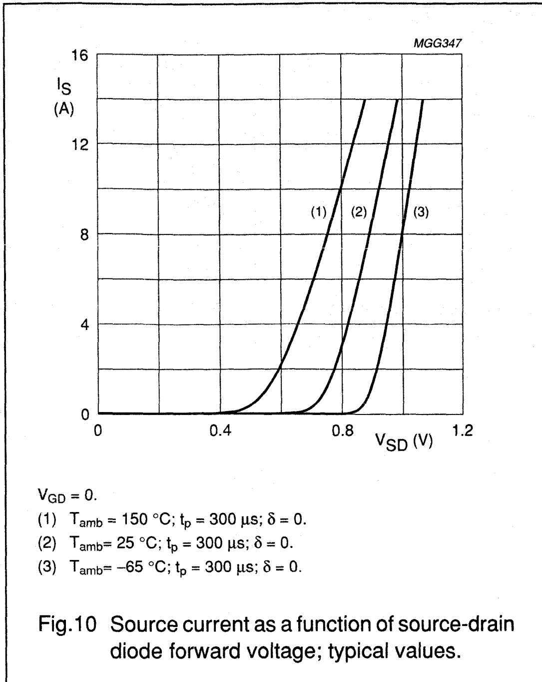
V_{DS} = 10 V; T_{amb} = 25 °C; t_p = 80 µs; δ = 0.

Fig.8 Transfer characteristics; typical values.



V_{DD} = 12.5 V; I_D = 3.2 A; T_{amb} = 25 °C.
(1) V_{DS}.
(2) V_{GS}.

Fig.9 Gate-source voltage and drain-source voltage as a function of total gate charge; typical values.



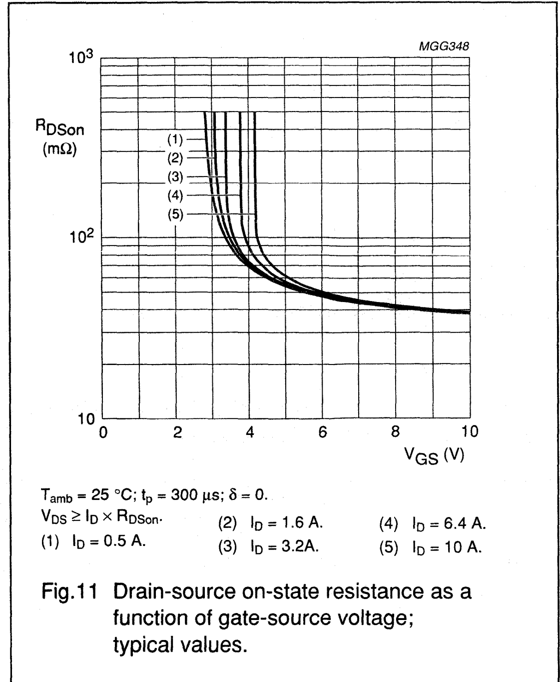
$V_{GD} = 0$.

(1) $T_{amb} = 150$ °C; $t_p = 300$ µs; $\delta = 0$.

(2) $T_{amb} = 25$ °C; $t_p = 300$ µs; $\delta = 0$.

(3) $T_{amb} = -65$ °C; $t_p = 300$ µs; $\delta = 0$.

Fig.10 Source current as a function of source-drain diode forward voltage; typical values.



$T_{amb} = 25$ °C; $t_p = 300$ µs; $\delta = 0$.

$V_{DS} \geq I_D \times R_{DSon}$.

(1) $I_D = 0.5$ A.

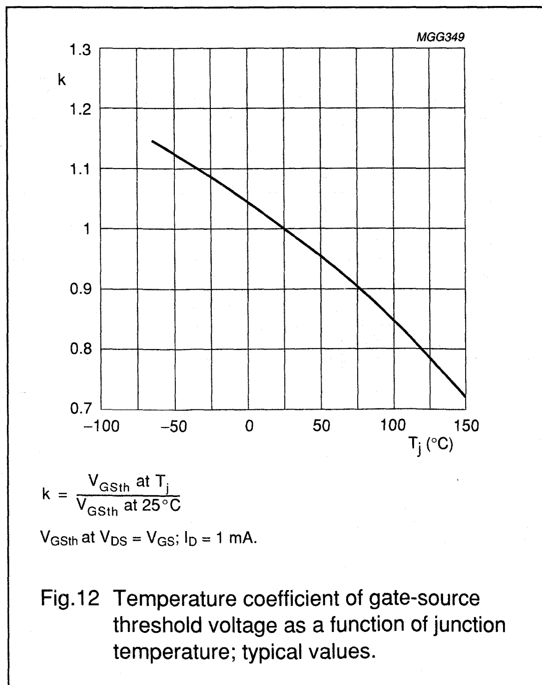
(2) $I_D = 1.6$ A.

(3) $I_D = 3.2$A.

(4) $I_D = 6.4$ A.

(5) $I_D = 10$ A.

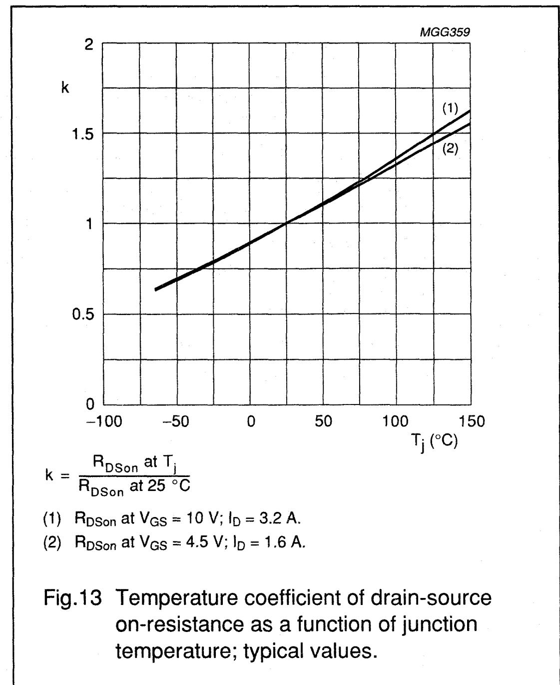
Fig.11 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25\,°\text{C}}$$

V_{GSth} at $V_{DS} = V_{GS}$; $I_D = 1$ mA.

Fig.12 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\,°\text{C}}$$

(1) R_{DSon} at $V_{GS} = 10$ V; $I_D = 3.2$ A.

(2) R_{DSon} at $V_{GS} = 4.5$ V; $I_D = 1.6$ A.

Fig.13 Temperature coefficient of drain-source on-resistance as a function of junction temperature; typical values.

Dual N-channel enhancement mode MOS transistor

PHN210

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

Two N-channel enhancement mode MOS transistors in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

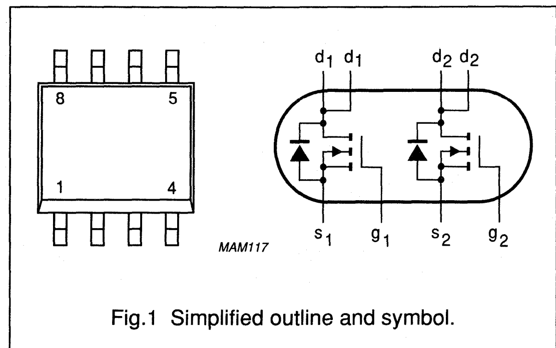


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per N-channel					
V_{DS}	drain-source voltage (DC)		–	30	V
V_{SD}	source-drain diode forward voltage	$I_S = 1.25$ A	–	1.2	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	$I_D = 1$ mA; $V_{DS} = V_{GS}$	1	2.8	V
I_D	drain current (DC)		–	3.5	A
R_{DSon}	drain-source on-state resistance	$I_D = 2.2$ A; $V_{GS} = 10$ V	–	0.1	Ω
P_{tot}	total power dissipation	$T_s = 80$ °C	–	2	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per N-channel					
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)	$T_s \leq 80°$ C	–	3.5	A
I_{DM}	peak drain current	note 1	–	14	A
P_{tot}	total power dissipation	T_s = 80 °C; note 2	–	2	W
		T_{amb} = 25 °C; note 3	–	2	W
		T_{amb} = 25 °C; note 4	–	1	W
		T_{amb} = 25 °C; note 5	–	1.3	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C
Source-drain diode					
I_S	source current (DC)	$T_s \leq 80$ °C	–	1.5	A
I_{SM}	peak pulsed source current	note 1	–	6	A

Notes

1. Pulse width and duty cycle limited by maximum junction temperature.
2. Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 2 W at the same time.
3. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.
5. Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

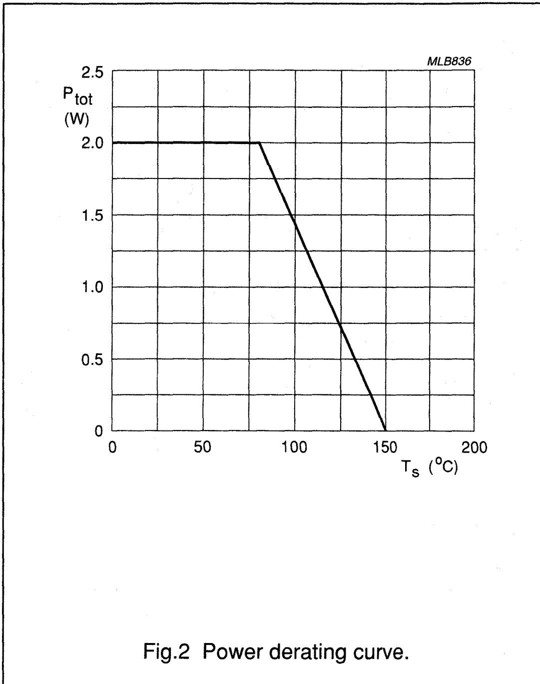
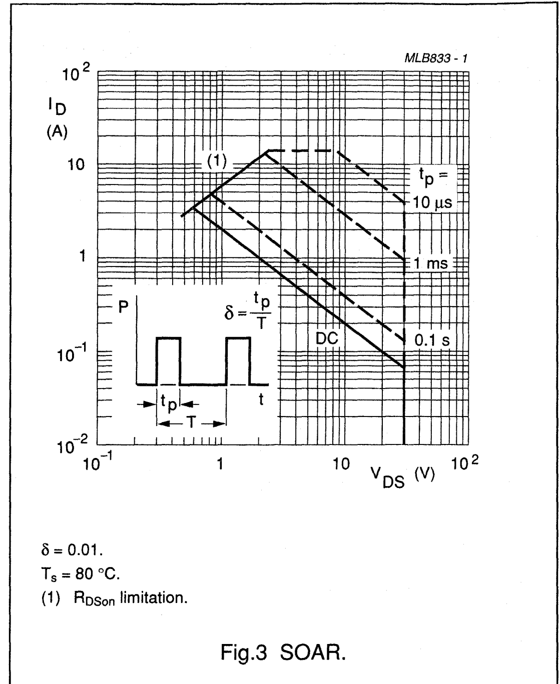


Fig.2 Power derating curve.



$\delta = 0.01$.

$T_s = 80$ °C.

(1) R_{DSon} limitation.

Fig.3 SOAR.

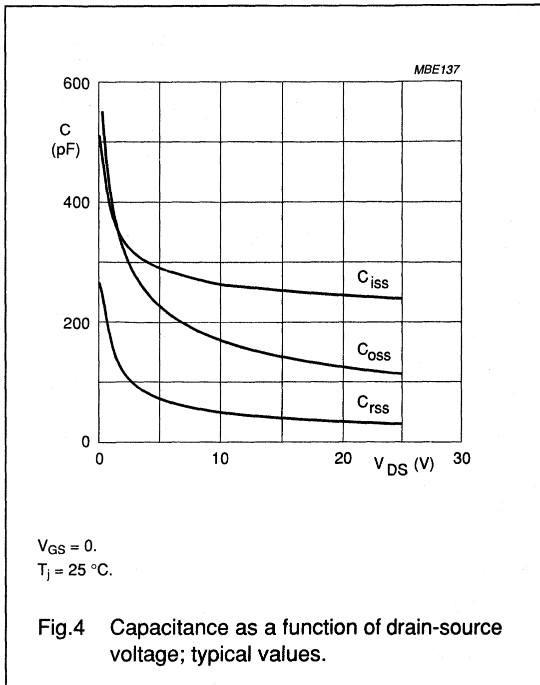
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-s}$	thermal resistance from junction to soldering point	35	K/W

CHARACTERISTICS

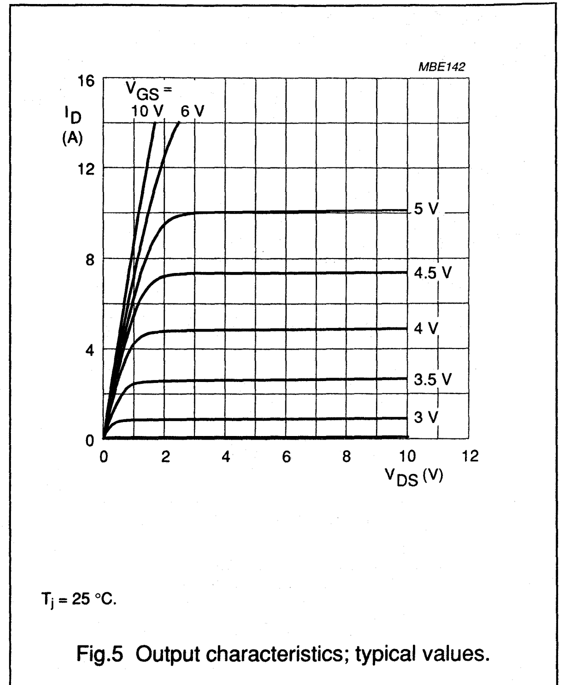
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per N-channel						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
I_{Don}	on-state drain current	V_{GS} = 10 V; V_{DS} = 1 V	3.5	–	–	A
		V_{GS} = 4.5 V; V_{DS} = 5 V	2	–	–	A
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 1 A	–	0.11	0.2	Ω
		V_{GS} = 10 V; I_D = 2.2 A	–	0.08	0.1	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = 20 V; I_D = 2.2 A	2	4.5	–	S
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	250	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	140	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 20 V; f = 1 MHz	–	50	–	pF
Q_G	total gate charge	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	10	30	nC
Q_{GS}	gate-source charge	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	1	–	nC
Q_{GD}	gate-drain charge	V_{GS} = 10 V; V_{DS} = 15 V; I_D = 2.3 A	–	2.5	–	nC
Switching times						
t_{on}	turn-on time	V_{GS} = 0 to 10 V; V_{DD} = 20 V; I_D = 1 A; R_L = 20 Ω	–	15	40	ns
t_{off}	turn-off time	V_{GS} = 10 to 0 V; V_{DD} = 20 V; I_D = 1 A; R_L = 20 Ω	–	25	140	ns
Source-drain diode						
V_{SD}	source drain diode forward voltage	V_{GD} = 0; I_S = 1.25 A	–	–	1.2	V
t_{rr}	reverse recovery time	I_S = 1.25 A; di/dt = 100 A/μs	–	35	100	ns



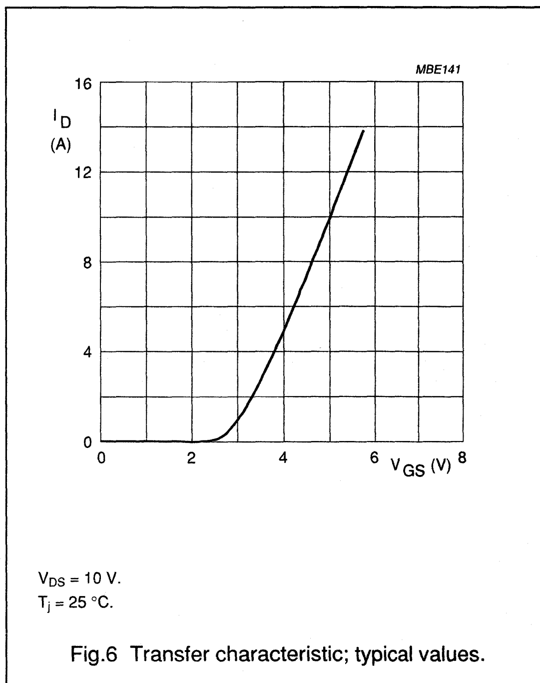
V_{GS} = 0.
T_j = 25 °C.

Fig.4 Capacitance as a function of drain-source voltage; typical values.



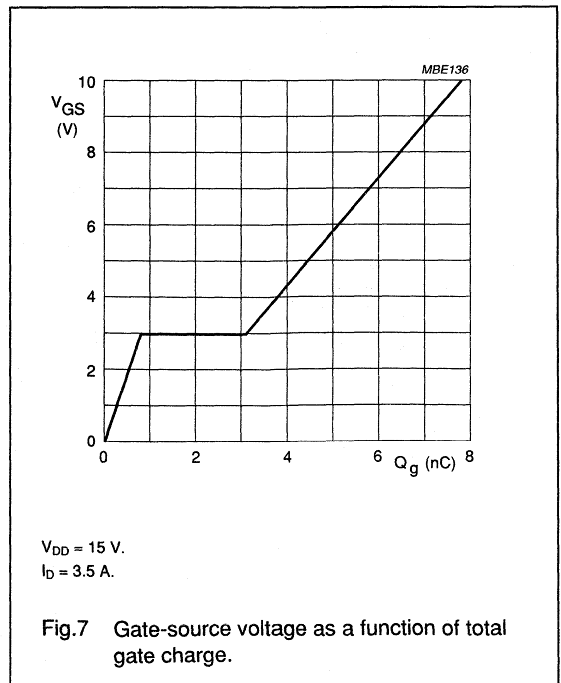
T_j = 25 °C.

Fig.5 Output characteristics; typical values.



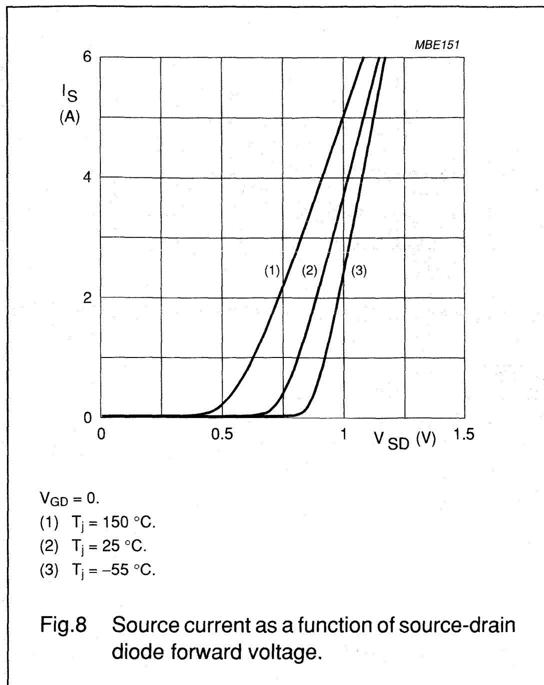
V_{DS} = 10 V.
T_j = 25 °C.

Fig.6 Transfer characteristic; typical values.



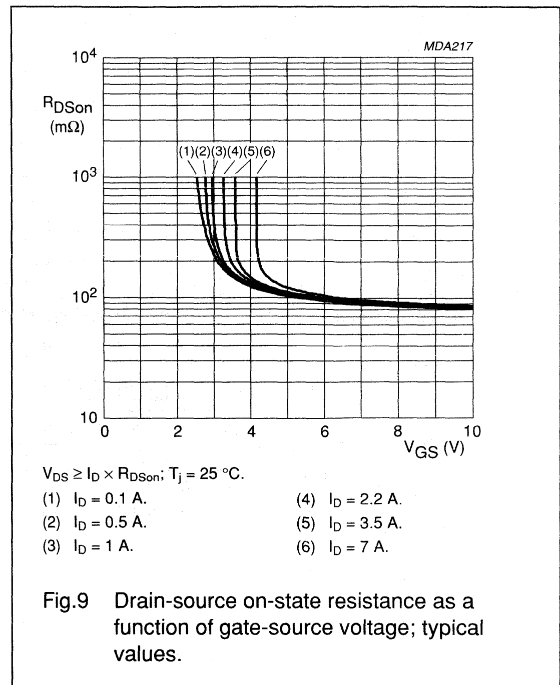
V_{DD} = 15 V.
I_D = 3.5 A.

Fig.7 Gate-source voltage as a function of total gate charge.



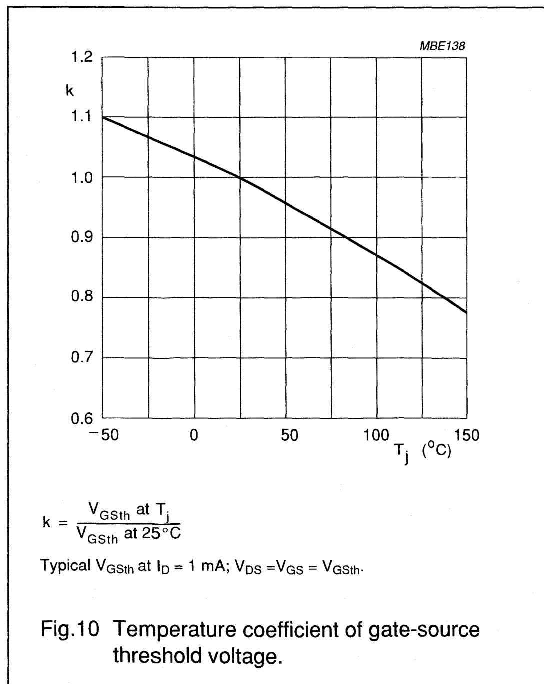
$V_{GD} = 0$.
(1) $T_j = 150$ °C.
(2) $T_j = 25$ °C.
(3) $T_j = -55$ °C.

Fig.8 Source current as a function of source-drain diode forward voltage.



$V_{DS} \geq I_D \times R_{DSon}$; $T_j = 25$ °C.
(1) $I_D = 0.1$ A.
(2) $I_D = 0.5$ A.
(3) $I_D = 1$ A.
(4) $I_D = 2.2$ A.
(5) $I_D = 3.5$ A.
(6) $I_D = 7$ A.

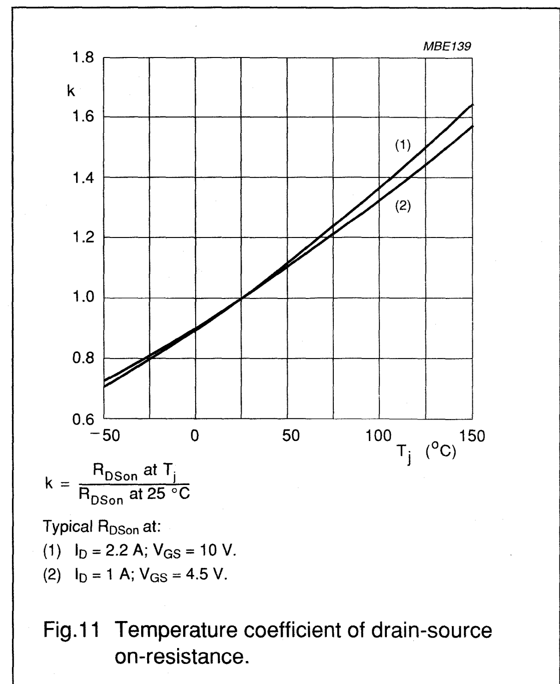
Fig.9 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25\,°C}$$

Typical V_{GSth} at $I_D = 1$ mA; $V_{DS} = V_{GS} = V_{GSth}$.

Fig.10 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\,°C}$$

Typical R_{DSon} at:
(1) $I_D = 2.2$ A; $V_{GS} = 10$ V.
(2) $I_D = 1$ A; $V_{GS} = 4.5$ V.

Fig.11 Temperature coefficient of drain-source on-resistance.

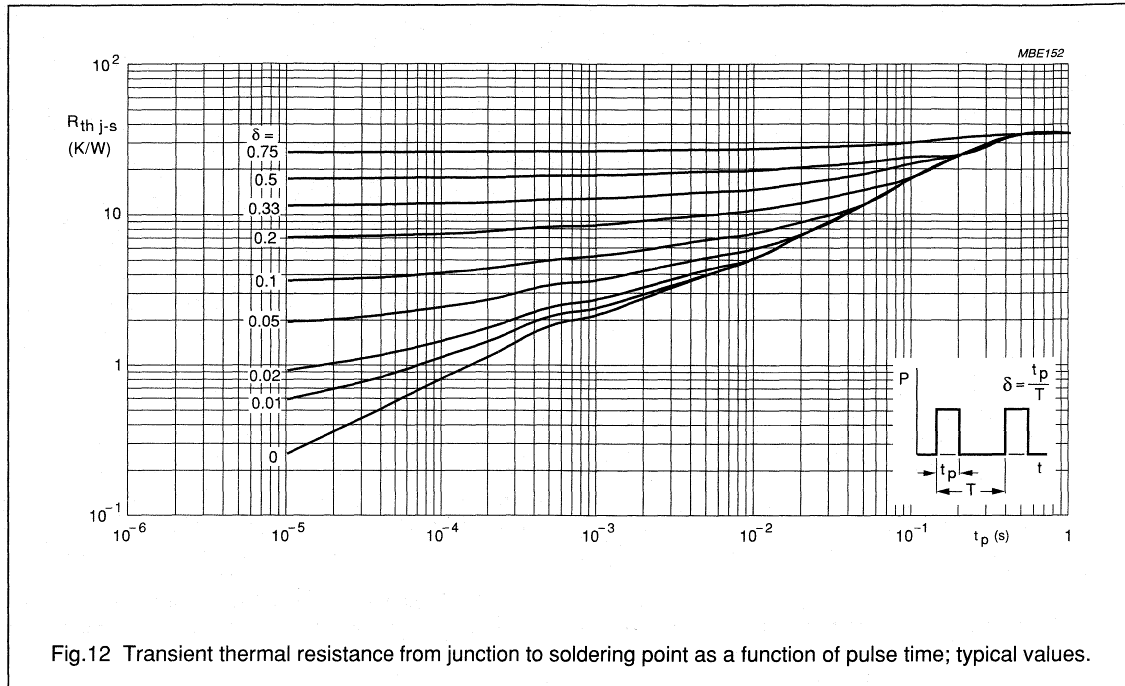


Fig.12 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

4 N-channel 50 mΩ FET array enhancement mode MOS transistors

PHN405

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-state resistance
- Current monitoring.

APPLICATIONS

- Motor and actuator driver, power management, synchronized rectification.

DESCRIPTION

Four enhancement mode MOS transistors in a 16-pin plastic SOT338-1 (SSOP16) package. Two transistors feature current monitoring (sense FETs).

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT338-1 (SSOP16)

PIN	SYMBOL	DESCRIPTION
1 and 4	d_1	drain 1
2	s_1	source 1
3	g_1	gate 1
5 and 8	d_2	drain 2
6	s_2	source 2
7	g_2	gate 2
9	g_3	gate 3
10	s_3	source 3
11 and 15	d_3	drain 3
12	m_3	current monitor 3
13	g_4	gate 4
14	s_4	source 4
16	m_4	current monitor 4

PRELIMINARY
See Philips Semiconductors for Design-in Information

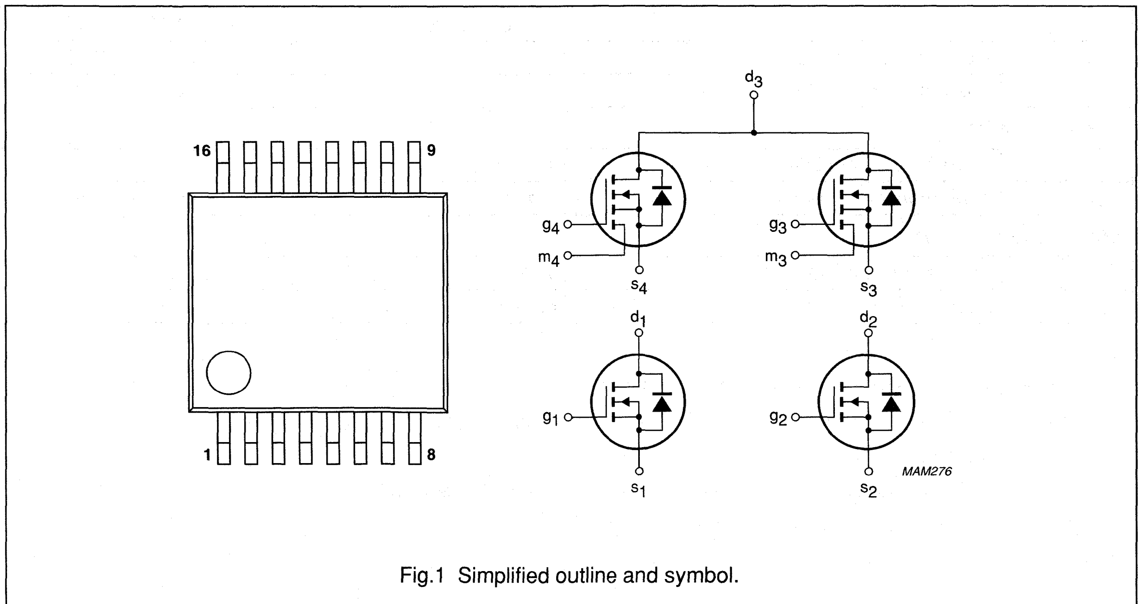


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; $V_{DS} = V_{GS}$	1	2.8	V
I_D	drain current (DC)	T_s = 80 °C	–	4	A
R_{DSon}	drain-source on-state resistance	I_D = 2 A; V_{GS} = 10 V	–	0.05	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	1.4	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per FET					
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	4	A
I_{DM}	peak drain current	note 2	–	16	A
P_{tot}	total power dissipation	T_s = 80 °C; note 3	–	1.4	W
		T_s = 80 °C; note 4	–	1.25	W
		T_s = 80 °C; note 5	–	1.09	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Current monitor					
I_M	monitor current (DC)	T_s = 80 °C	–	0.05	A
I_{MM}	peak monitor current	note 2	–	0.2	A
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	1.7	A
I_{SM}	peak source current	note 2	–	6.8	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. When only one FET dissipates.
4. When either FETs 1 and 3 or 2 and 4 dissipate an equal amount of power.
5. When all four FETs dissipate an equal amount of power.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
Per FET				
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	note 1	50	K/W
		note 2	56	K/W
		note 3	64	K/W

Notes

1. When only one FET dissipates.
2. When either FETs 1 and 3 or 2 and 4 dissipate an equal amount of power.
3. When all four FETs dissipate an equal amount of power.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per FET						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 16 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 1 A	–	–	0.08	Ω
		V_{GS} = 10 V; I_D = 2 A	–	–	0.05	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	350	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	180	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	120	–	pF
Q_G	total gate charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 2 A; T_{amb} = 25 °C	–	14	20	nC
Q_{GS}	gate-source charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 2 A; T_{amb} = 25 °C	–	0.8	–	nC
Q_{GD}	gate-drain charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 2 A; T_{amb} = 25 °C	–	5.8	–	nC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω	–	7	–	ns
t_f	fall time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω	–	11	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω	–	18	30	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω	–	17	–	ns
t_r	rise time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω	–	11	–	ns
t_{off}	turn-off switching time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω	–	28	50	ns
Current monitor						
R_{DMon}	on-state drain-monitor resistance	V_{GM} = 10 V; I_D = 25 mA; I_S = 0	–	–	4	Ω
		V_{GM} = 4.5 V; I_D = 12 mA; I_S = 0	–	–	6.4	Ω
I_D/I_M	drain to monitor current ratio	I_D = 2 A; V_{GS} = 10 V; V_{MS} = 0	–	80	–	
C_{Moss}	output capacitance of monitor cells	V_{GM} = V_{MS} = 0; V_{DS} = 24 V; f = 1 MHz	–	2.3	–	pF
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 1.25 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 1.25 A; di/dt = −100 A/μs	–	80	–	ns

7 N-channel 80 mΩ FET array enhancement mode MOS transistors

PHN708

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-state resistance.

APPLICATIONS

- Driving high performance three phase brushless DC motors.

DESCRIPTION

Seven enhancement mode MOS transistors in a 24-pin plastic SOT340-1 (SSOP24) package. Six of the transistors are in three half-bridge configurations.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT340-1 (SSOP24)

PIN	SYMBOL	DESCRIPTION
1 and 4	d_1	drain 1
2	s_1	source 1
3	g_1	gate 1
5 and 8	d_2	drain 2
6	s_2	source 2
7	g_2	gate 2
9,12	d_3	drain 3
10	s_3	source 3
11	g_3	gate 3
13	g_4	gate 4
14	s_4	source 4
15, 17, 18, 20, 21, 23, 24	d_4	drain 4
16	g_5	gate 5
19	g_6	gate 6
22	g_7	gate 7

PRELIMINARY
See Philips Semiconductors for Design-in information

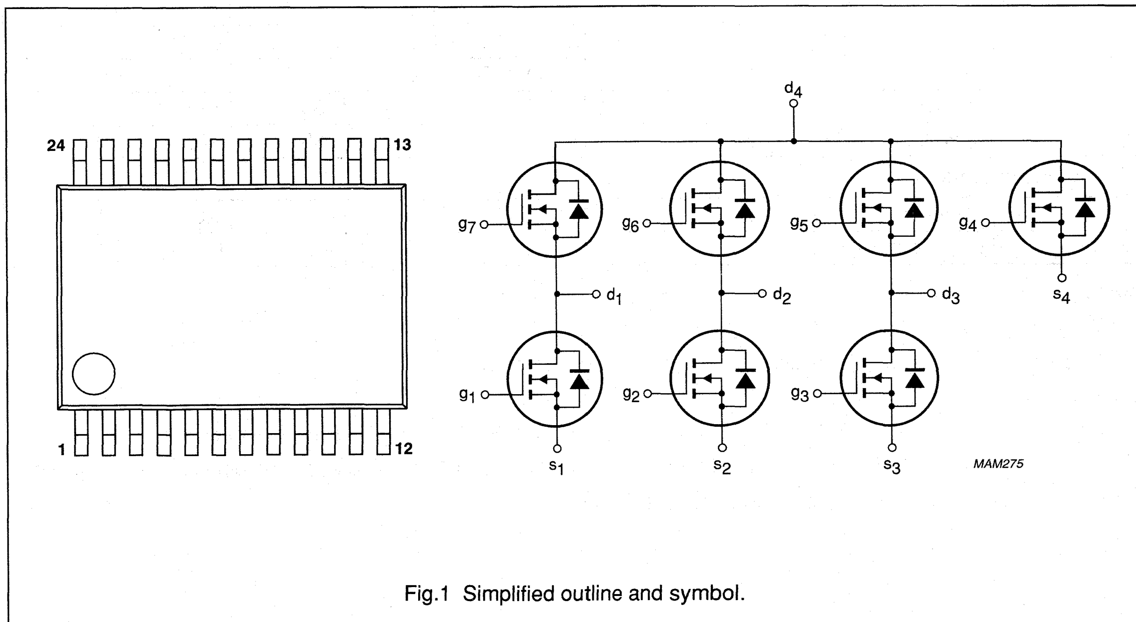


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}	1	2.8	V
I_D	drain current (DC)	T_s = 80 °C	–	3.1	A
R_{DSon}	drain-source on-state resistance	I_D = 1.5 A; V_{GS} = 10 V	–	0.08	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	1.3	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per FET					
V_{DS}	drain-source voltage (DC)		–	30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	3.1	A
I_{DM}	peak drain current	note 2	–	12.4	A
P_{tot}	total power dissipation	T_s = 80 °C; note 3	–	1.3	W
		T_s = 80 °C; note 4	–	1.13	W
		T_s = 80 °C; note 5	–	0.92	W
		T_s = 80 °C; note 6	–	0.77	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	1.6	A
I_{SM}	peak source current	note 2	–	6.4	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. When only one FET dissipates.
4. When either combination of FETs 1-5, 1-6, 2-5, 2-7, 3-6 or 3-7 dissipate an equal amount of power.
5. When FET four plus either combination of FETs 1-5, 1-6, 2-5, 2-7, 3-6 or 3-7 dissipate an equal amount of power.
6. When all seven FETs dissipate an equal amount of power.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
Per FET				
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	note 1	53	K/W
		note 2	62	K/W
		note 3	76	K/W
		note 4	91	K/W

Notes

1. When only one FET dissipates.
2. When either combination of FETs 1-5, 1-6, 2-5, 2-7, 3-6 or 3-7 dissipate an equal amount of power.
3. When FET four plus either combination of FETs 1-5, 1-6, 2-5, 2-7, 3-6 or 3-7 dissipate an equal amount of power.
4. When all seven FETs dissipate an equal amount of power.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per FET						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 10 μA	30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = 1 mA	1	–	2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 24 V	–	–	100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 0.75 A	–	–	0.13	Ω
		V_{GS} = 10 V; I_D = 1.5 A	–	–	0.08	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	250	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	125	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 24 V; f = 1 MHz	–	75	–	pF
Q_G	total gate charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 1.5 A; T_{amb} = 25 °C	–	10	15	nC
Q_{GS}	gate-source charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 1.5 A; T_{amb} = 25 °C	–	0.6	–	nC
Q_{GD}	gate-drain charge	V_{GS} = 10 V; V_{DD} = 15 V; I_D = 1.5 A; T_{amb} = 25 °C	–	3.8	–	nC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω	–	6	–	ns
t_f	fall time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω	–	9	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to 10 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω	–	15	30	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω	–	15	–	ns
t_r	rise time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω	–	7	–	ns
t_{off}	turn-off switching time	V_{GS} = 10 to 0 V; V_{DD} = 15 V; I_D = 1 A; R_{gen} = 6 Ω	–	22	45	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = 1.25 A	–	–	1	V
t_{rr}	reverse recovery time	I_S = 1.25 A; di/dt = −100 A/μs	–	60	–	ns

N-channel enhancement mode MOS transistor

PHN1013

FEATURES

- Very low on-state resistance.

APPLICATIONS

- DC to DC converters
- General purpose switching applications.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s	source
2	s	source
3	s	source
4	g	gate
5	d	drain
6	d	drain
7	d	drain
8	d	drain

DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor using 'trench' technology, in an 8-pin plastic SOT96-1 (SO8) package.

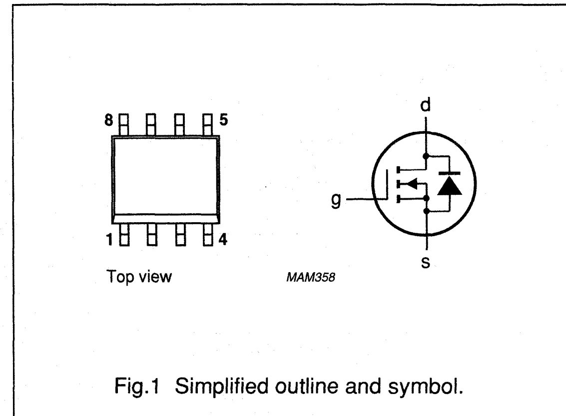


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		30	V
I_D	drain current (DC)		10	A
P_{tot}	total power dissipation		2.5	W
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V	13.5	mΩ
T_j	junction temperature		150	°C

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	30	V
V_{DG}	drain-gate voltage	R_{GS} = 20 kΩ	–	30	V
V_{GS}	gate-source voltage		–	±20	V
I_D	drain current (DC)	T_{amb} = 25 °C; $t_p \leq$ 10 s	–	10	A
		T_{amb} = 70 °C; $t_p \leq$ 10 s	–	8	A
I_{DM}	peak drain current	T_{amb} = 25 °C	–	50	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	–	2.5	W
		T_{amb} = 70 °C	–	1.6	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C

See Philips Semiconductors for Design-in information OBJECTIVE

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	minimum footprint; $t_p \leq 10$ s; note 1	50	K/W

Note

1. Device mounted on an FR4 printed-circuit board.

STATIC CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = 250$ μA	30	–	–	V
		$V_{GS} = 0$; $I_D = 250$ μA; $T_j = -55$ °C	27	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = V_{GS}$; $I_D = 250$ μA	2.1	3	4	V
		$V_{DS} = V_{GS}$; $I_D = 250$ μA; $T_j = 150$ °C	1.4	–	–	V
		$V_{DS} = V_{GS}$; $I_D = 250$ μA; $T_j = -55$ °C	–	–	4.4	V
I_{DSS}	drain-source leakage current	$V_{DS} = 30$ V; $V_{GS} = 0$	–	0.05	10	μA
		$V_{DS} = 30$ V; $V_{GS} = 0$; $T_j = 150$ °C	–	–	500	μA
I_{GSS}	gate leakage current	$V_{GS} = \pm 10$ V; $V_{DS} = 0$	–	10	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 10$ A	–	11	13.5	mΩ
		$V_{GS} = 10$ V; $I_D = 10$ A; $T_j = 150$ °C	–	–	26	mΩ

DYNAMIC CHARACTERISTICS

$T_j = 25$ °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	forward transconductance	$V_{DS} = 25$ V; $I_D = 10$ A	4	8	–	S
C_{iss}	input capacitance	$V_{GS} = 0$; $V_{DS} = 25$ V; f = 1 MHz	–	1700	2200	pF
C_{oss}	output capacitance	$V_{GS} = 0$; $V_{DS} = 25$ V; f = 1 MHz	–	325	450	pF
C_{rss}	reverse transfer capacitance	$V_{GS} = 0$; $V_{DS} = 25$ V; f = 1 MHz	–	214	260	pF
Q_G	total gate charge	$V_{GS} = 5$ V; $V_{DD} = 24$ V; $I_D = 10$ A	–	27	–	nC
Q_{GS}	gate-source charge	$V_{GS} = 5$ V; $V_{DD} = 24$ V; $I_D = 10$ A	–	3.5	–	nC
Q_{GD}	gate-drain charge	$V_{GS} = 5$ V; $V_{DD} = 24$ V; $I_D = 10$ A	–	15	–	nC
Switching times						
$t_{d(on)}$	turn-on delay time	$V_{GS} = 5$ V; $V_{DD} = 25$ V; $I_D = 10$ A; $R_{gen} = 10$ Ω resistive load	–	25	40	ns
$t_{d(off)}$	turn-off delay time	$V_{GS} = 5$ V; $V_{DD} = 25$ V; $I_D = 10$ A; $R_{gen} = 10$ Ω resistive load	–	90	130	ns
t_r	rise time	$V_{GS} = 5$ V; $V_{DD} = 25$ V; $I_D = 10$ A; $R_{gen} = 10$ Ω resistive load	–	75	125	ns
t_f	fall time	$V_{GS} = 5$ V; $V_{DD} = 25$ V; $I_D = 10$ A; $R_{gen} = 10$ Ω resistive load	–	35	50	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
I_{DR}	continuous reverse drain current	T_{amb} = 25 °C; $t_p \leq$ 10 s	–	10	A
I_{DRM}	pulsed reverse drain current		–	50	A
V_{SD}	source-drain diode forward voltage	I_F = 10 A; V_{GS} = 0	0.95	1.2	V
		I_F = 50 A; V_{GS} = 0	1	–	V
t_{rr}	reverse recovery time	I_F = 10 A; di/dt = −100 A/µs; V_{GS} = −10 V; V_R = 25 V	50	–	ns
Q_{rr}	reverse recovery charge	I_F = 10 A; di/dt = −100 A/µs; V_{GS} = −10 V; V_R = 25 V	0.1	–	µC

P-channel enhancement mode MOS transistor

PHP109

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

P-channel enhancement mode MOS transistor in an 8-pin plastic SO8 (SOT96-1) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SO8 (SOT96-1)

PIN	SYMBOL	DESCRIPTION
1	n.c.	not connected
2	s	source
3	s	source
4	g	gate
5	d	drain
6	d	drain
7	d	drain
8	d	drain

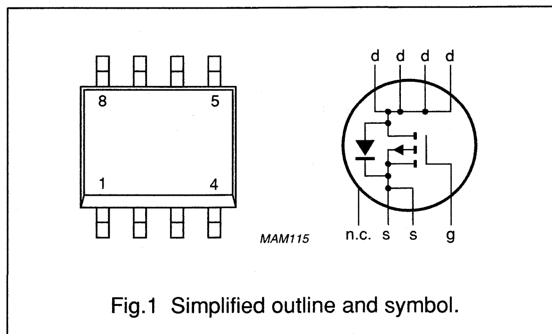


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	I_S = –1.25 A	–	–1.3	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = –1 mA; $V_{DS} = V_{GS}$	–1	–2.8	V
I_D	drain current (DC)	T_s = 80 °C	–	–5	A
R_{DSon}	drain-source on-state resistance	I_D = –2.5 A; V_{GS} = –10 V	–	0.09	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	4	W

P-channel enhancement mode MOS transistor

PHP109

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	–5	A
I_{DM}	peak drain current	note 2	–	–20	A
P_{tot}	total power dissipation	T_s = 80 °C	–	4	W
		T_{amb} = 25 °C; note 3	–	2.7	W
		T_{amb} = 25 °C; note 4	–	1.15	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–65	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	–3	A
I_{SM}	peak pulsed source current	note 2	–	–12	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Value based on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Value based on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

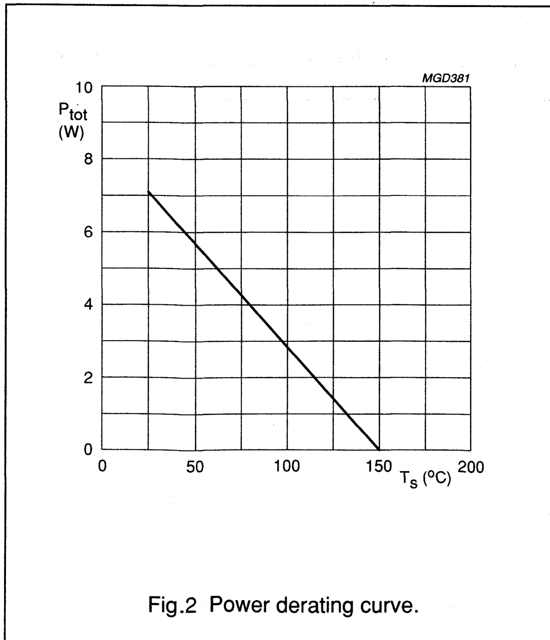
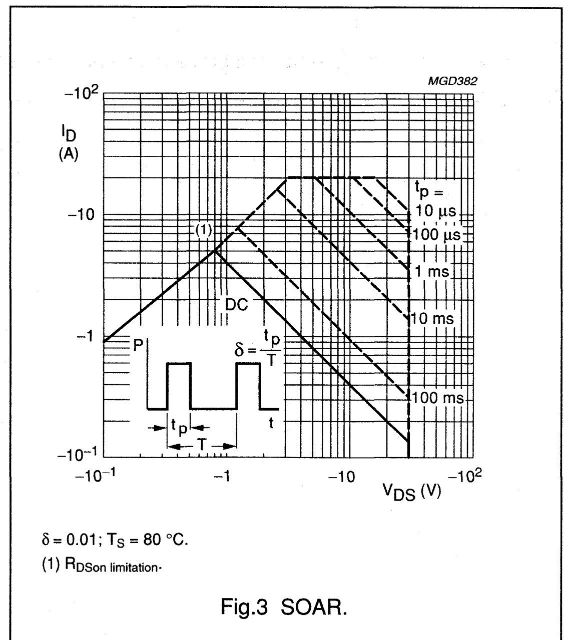


Fig.2 Power derating curve.



$\delta = 0.01$; $T_S = 80$ °C.

(1) R_{DSon} limitation.

Fig.3 SOAR.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	17.5	K/W

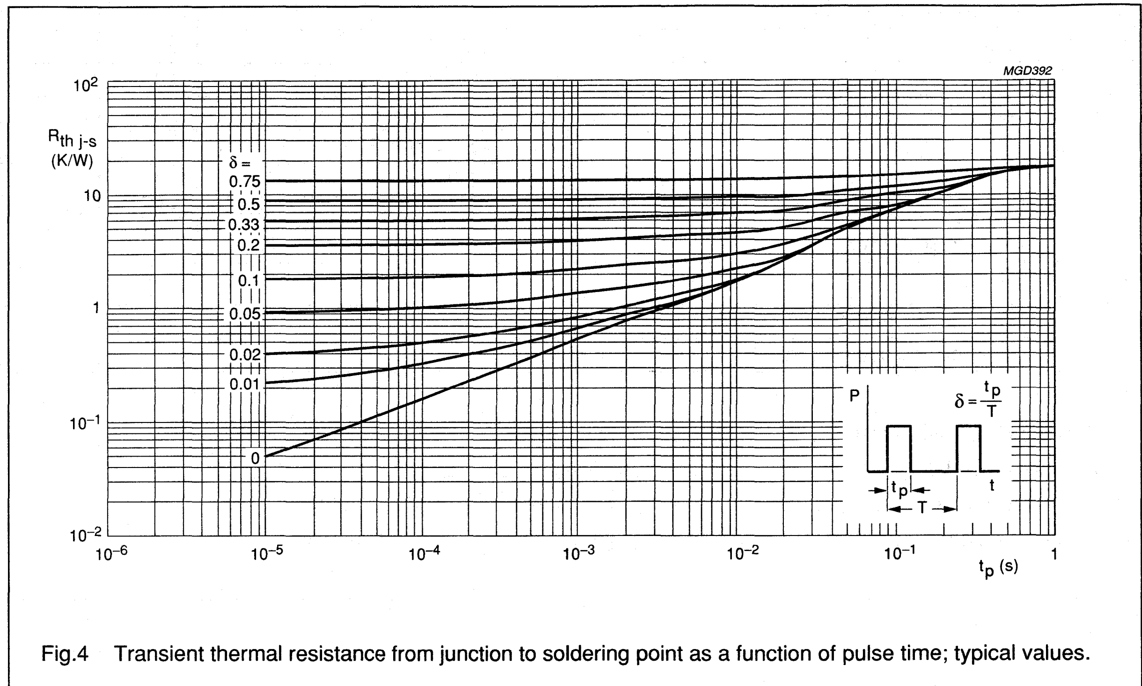
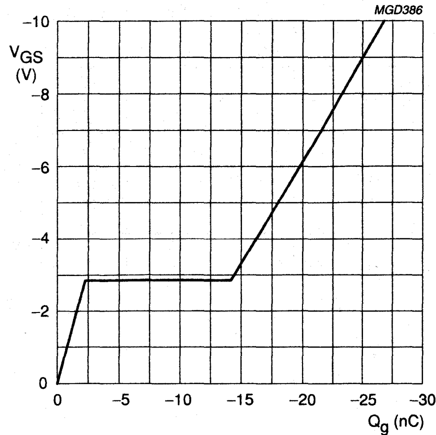


Fig.4 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

CHARACTERISTICS

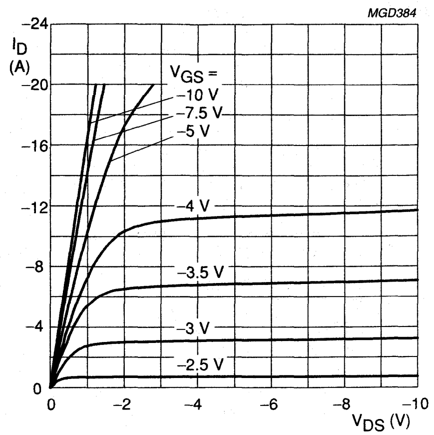
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−1	–	−2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −24 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −1.25 A	–	–	0.15	Ω
		V_{GS} = −10 V; I_D = −2.5 A	–	–	0.09	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	825	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	350	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	150	–	pF
Q_G	total gate charge	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −2.5 A	–	30	40	nC
Q_{GS}	gate-source charge	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −2.5 A	–	3	–	nC
Q_{GD}	gate-drain charge	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −2.5 A	–	12	–	nC
Switching times (see Fig.11)						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	7	–	ns
t_f	fall time		–	10	–	ns
t_{on}	turn-on switching time		–	17	35	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_L = 15 Ω; R_{gen} = 6 Ω	–	60	–	ns
t_r	rise time		–	40	–	ns
t_{off}	turn-off switching time		–	100	200	ns
Source-drain diode						
V_{SD}	source-drain forward voltage	V_{GD} = 0; I_S = −1.25 A	–	–	−1.3	V
t_{rr}	reverse recovery time	I_S = −1.25 A; di/dt = 100 A/μs	–	70	–	ns



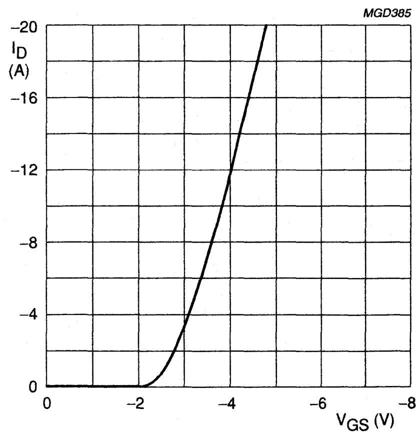
V_{DD} = −15 V: I_D = −2.5 A.

Fig.5 Gate-source voltage as a function of total gate charge; typical values.



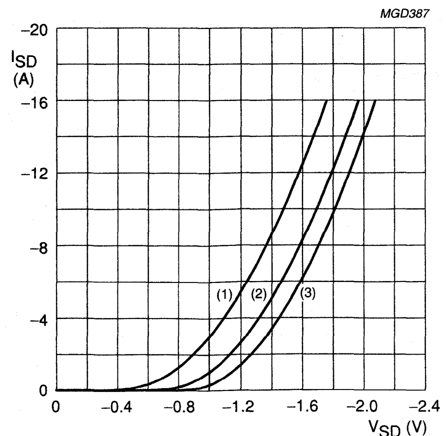
T_j = 25 °C.

Fig.6 Output characteristics; typical values.



V_{DS} = −10 V; T_j = 25 °C.

Fig.7 Transfer characteristics; typical values.



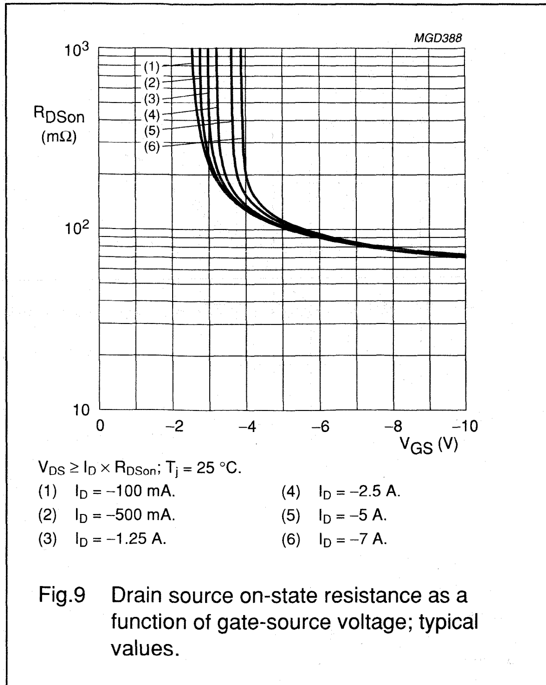
V_{GD} = 0.

(1) T_j = 150 °C.

(2) T_j = 25 °C.

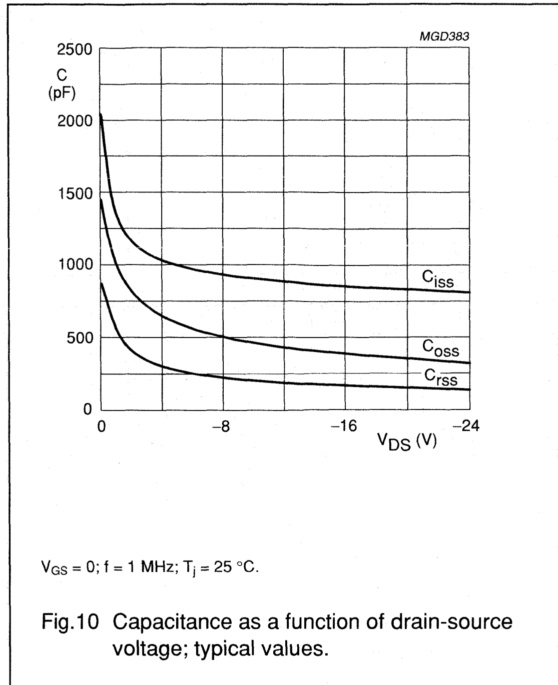
(3) T_j = −65 °C.

Fig.8 Source current as a function of source-drain diode forward voltage; typical values.



$V_{DS} \geq I_D \times R_{DSon}$; T_j = 25 °C.
(1) I_D = −100 mA.
(2) I_D = −500 mA.
(3) I_D = −1.25 A.
(4) I_D = −2.5 A.
(5) I_D = −5 A.
(6) I_D = −7 A.

Fig.9 Drain source on-state resistance as a function of gate-source voltage; typical values.



V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.10 Capacitance as a function of drain-source voltage; typical values.

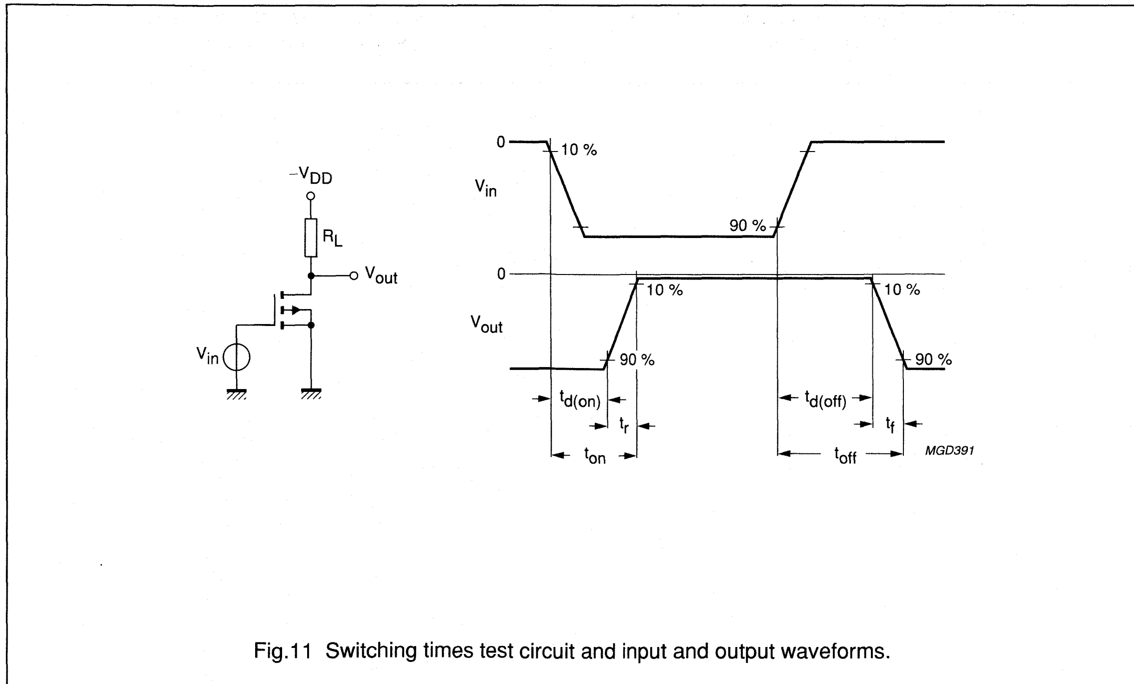
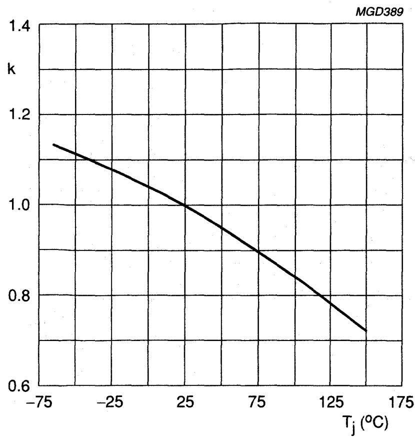


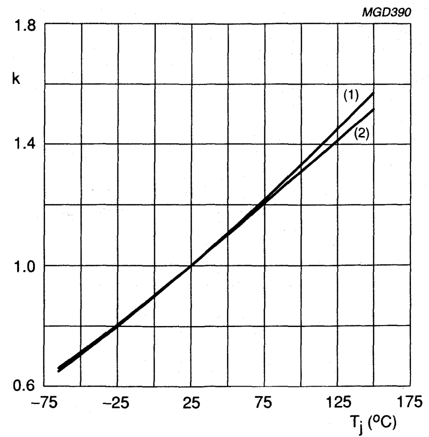
Fig.11 Switching times test circuit and input and output waveforms.



$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$

V_{GSth} at $V_{DS} = V_{GS}$; $I_D = -1$ mA.

Fig.12 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; typical values.



$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25 °C}$

R_{DSon} at:

(1) $V_{GS} = -10$ V; $I_D = -2.5$ A.

(2) $V_{GS} = -4.5$ V; $I_D = -1.25$ A.

Fig.13 Temperature coefficient of drain-source on-resistance as a function of junction temperature; typical values.

P-channel enhancement mode MOS transistor

PHP125

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

PINNING - SO8 (SOT96-1)

PIN	SYMBOL	DESCRIPTION
1	n.c.	not connected
2	s	source
3	s	source
4	g	gate
5	d	drain
6	d	drain
7	d	drain
8	d	drain

DESCRIPTION

P-channel enhancement mode MOS transistor in an 8-pin plastic SO8 (SOT96-1) package.

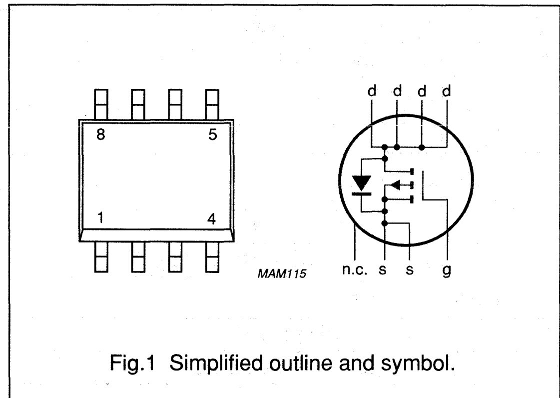


Fig.1 Simplified outline and symbol.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	$I_S = -1.25$ A	–	–1.6	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	$I_D = -1$ mA; $V_{DS} = V_{GS}$	–1	–2.8	V
I_D	drain current (DC)	$T_s = 80$ °C	–	–2.5	A
R_{DSon}	drain-source on-state resistance	$I_D = -1$ A; $V_{GS} = -10$ V	–	0.25	Ω
P_{tot}	total power dissipation	$T_s = 80$ °C	–	2.8	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	–2.5	A
I_{DM}	peak drain current	note 2	–	–10	A
P_{tot}	total power dissipation	T_s = 80 °C	–	2.8	W
		T_{amb} = 25 °C; note 3	–	2.4	W
		T_{amb} = 25 °C; note 4	–	1.1	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–65	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	–2	A
I_{SM}	peak pulsed source current	note 2	–	–8	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Value based on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Value based on a printed-circuit board with a $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

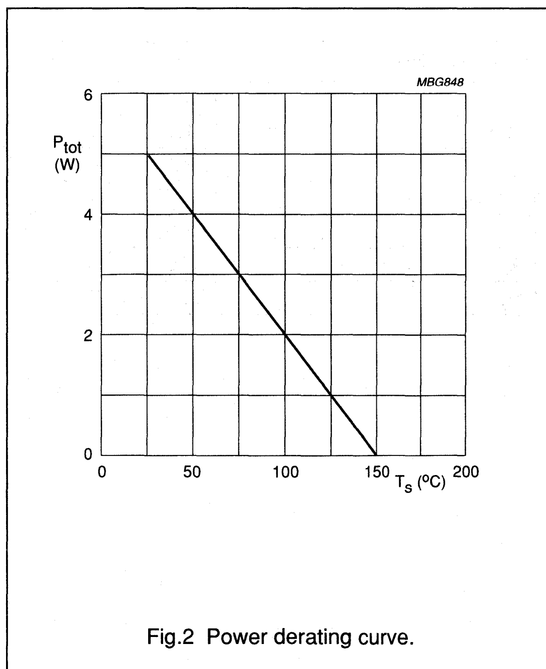
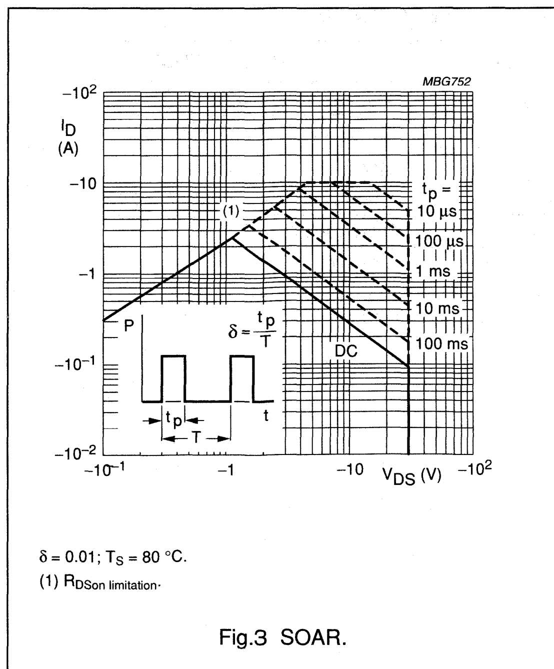


Fig.2 Power derating curve.



δ = 0.01; T_S = 80 °C.

(1) R_{DSon} limitation.

Fig.3 SOAR.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	25	K/W

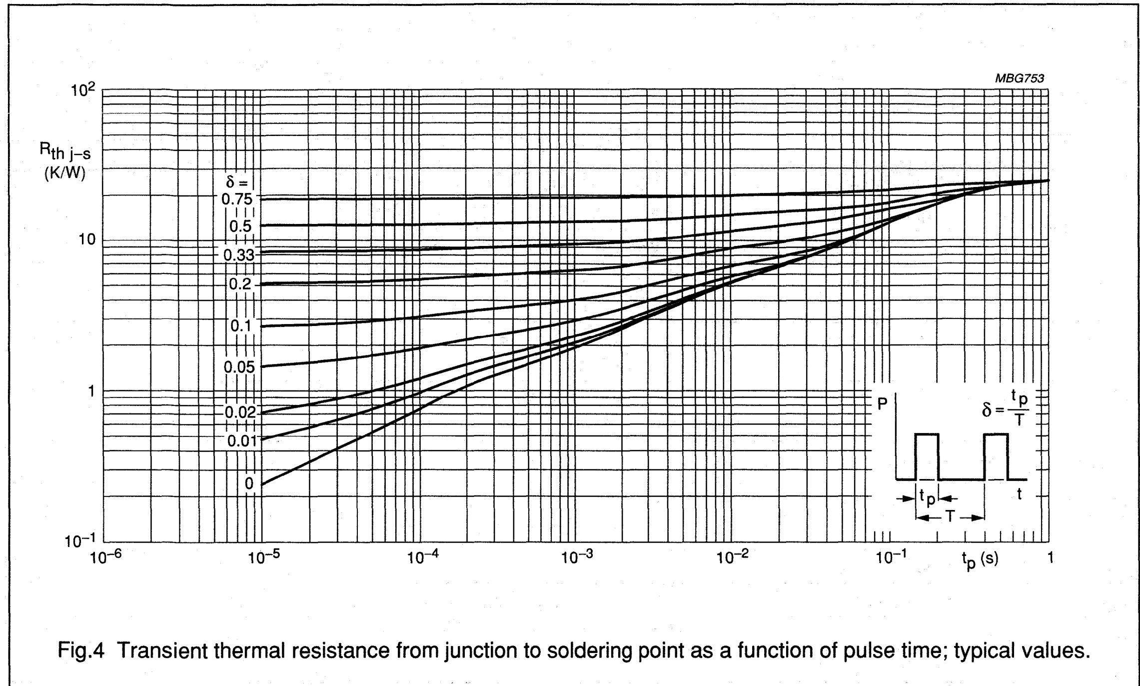
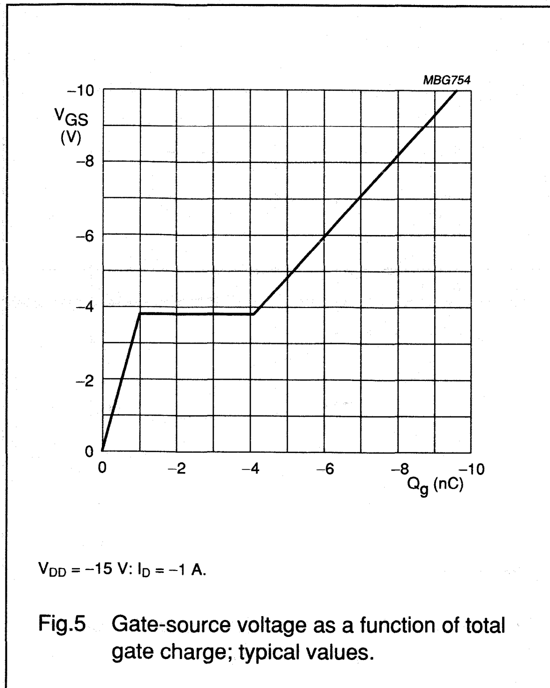


Fig.4 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

CHARACTERISTICS

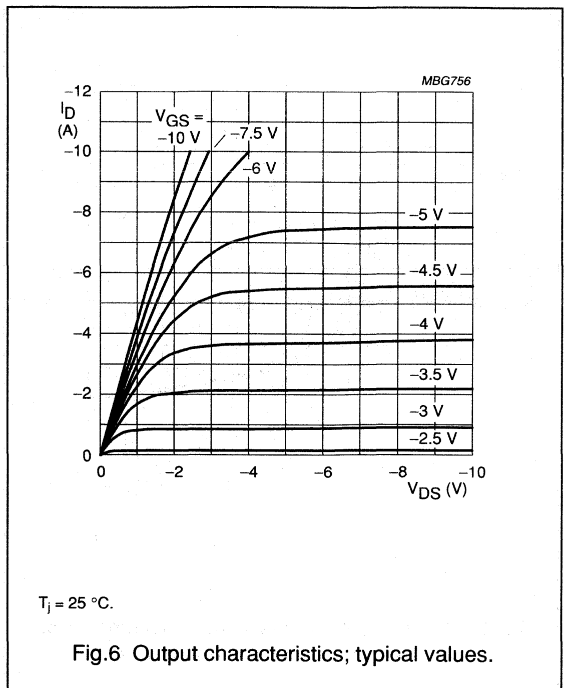
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−30	−	−	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−1	−	−2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −24 V	−	−	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	−	−	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −0.5 A	−	0.33	0.4	Ω
		V_{GS} = −10 V; I_D = −1 A	−	0.22	0.25	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	−	250	−	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	−	140	−	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	−	50	−	pF
Q_G	total gate charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −1 A	−	10	25	nC
Q_{GS}	gate-source charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −1 A	−	1	−	nC
Q_{GD}	gate-drain charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −1 A	−	3	−	nC
Switching times (see Fig.11)						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −1 A; R_L = 15 Ω; R_{gen} = 6 Ω	−	4.5	−	ns
t_f	fall time		−	3.5	−	ns
t_{on}	turn-on switching time		−	8	16	ns
$t_{d(off)}$	turn-off delay time	V_{GS} =−10 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_L = 15 Ω; R_{gen} = 6 Ω	−	25	−	ns
t_r	rise time		−	15	−	ns
t_{off}	turn-off switching time		−	40	80	ns
Source-drain diode						
V_{SD}	source-drain forward voltage	V_{GD} = 0; I_S = −1.25 A	−	−	−1.6	V
t_{rr}	reverse recovery time	I_S = −1.25 A; di/dt = 100 A/μs	−	150	200	ns



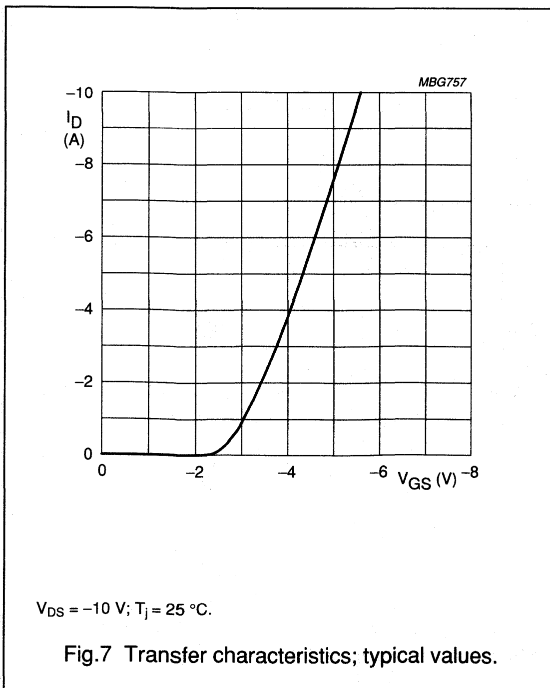
$V_{DD} = -15$ V: $I_D = -1$ A.

Fig.5 Gate-source voltage as a function of total gate charge; typical values.



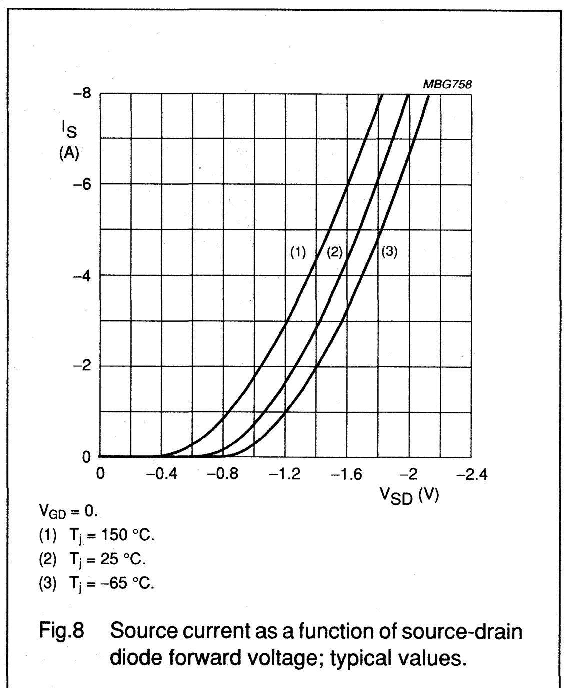
$T_j = 25$ °C.

Fig.6 Output characteristics; typical values.



$V_{DS} = -10$ V; $T_j = 25$ °C.

Fig.7 Transfer characteristics; typical values.



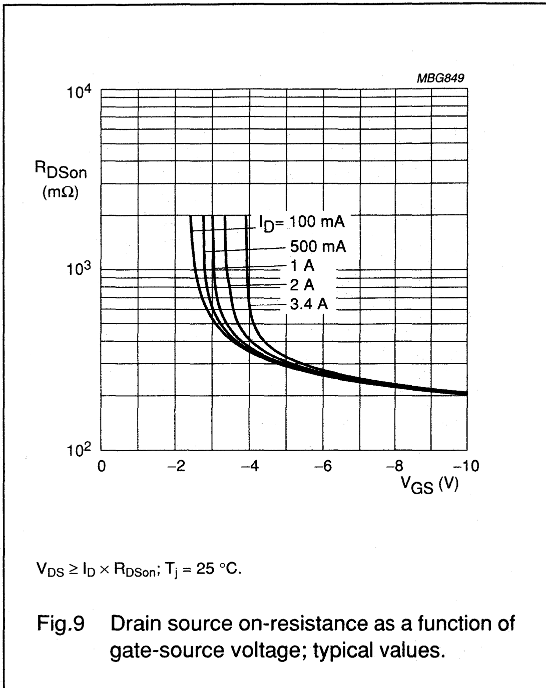
$V_{GD} = 0$.

(1) $T_j = 150$ °C.

(2) $T_j = 25$ °C.

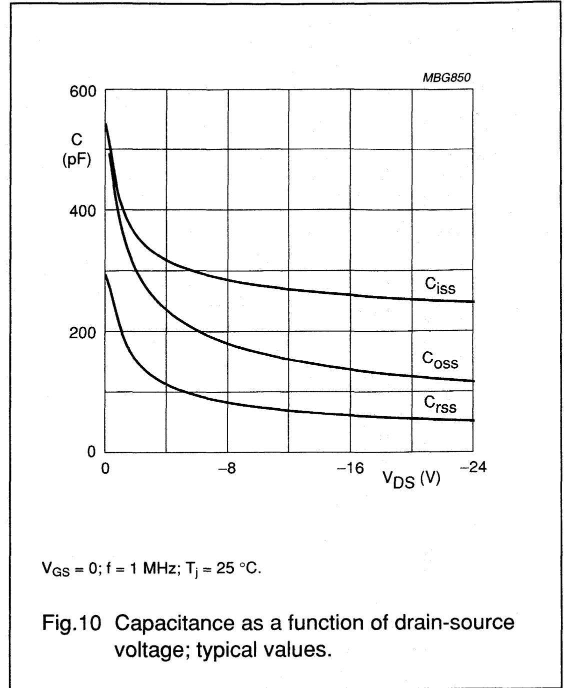
(3) $T_j = -65$ °C.

Fig.8 Source current as a function of source-drain diode forward voltage; typical values.



$V_{DS} \geq I_D \times R_{DSon}$; T_j = 25 °C.

Fig.9 Drain source on-resistance as a function of gate-source voltage; typical values.



V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.10 Capacitance as a function of drain-source voltage; typical values.

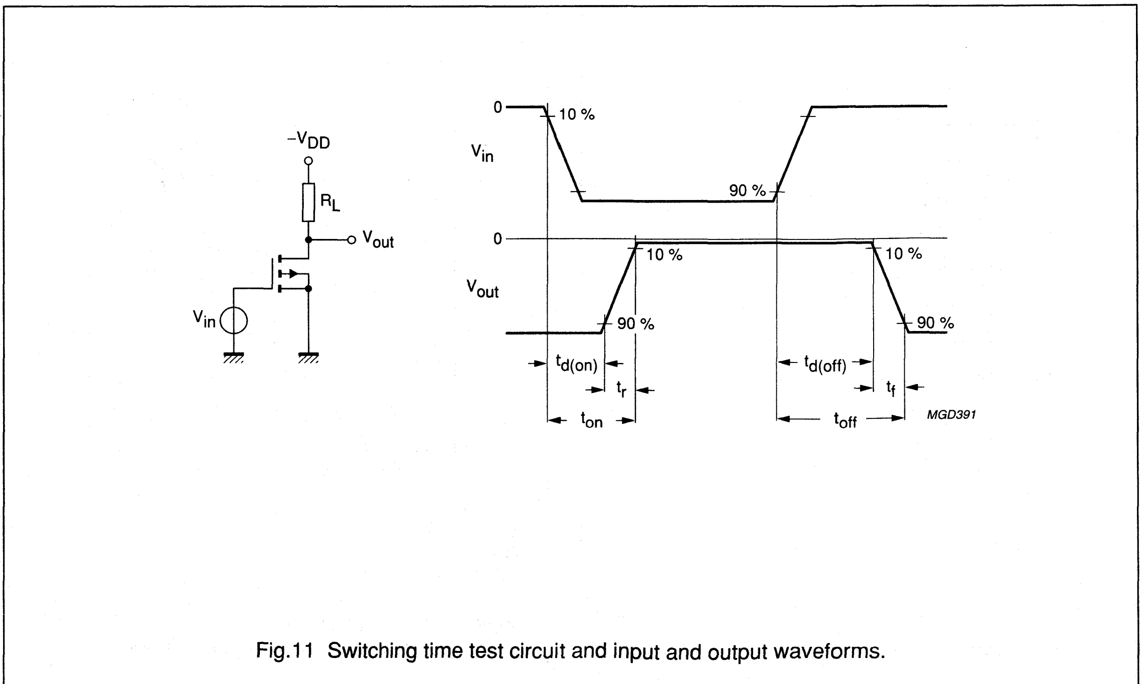
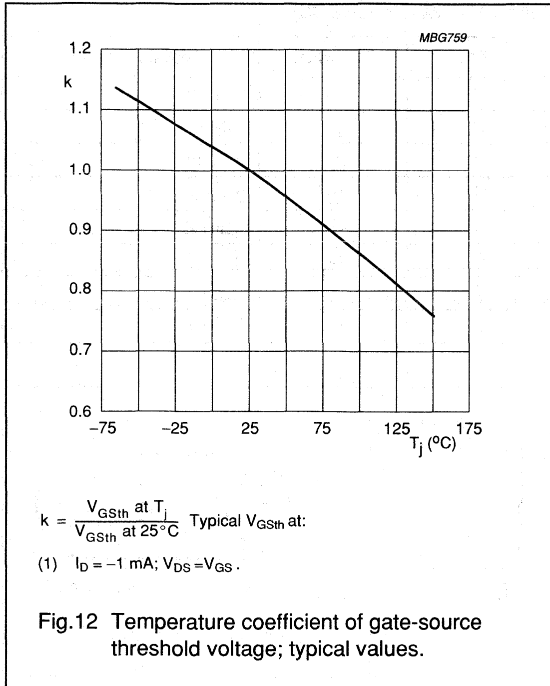


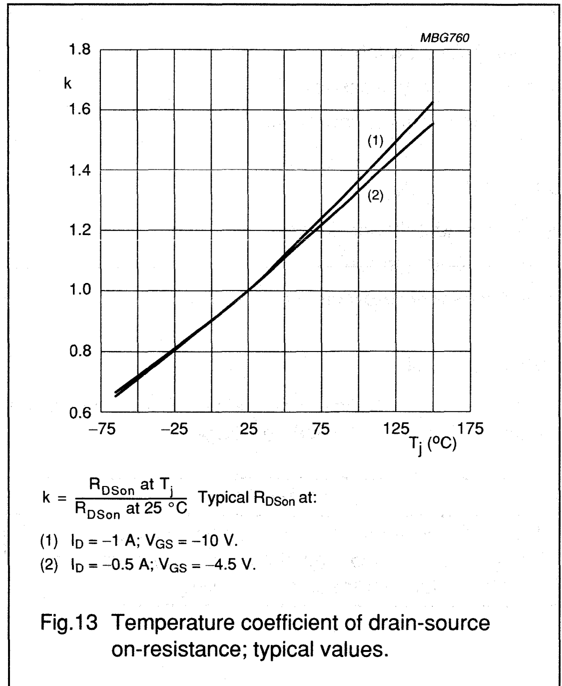
Fig.11 Switching time test circuit and input and output waveforms.



$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$ Typical V_{GSth} at:

(1) $I_D = -1$ mA; $V_{DS} = V_{GS}$.

Fig.12 Temperature coefficient of gate-source threshold voltage; typical values.



$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25 °C}$ Typical R_{DSon} at:

(1) $I_D = -1$ A; $V_{GS} = -10$ V.

(2) $I_D = -0.5$ A; $V_{GS} = -4.5$ V.

Fig.13 Temperature coefficient of drain-source on-resistance; typical values.

Dual P-channel enhancement mode MOS transistor

PHP212

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-state resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

Two P-channel enhancement mode MOS transistors in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

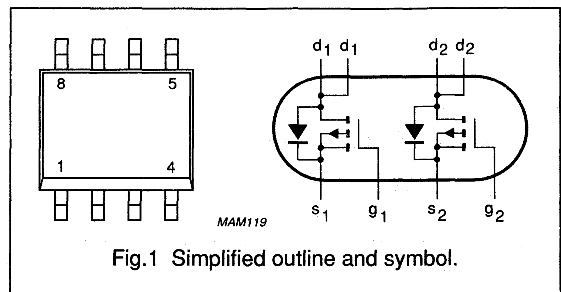


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	$I_S = -1.25$ A	–	–1.3	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	$I_D = -1$ mA; $V_{DS} = V_{GS}$	–1	–2.8	V
I_D	drain current (DC)	$T_s = 80$ °C	–	–4	A
R_{DSon}	drain-source on-state resistance	$I_D = -2$ A; $V_{GS} = -10$ V	–	0.12	Ω
P_{tot}	total power dissipation	$T_s = 80$ °C	–	3.5	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per P-channel					
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	–4	A
I_{DM}	peak drain current	note 2	–	–16	A
P_{tot}	total power dissipation	T_s = 80 °C; note 3	–	3.5	W
		T_{amb} = 25 °C; note 4	–	2.6	W
		T_{amb} = 25 °C; note 5	–	1.1	W
		T_{amb} = 25 °C; note 6	–	1.5	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	–2.6	A
I_{SM}	peak pulsed source current	note 2	–	–10	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 3.5 W at the same time.
4. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
5. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.
6. Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	20	K/W

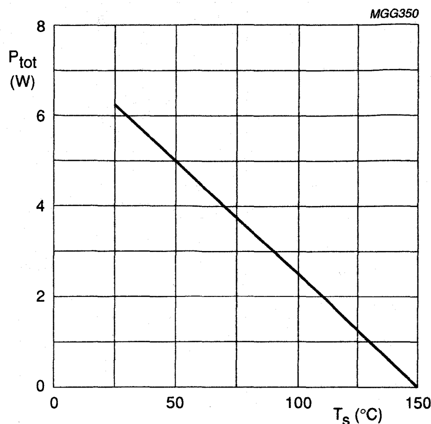
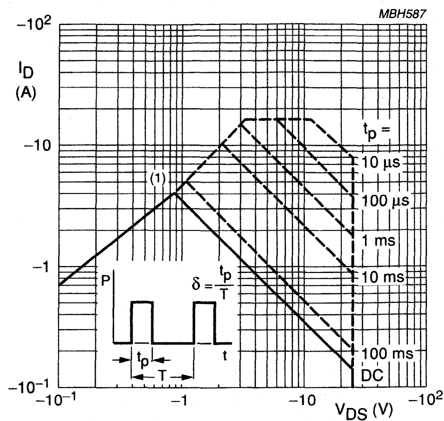


Fig.2 Power derating curve.



$\delta = 0.01$; $T_s = 80$ °C.

(1) R_{DSon} limitation.

Fig.3 SOAR.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per P-channel						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−30	−	−	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−1	−	−2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −24 V	−	−	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	−	−	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −1 A	−	−	0.25	Ω
		V_{GS} = −10 V; I_D = −2 A	−	−	0.12	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	−	450	−	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	−	200	−	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	−	100	−	pF
Q_G	total gate charge	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −2 A	−	13	−	nC
Q_{GS}	gate-source charge	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −2 A	−	1	−	nC
Q_{GD}	gate-drain charge	V_{GS} = −10 V; V_{DD} = −15 V; I_D = −2 A	−	4	−	nC
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω; see Fig.4	−	6	−	ns
t_r	rise time	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω; see Fig.4	−	4	−	ns
t_{on}	turn-on switching time	V_{GS} = 0 to −10 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω; see Fig.4	−	10	−	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω; see Fig.4	−	29	−	ns
t_f	fall time	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω; see Fig.4	−	16	−	ns
t_{off}	turn-off switching time	V_{GS} = −10 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω; see Fig.4	−	45	−	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = −1.25 A	−	−	−1.3	V
t_{rr}	reverse recovery time	I_S = −1.25 A; di/dt = 100 A/μs	−	75	−	ns

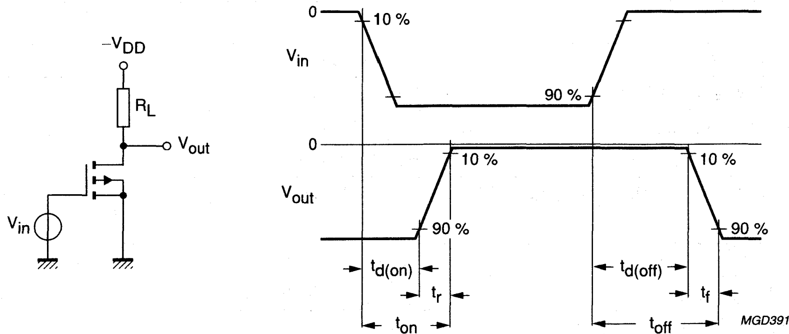
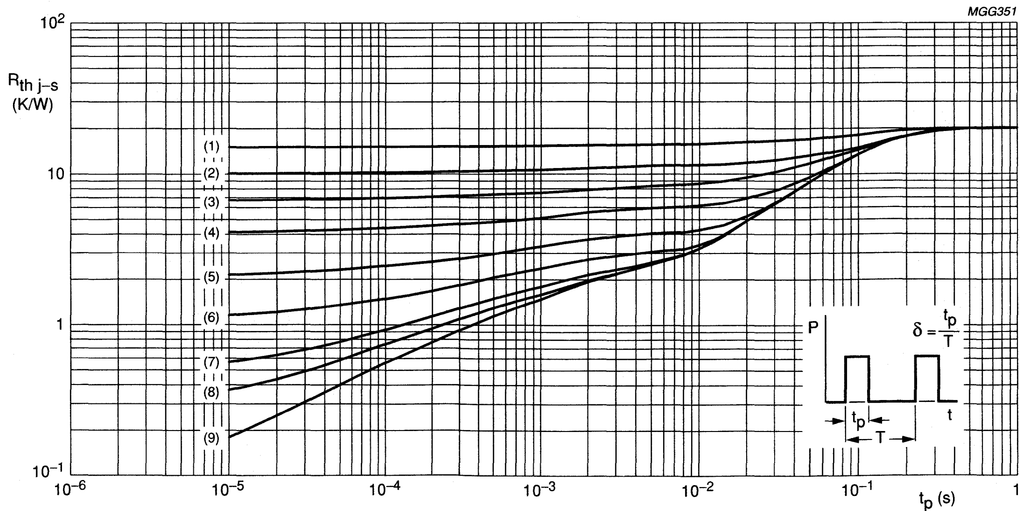


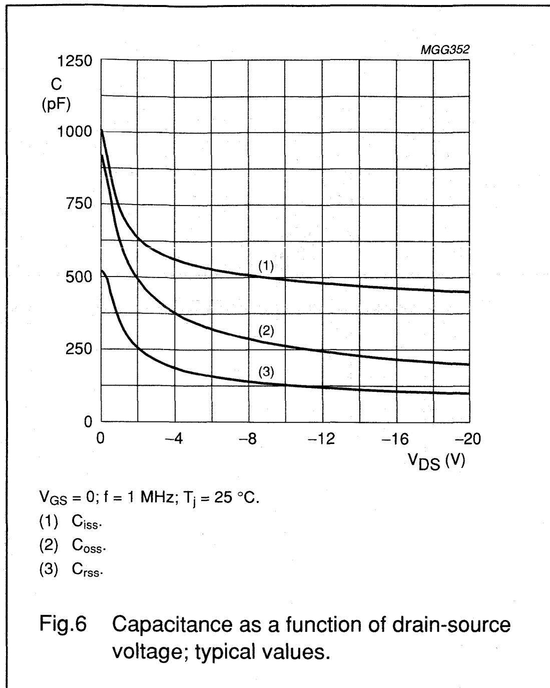
Fig.4 Switching times test circuit; input and output waveforms.



(1) δ = 0.75. (2) δ = 0.5. (3) δ = 0.33. (4) δ = 0.2.

(5) δ = 0.1. (6) δ = 0.05. (7) δ = 0.02. (8) δ = 0.01. (9) δ = 0.

Fig.5 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.



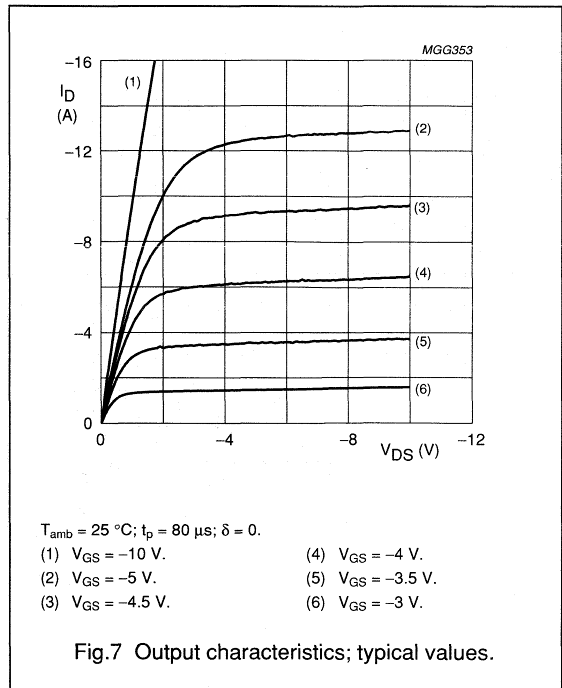
$V_{GS} = 0$; f = 1 MHz; $T_j = 25$ °C.

(1) C_{iss}.

(2) C_{oss}.

(3) C_{rss}.

Fig.6 Capacitance as a function of drain-source voltage; typical values.



$T_{amb} = 25$ °C; $t_p = 80$ µs; δ = 0.

(1) $V_{GS} = -10$ V.

(2) $V_{GS} = -5$ V.

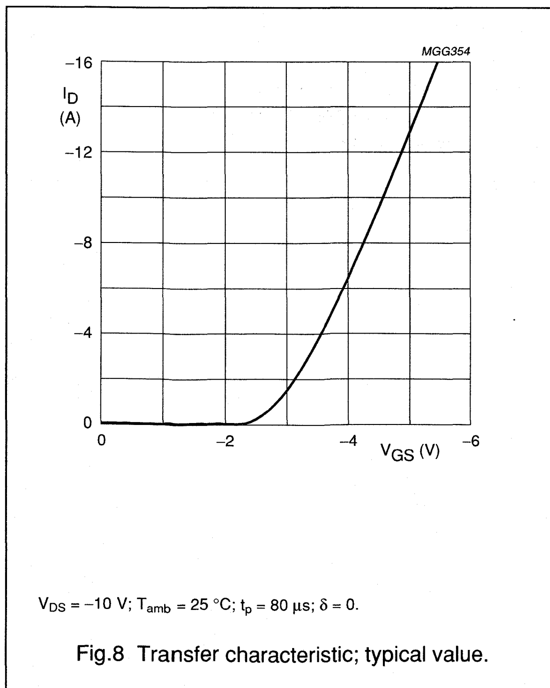
(3) $V_{GS} = -4.5$ V.

(4) $V_{GS} = -4$ V.

(5) $V_{GS} = -3.5$ V.

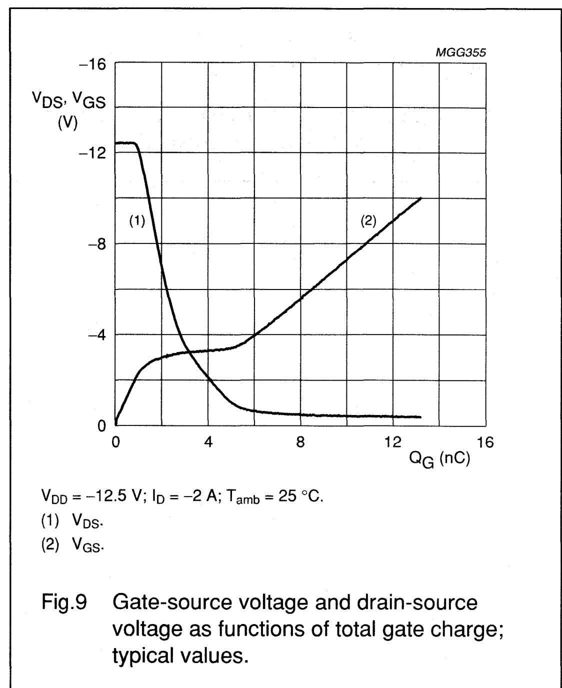
(6) $V_{GS} = -3$ V.

Fig.7 Output characteristics; typical values.



$V_{DS} = -10$ V; $T_{amb} = 25$ °C; $t_p = 80$ µs; δ = 0.

Fig.8 Transfer characteristic; typical value.

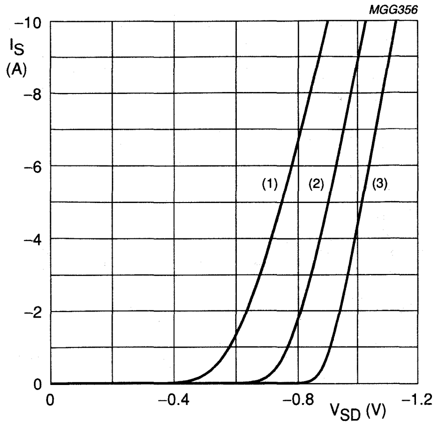


$V_{DD} = -12.5$ V; $I_D = -2$ A; $T_{amb} = 25$ °C.

(1) V_{DS}.

(2) V_{GS}.

Fig.9 Gate-source voltage and drain-source voltage as functions of total gate charge; typical values.



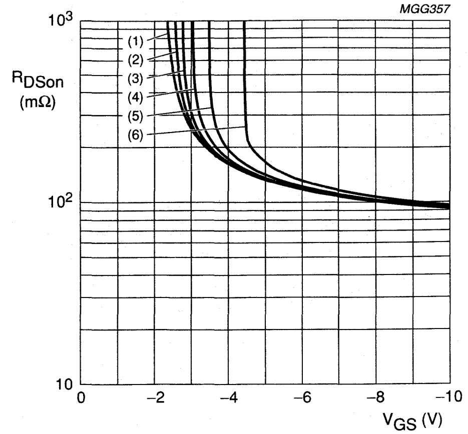
$V_{GD} = 0$.

(1) $T_{amb} = 150$ °C; $t_p = 300$ μs; $\delta = 0$.

(2) $T_{amb} = 25$ °C; $t_p = 300$ μs; $\delta = 0$.

(3) $T_{amb} = -65$ °C; $t_p = 300$ μs; $\delta = 0$.

Fig.10 Source current as a function of source-drain diode forward voltage; typical values.



$T_{amb} = 25$ °C; $t_p = 300$ μs; $\delta = 0$.

$V_{DS} \geq I_D \times R_{DSon}$.

(1) $I_D = 0.1$ A.

(2) $I_D = 0.5$ A.

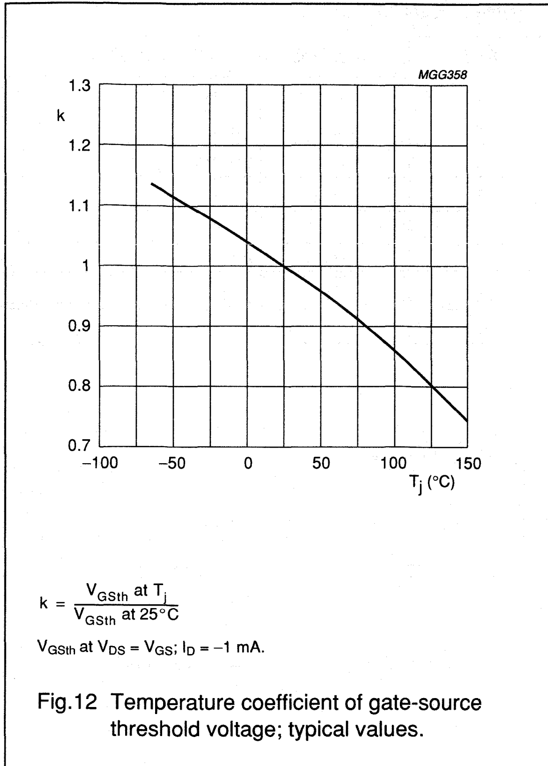
(3) $I_D = 1$ A.

(4) $I_D = 2$ A.

(5) $I_D = 4$ A.

(6) $I_D = 8$ A.

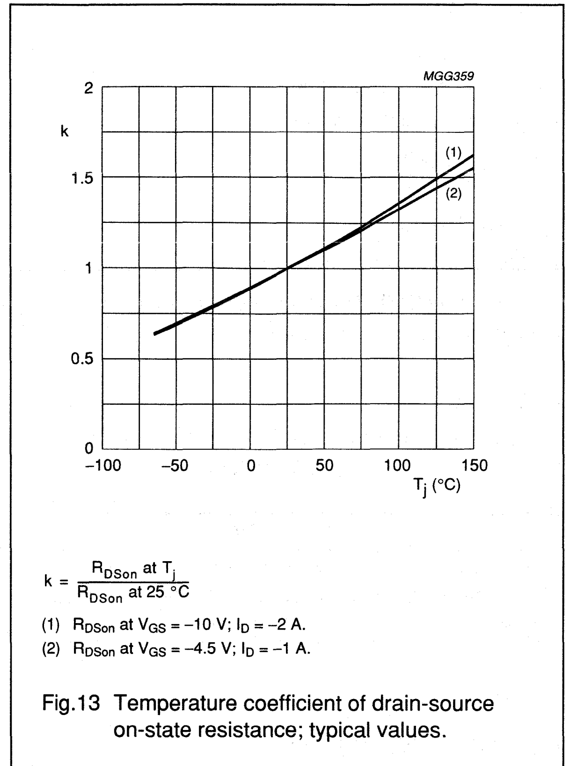
Fig.11 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; $I_D = -1$ mA.

Fig.12 Temperature coefficient of gate-source threshold voltage; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25 °C}$$

(1) R_{DSon} at $V_{GS} = -10$ V; $I_D = -2$ A.

(2) R_{DSon} at $V_{GS} = -4.5$ V; $I_D = -1$ A.

Fig.13 Temperature coefficient of drain-source on-state resistance; typical values.

Dual P-channel enhancement mode MOS transistor

PHP212L

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-state resistance
- Low threshold.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

Two P-channel enhancement mode MOS transistors in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

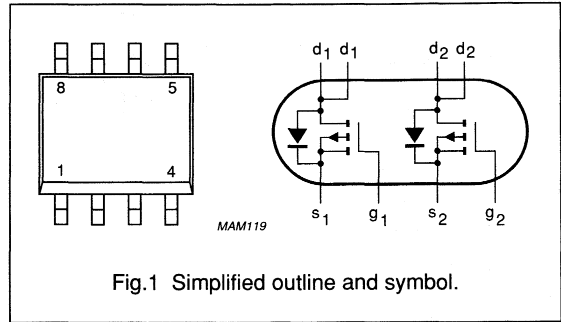


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	I_S = –1.25 A	–	–1.3	V
V_{GS}	gate-source voltage (DC)		–	±12	V
V_{GSth}	gate-source threshold voltage	I_D = –1 mA; V_{DS} = V_{GS}	–0.5	–1.1	V
I_D	drain current (DC)	T_s = 80 °C	–	–4	A
R_{DSon}	drain-source on-state resistance	I_D = –2 A; V_{GS} = –4.5 V	–	0.12	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	3.5	W

OBJECTIVE
See Philips Semiconductors for Design-in information

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per P-channel					
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GS}	gate-source voltage (DC)		–	±12	V
I_D	drain current (DC)	T_s = 80 °C; note 1	–	–4	A
I_{DM}	peak drain current	note 2	–	–16	A
P_{tot}	total power dissipation	T_s = 80 °C; note 3	–	3.5	W
		T_{amb} = 25 °C; note 4	–	2.6	W
		T_{amb} = 25 °C; note 5	–	1.1	W
		T_{amb} = 25 °C; note 6	–	1.5	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 80 °C	–	–2.6	A
I_{SM}	peak pulsed source current	note 2	–	–10	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.
3. Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 3.5 W at the same time.
4. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
5. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.
6. Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	20	K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per P-channel						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−30	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−0.5	–	−1.1	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −24 V	–	–	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±12 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = −2.5 V; I_D = −1 A	–	–	0.25	Ω
		V_{GS} = −4.5 V; I_D = −2 A	–	–	0.12	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	450	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	200	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −24 V; f = 1 MHz	–	100	–	pF
Q_G	total gate charge	V_{GS} = −6 V; V_{DD} = −15 V; I_D = −1 A	–	13	–	nC
Q_{GS}	gate-source charge	V_{GS} = −6 V; V_{DD} = −15 V; I_D = −1 A	–	1	–	nC
Q_{GD}	gate-drain charge	V_{GS} = −6 V; V_{DD} = −15 V; I_D = −1 A	–	4	–	nC
Switching times						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to −6 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω	–	6	–	ns
t_r	rise time	V_{GS} = 0 to −6 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω	–	4	–	ns
t_{on}	turn-on switching time	V_{GS} = 0 to −6 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω	–	10	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = −6 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω	–	29	–	ns
t_f	fall time	V_{GS} = −6 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω	–	16	–	ns
t_{off}	turn-off switching time	V_{GS} = −6 to 0 V; V_{DD} = −15 V; I_D = −1 A; R_{gen} = 6 Ω	–	45	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	V_{GD} = 0; I_S = −1.25 A	–	–	−1.3	V
t_{rr}	reverse recovery time	I_S = −1.25 A; di/dt = 100 A/μs	–	75	–	ns

Dual P-channel enhancement mode MOS transistor

PHP225

FEATURES

- High-speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

- Motor and actuator driver
- Power management
- Synchronized rectification.

DESCRIPTION

Two P-channel enhancement mode MOS transistors in an 8-pin plastic SOT96-1 (SO8) package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s_1	source 1
2	g_1	gate 1
3	s_2	source 2
4	g_2	gate 2
5	d_2	drain 2
6	d_2	drain 2
7	d_1	drain 1
8	d_1	drain 1

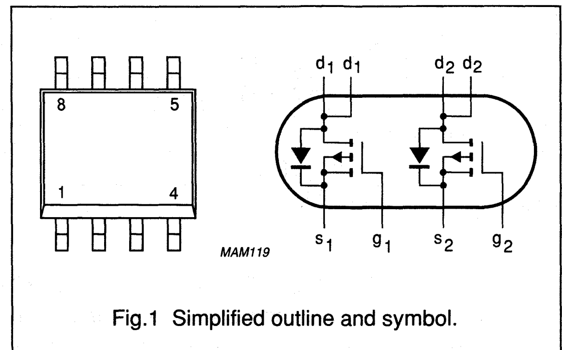


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per P-channel					
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	I_S = –1.25 A	–	–1.6	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = –1 mA; V_{DS} = V_{GS}	–1	–2.8	V
I_D	drain current (DC)		–	–2.3	A
R_{DSon}	drain-source on-state resistance	I_D = –1 A; V_{GS} = –10 V	–	0.25	Ω
P_{tot}	total power dissipation	T_s = 80 °C	–	2	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per P-channel					
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)	$T_s \leq 80$ °C	–	–2.3	A
I_{DM}	peak drain current	note 1	–	–10	A
P_{tot}	total power dissipation	$T_s = 80$ °C; note 2	–	2	W
		$T_{amb} = 25$ °C; note 3	–	2	W
		$T_{amb} = 25$ °C; note 4	–	1	W
		$T_{amb} = 25$ °C; note 5	–	1.3	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C
Source-drain diode					
I_S	source current (DC)	$T_s \leq 80$ °C	–	–1.25	A
I_{SM}	peak pulsed source current	note 1	–	–5	A

Notes

1. Pulse width and duty cycle limited by maximum junction temperature.
2. Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 2 W at the same time.
3. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 27.5 K/W.
4. Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.
5. Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on printed-circuit board with an $R_{th\ a\text{-}tp}$ (ambient to tie-point) of 90 K/W.

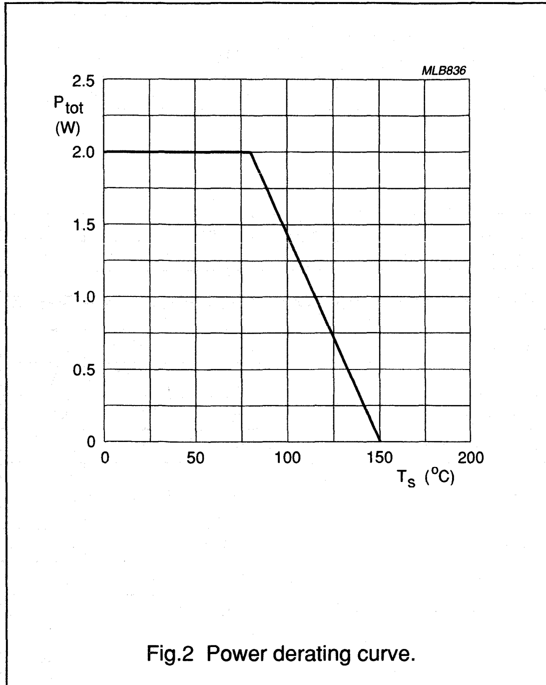
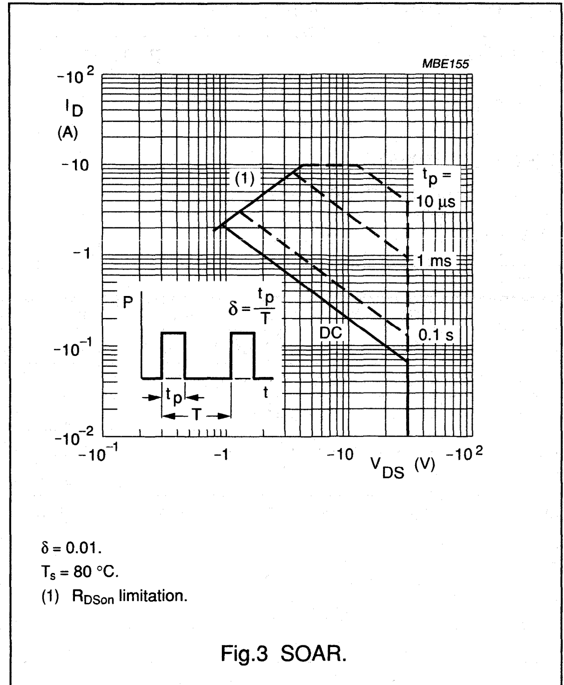


Fig.2 Power derating curve.



$\delta = 0.01$.

$T_s = 80$ °C.

(1) R_{DSon} limitation.

Fig.3 SOAR.

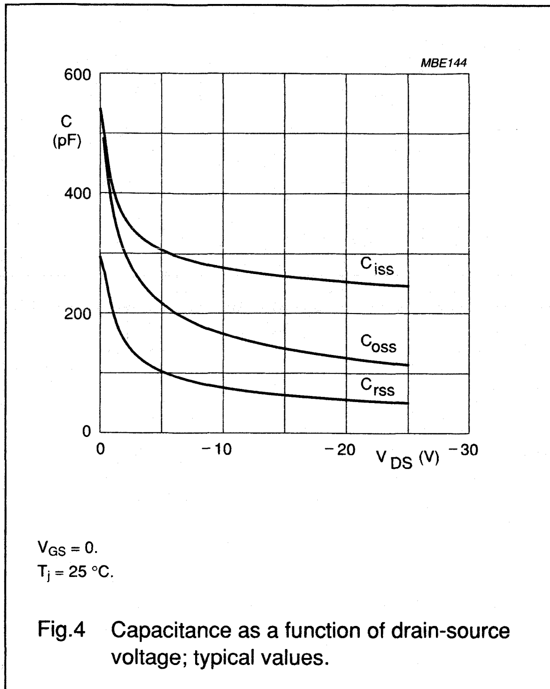
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	35	K/W

CHARACTERISTICS

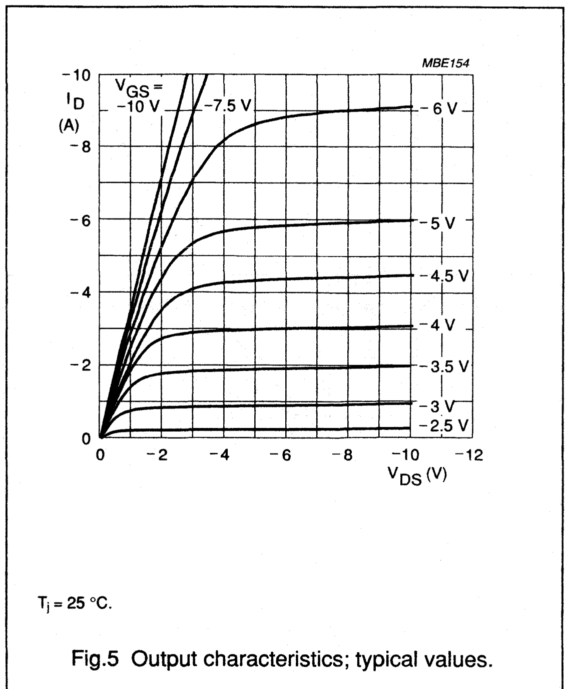
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per P-channel						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = −10 μA	−30	−	−	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = −1 mA	−1	−	−2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = −24 V	−	−	−100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	−	−	±100	nA
I_{Don}	on-state drain current	V_{GS} = −10 V; V_{DS} = −1 V	−2.3	−	−	A
		V_{GS} = −4.5 V; V_{DS} = −5 V	−1	−	−	A
R_{DSon}	drain-source on-state resistance	V_{GS} = −4.5 V; I_D = −0.5 A	−	0.33	0.4	Ω
		V_{GS} = −10 V; I_D = −1 A	−	0.22	0.25	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = −20 V; I_D = −1 A	1	2	−	S
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	−	250	−	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	−	140	−	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = −20 V; f = 1 MHz	−	50	−	pF
Q_G	total gate charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −2.3 A	−	10	25	nC
Q_{GS}	gate-source charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −2.3 A	−	1	−	nC
Q_{GD}	gate-drain charge	V_{GS} = −10 V; V_{DS} = −15 V; I_D = −2.3 A	−	3	−	nC
Switching times						
t_{on}	turn-on time	V_{GD} = 0 to −10 V; V_{DD} = −20 V; I_D = −1 A; R_L = 20 Ω	−	20	80	ns
t_{off}	turn-off time	V_{GS} = −10 to 0 V; V_{DD} = −20 V; I_D = −1 A; R_L = 20 Ω	−	50	140	ns
Source-drain diode						
V_{DS}	source drain diode forward voltage	V_{GD} = 0; I_S = −1.25 A	−	−	−1.6	V
t_{rr}	reverse recovery time	I_S = −1.25 A; di/dt = 100 A/μs	−	150	200	ns



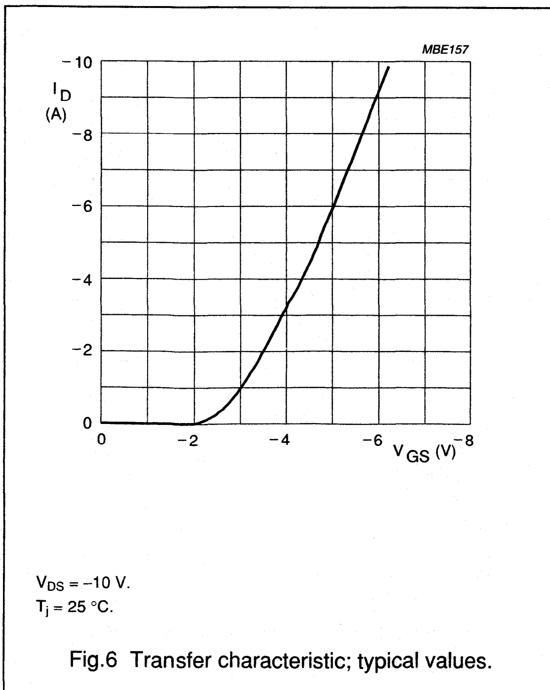
V_{GS} = 0.
T_j = 25 °C.

Fig.4 Capacitance as a function of drain-source voltage; typical values.



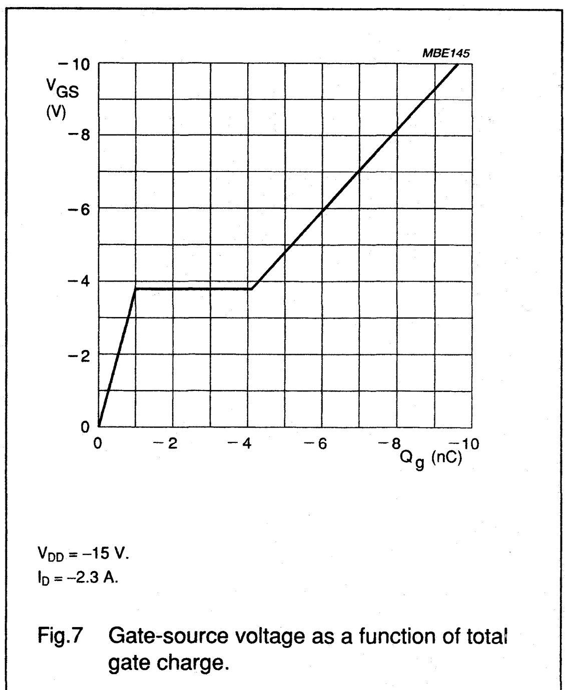
T_j = 25 °C.

Fig.5 Output characteristics; typical values.



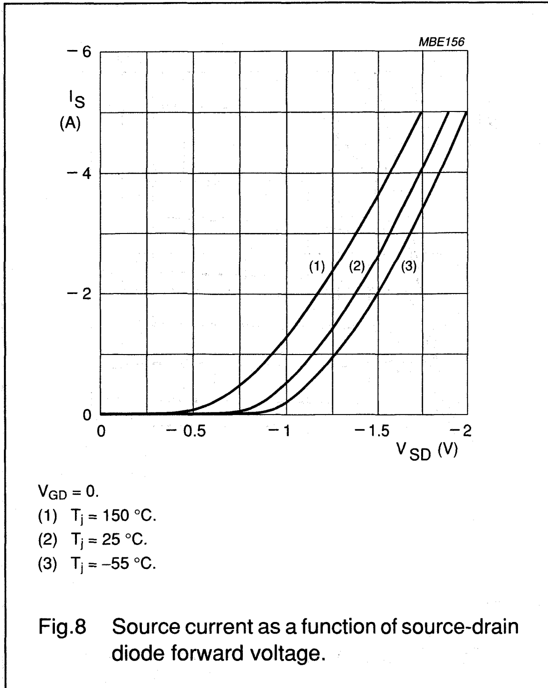
V_{DS} = −10 V.
T_j = 25 °C.

Fig.6 Transfer characteristic; typical values.



V_{DD} = −15 V.
I_D = −2.3 A.

Fig.7 Gate-source voltage as a function of total gate charge.



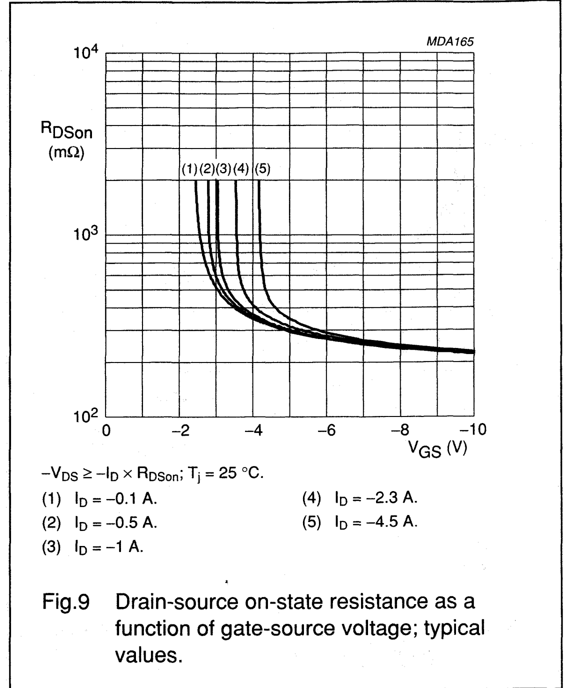
$V_{GD} = 0$.

(1) $T_j = 150$ °C.

(2) $T_j = 25$ °C.

(3) $T_j = -55$ °C.

Fig.8 Source current as a function of source-drain diode forward voltage.



$-V_{DS} \geq -I_D \times R_{DSon}$; $T_j = 25$ °C.

(1) $I_D = -0.1$ A.

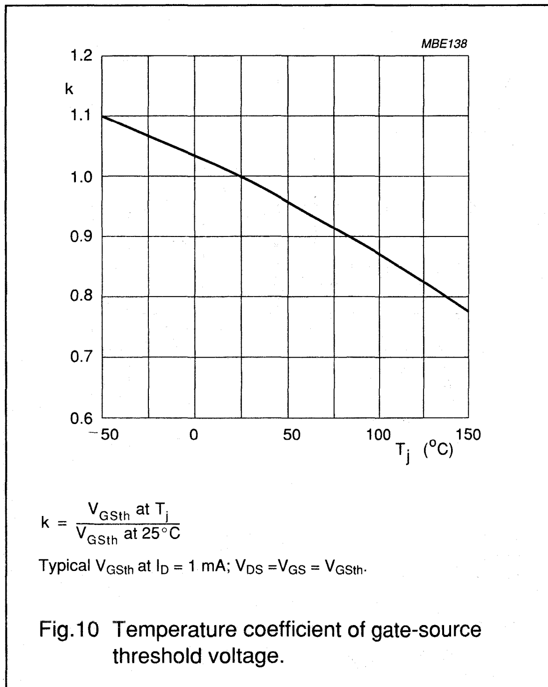
(2) $I_D = -0.5$ A.

(3) $I_D = -1$ A.

(4) $I_D = -2.3$ A.

(5) $I_D = -4.5$ A.

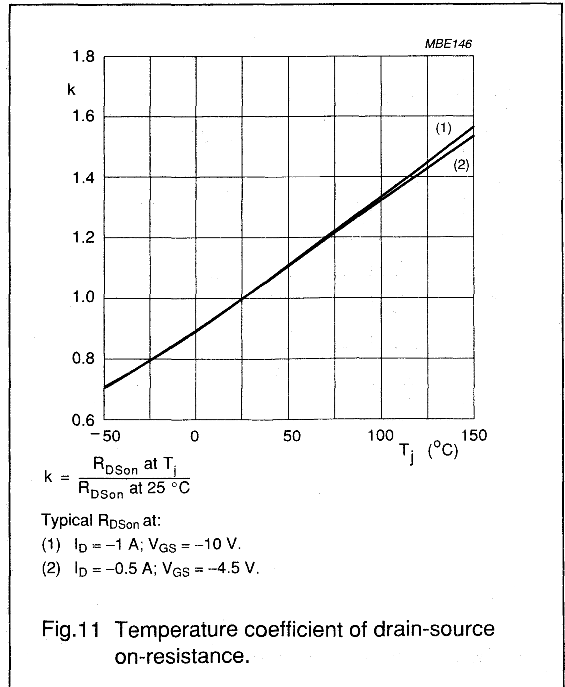
Fig.9 Drain-source on-state resistance as a function of gate-source voltage; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

Typical V_{GSth} at $I_D = 1$ mA; $V_{DS} = V_{GS} = V_{GSth}$.

Fig.10 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25 °C}$$

Typical R_{DSon} at:

(1) $I_D = -1$ A; $V_{GS} = -10$ V.

(2) $I_D = -0.5$ A; $V_{GS} = -4.5$ V.

Fig.11 Temperature coefficient of drain-source on-resistance.

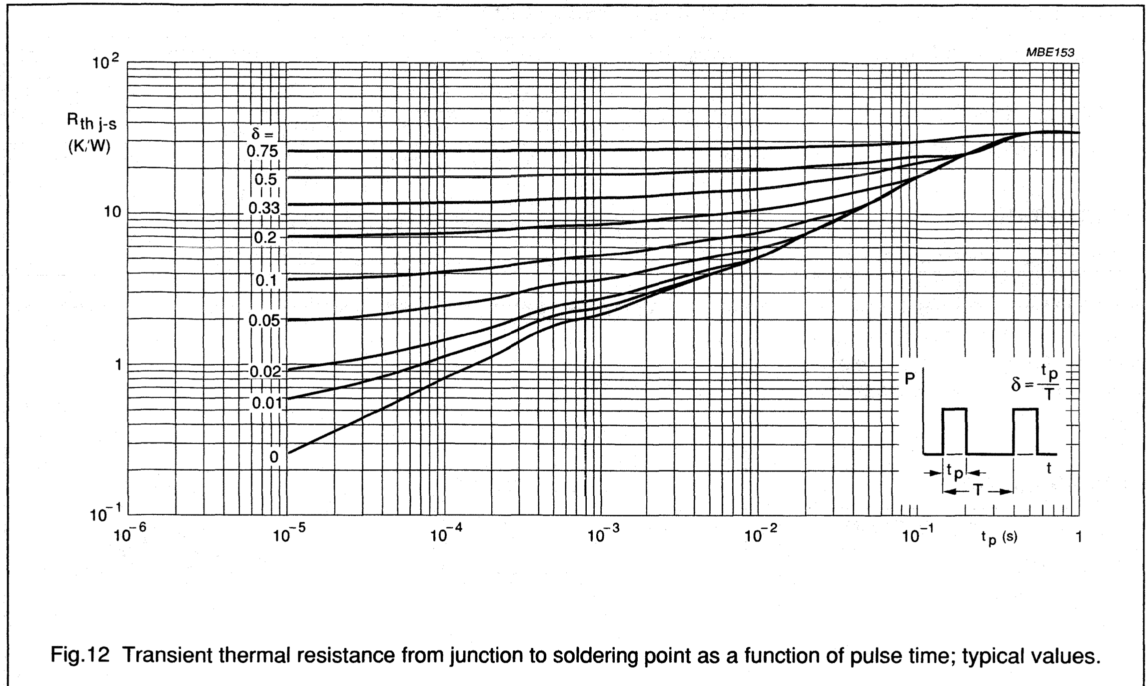


Fig.12 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

N-channel enhancement mode vertical D-MOS transistor

PMBF107

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope and intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - SOT23

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		200	V
I_D	drain current	DC value	100	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA V_{GS} = 2.6 V	28	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	2.4	V

PIN CONFIGURATION

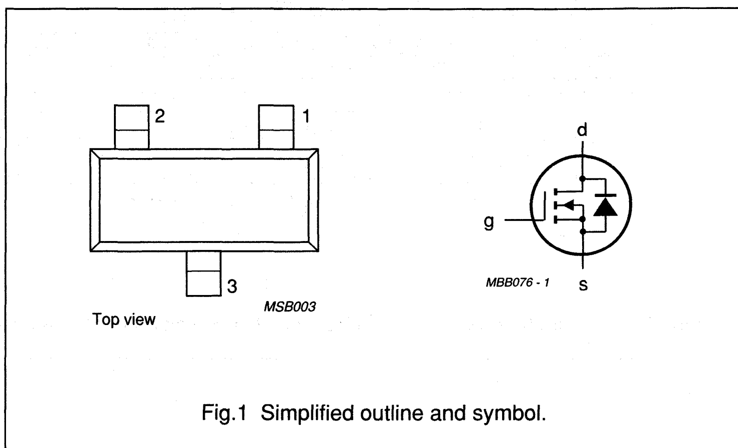


Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	200	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	drain current	DC value	–	100	mA
I_{DM}	drain current	peak value	–	250	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C (note 1)	–	250	mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Note

1. Device mounted on an FR4 printboard.

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient (note 1)	500	K/W

Note

1. Device mounted on an FR4 printboard.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	200	–	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 130 V V_{GS} = 0	–	–	30	nA
I_{DSX}	drain cut-off current	V_{DS} = 70 V V_{GS} = 0.2 V	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS}$ = 15 V V_{DS} = 0	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA $V_{GS} = V_{DS}$	0.8	–	2.4	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 20 mA V_{GS} = 2.6 V	–	20	28	Ω
		I_D = 150 mA V_{GS} = 10 V	–	14	–	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 250 mA V_{DS} = 15 V	90	180	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	50	65	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	16	25	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	4	10	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	I_D = 250 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	2	10	ns
t_{off}	turn-off time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	5	20	ns

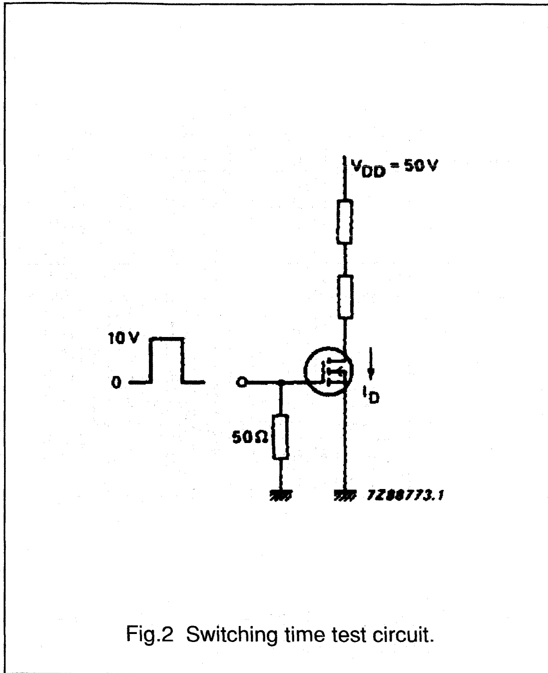


Fig.2 Switching time test circuit.

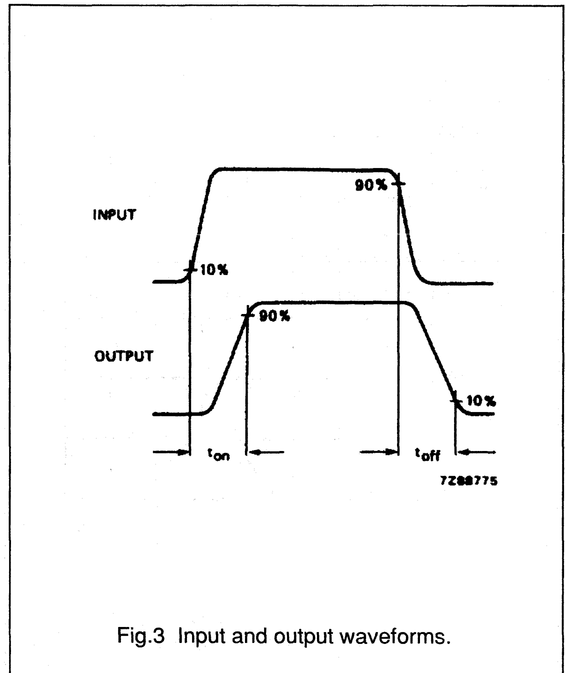


Fig.3 Input and output waveforms.

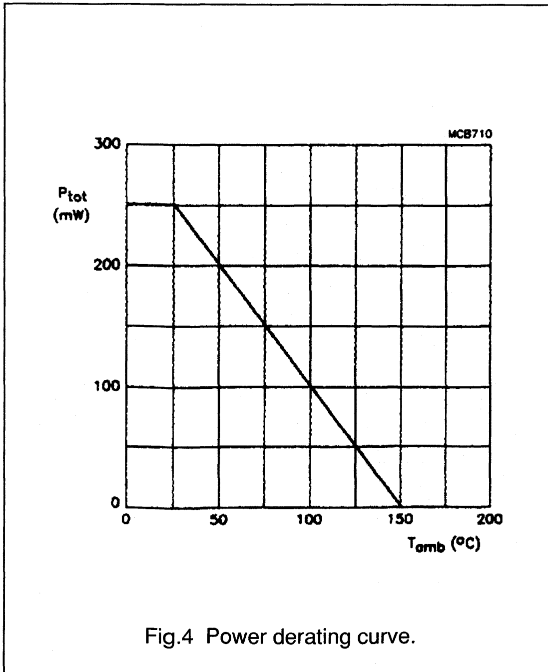


Fig.4 Power derating curve.

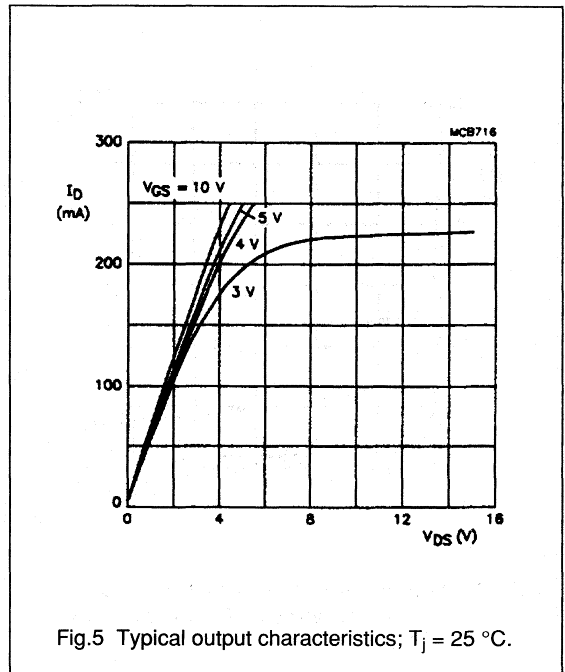


Fig.5 Typical output characteristics; T_j = 25 °C.

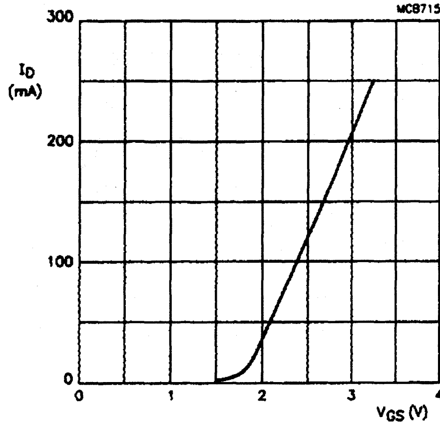


Fig.6 Typical transfer characteristic; V_{DS} = 10 V; T_j = 25 °C.

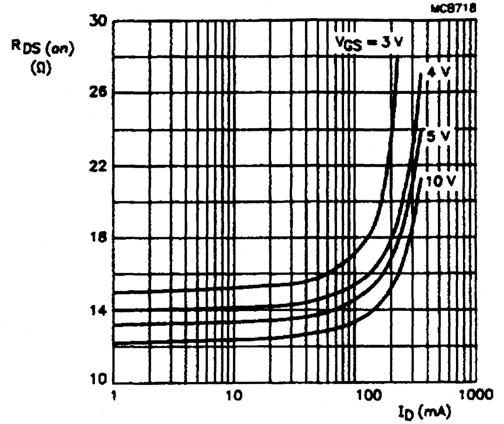


Fig.7 Typical on-resistance as a function of drain current; T_j = 25 °C.

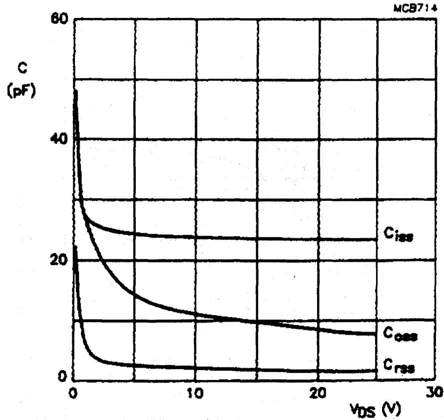


Fig.8 Typical capacitances as a function of drain-source voltage; V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

N-channel enhancement mode vertical D-MOS transistor

PMBF170

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope. Designed for use as a Surface Mounted Device (SMD) in thin and thick-film circuits with applications in relay, high-speed and line transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Drain-source on-resistance	$R_{DS(on)}$	typ.	2.5	Ω
I_D = 200 mA; V_{GS} = 10 V		max.	5.0	Ω
Transfer admittance	$\|Y_{fs}\|$	min.	100	mS
I_D = 200 mA; V_{DS} = 10 V		typ.	200	mS

PINNING - SOT23

1 = gate
2 = source
3 = drain

Marking code:

PMBF170 = pKX

PIN CONFIGURATION

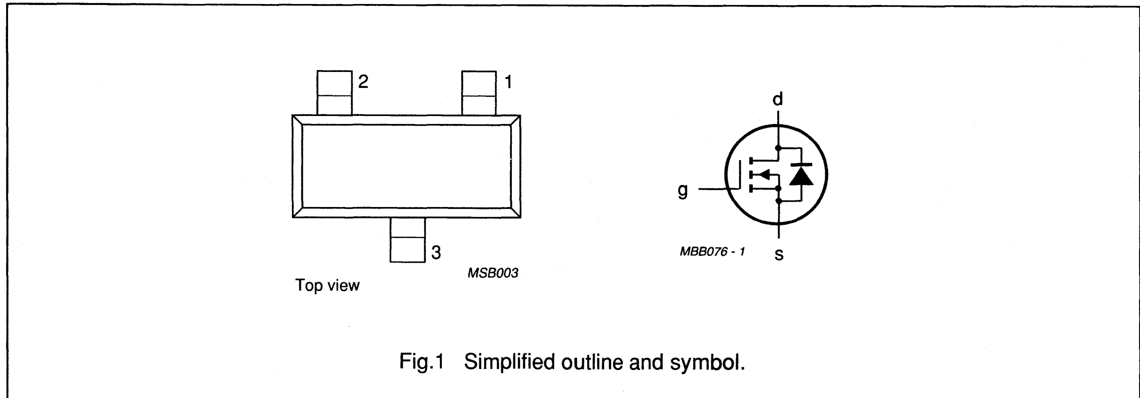


Fig.1 Simplified outline and symbol.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	60	V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20	V
Drain current (DC)	I_D	max.	250	mA
Drain current (peak)	I_{DM}	max.	500	mA
Total power dissipation up to		max.	300	mW (note 1)
T_{amb} = 25 °C (note 1)	P_{tot}	max.	250	mW (note 2)
Storage temperature range	T_{stg}		−65 to +150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j\text{-}a}$	=	430	K/W
From junction to ambient (note 2)	$R_{th\ j\text{-}a}$	=	500	K/W

Notes

1. Mounted on ceramic substrate measuring 10 mm × 8 mm × 0.7 mm.
2. Mounted on printed-circuit board.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Parameter / conditions	Symbol		Value	Unit
Drain-source breakdown voltage				
I_D = 10 μA; V_{GS} = 0	$V_{(BR)DSS}$	min.	60	V
		typ.	90	V
Drain-source leakage current				
V_{DS} = 25 V; V_{GS} = 0	I_{DSS}	max.	500	nA
V_{DS} = 48 V; V_{GS} = 0	I_{DSS}	max.	1	μA
Gate-source leakage current				
V_{GS} = 15 V; V_{DS} = 0	I_{GSS}	max.	10	nA
Gate-source cut-off voltage				
I_D = 1 mA; V_{DS} = V_{GS}	$V_{GS(th)}$	min.	0.8	V
		max.	3.0	V
Drain-source on-resistance				
I_D = 200 mA; V_{GS} = 10 V	$R_{DS(on)}$	typ.	2.5	Ω
		max.	5.0	Ω
Transfer admittance				
I_D = 200 mA; V_{DS} = 10 V	$\|Y_{fs}\|$	min.	100	mS
		typ.	200	mS
Input capacitance				
V_{DS} = 10 V; V_{GS} = 0 V; f = 1 MHz	C_{iss}	typ.	25	pF
		max.	40	pF
Output capacitance				
V_{DS} = 10 V; V_{GS} = 0 V; f = 1 MHz	C_{oss}	typ.	22	pF
		max.	30	pF
Feedback capacitance				
V_{DS} = 10 V; V_{GS} = 0 V; f = 1 MHz	C_{rss}	typ.	6	pF
		max.	10	pF
Switching times				
V_{GS} = 0 to 10 V; I_D = 200 mA ; V_{DD} = 50 V	t_{on}	max.	10	ns
	t_{off}	max.	15	ns

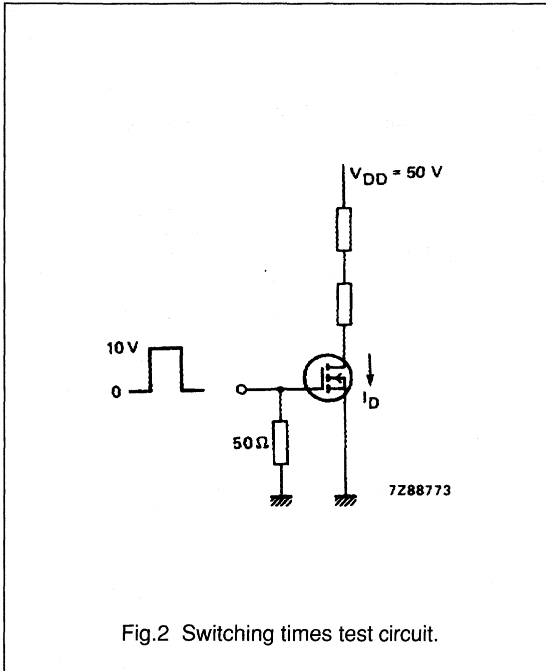


Fig.2 Switching times test circuit.

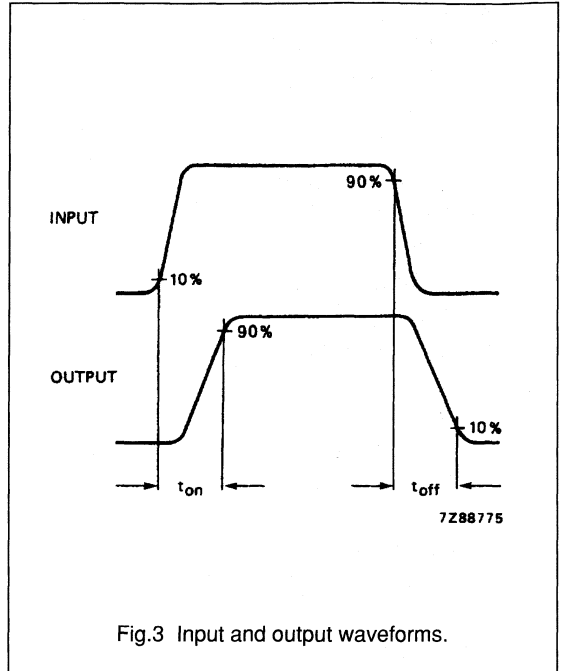


Fig.3 Input and output waveforms.

PACKAGE OUTLINES

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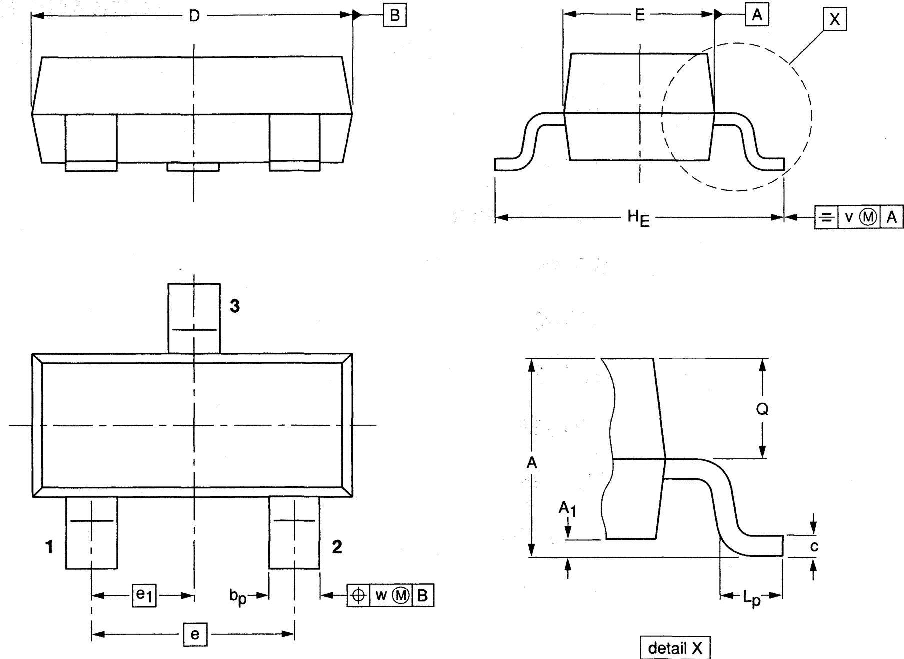
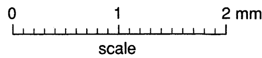
Plastic surface mounted package; 3 leads

SOT23



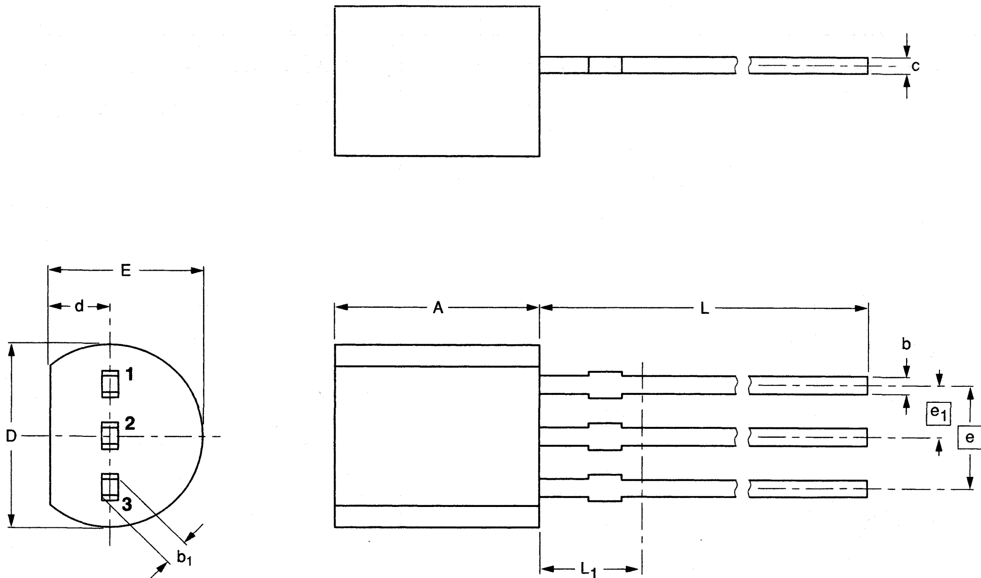


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max.	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT23						97-02-28

Plastic single-ended leaded (through hole) package; 3 leads **SOT54**



DIMENSIONS (mm are the original dimensions)

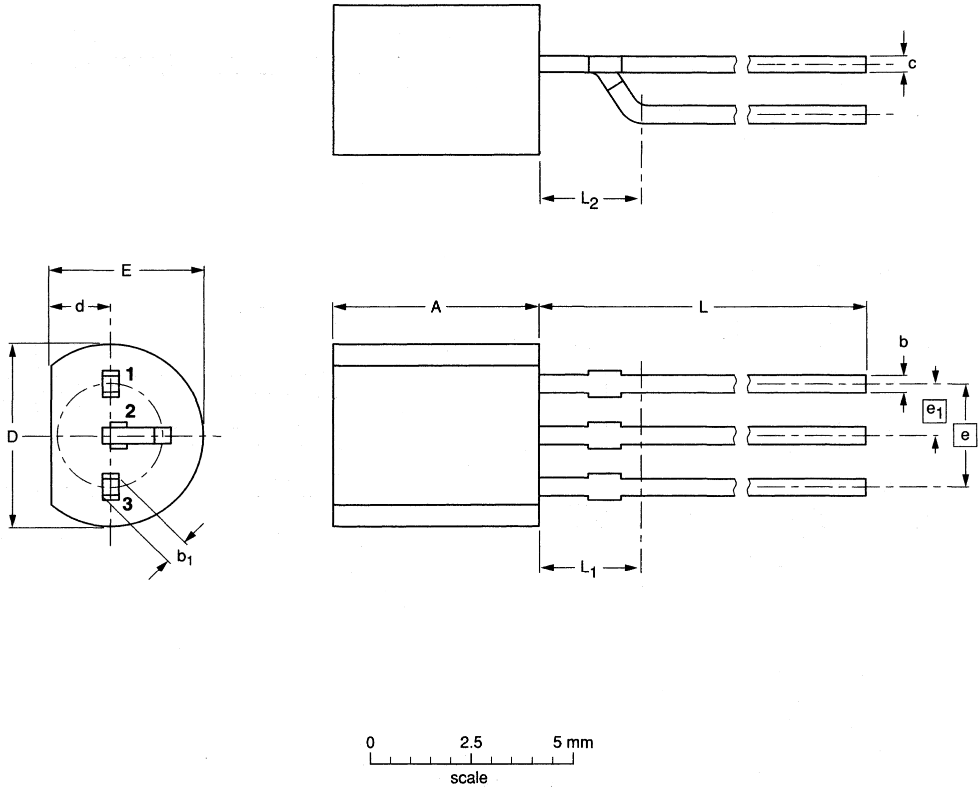
UNIT	A	b	b_1	c	D	d	E	e	e_1	L	L_1(1)
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54		TO-92	SC-43			97-02-28

Plastic single-ended leaded (through hole) package; 3 leads (on-circle) **SOT54 variant**



DIMENSIONS (mm are the original dimensions)

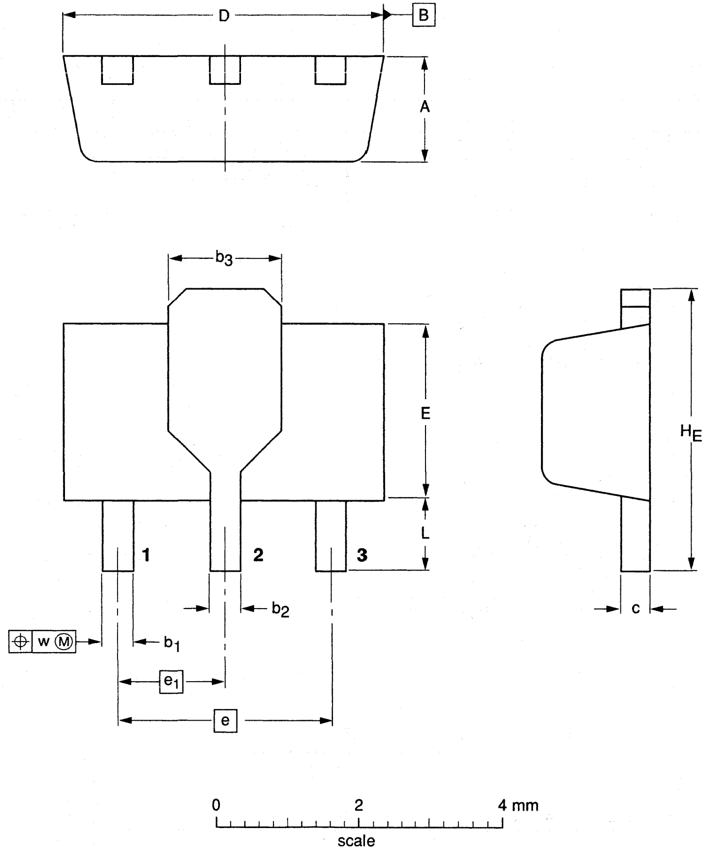
UNIT	A	b	b_1	c	D	d	E	e	e_1	L	$L_1^{(1)}$ max	L_2 max
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5	2.5

Notes

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54 variant		TO-92	SC-43			97-04-14

Plastic surface mounted package; drain pad for good heat transfer; 3 leads **SOT89**

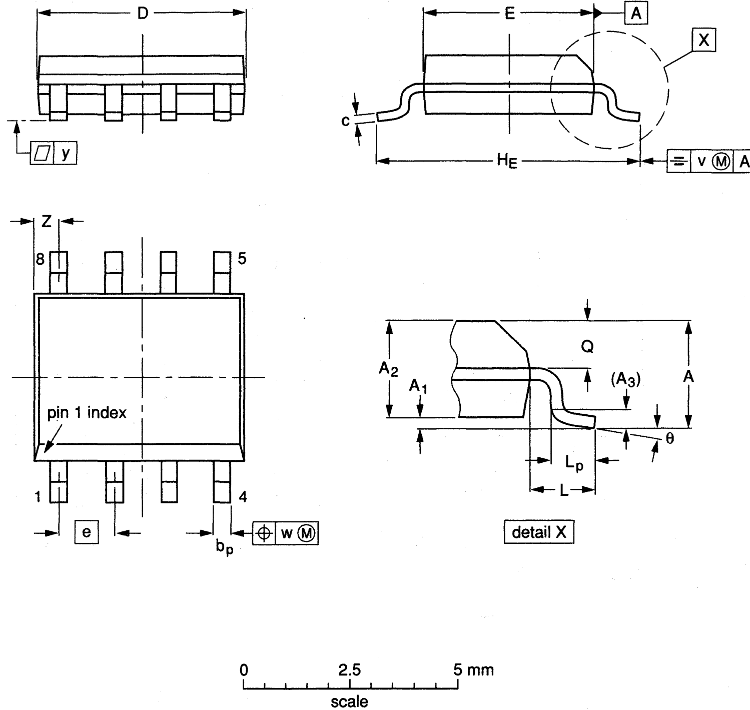


DIMENSIONS (mm are the original dimensions)

UNIT	A	b_1	b_2	b_3	c	D	E	e	e_1	H_E	L min.	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.37	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	0.8	0.13

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT89						97-02-28

SO8: plastic small outline package; 8 leads; body width 3.9 mm — SOT96-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

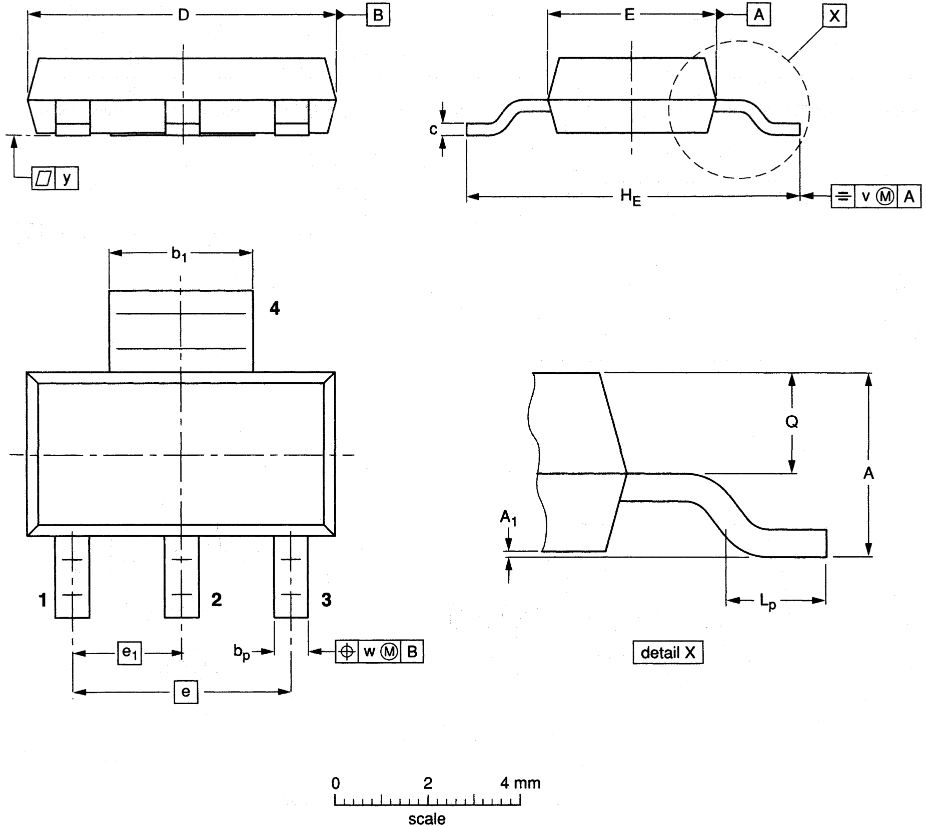
UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~95-02-04~~ 97-05-22

Plastic surface mounted package; collector pad for good heat transfer; 4 leads **SOT223**

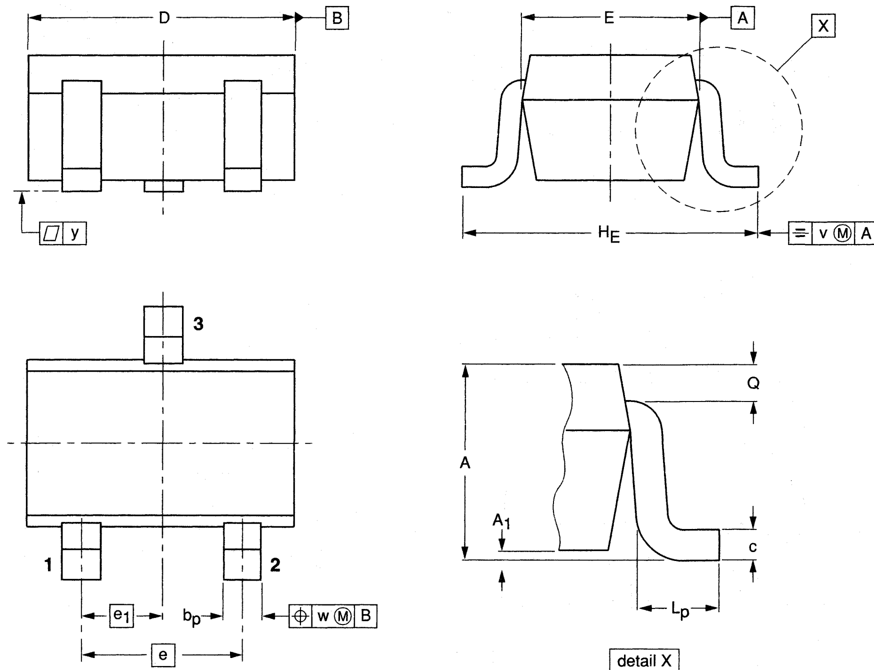


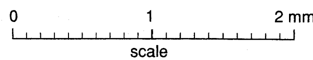
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT223						~~96-11-11~~ 97-02-28

Plastic surface mounted package; 3 leads **SOT323**



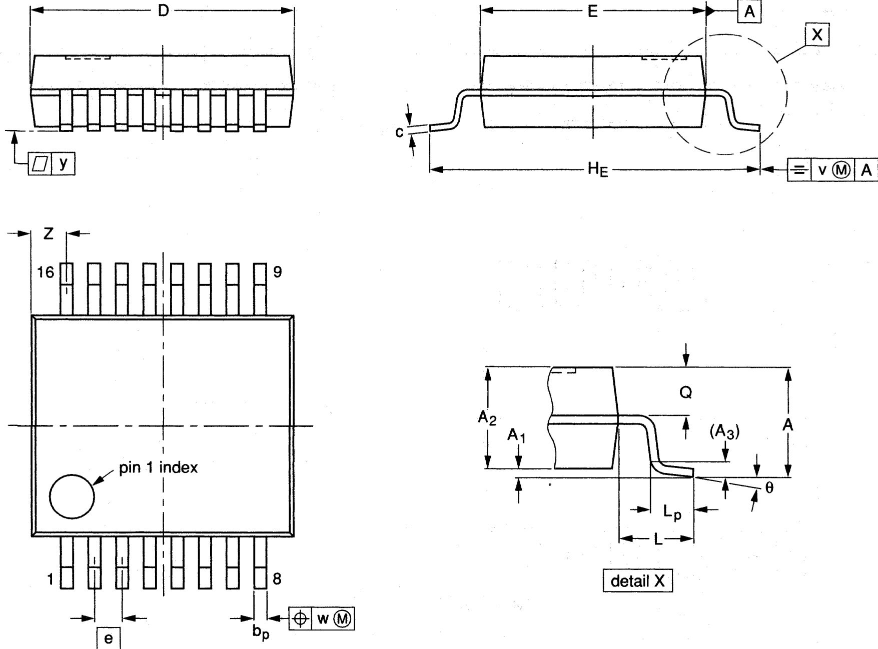


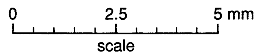
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.8	0.1	0.4 0.3	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT323			SC-70			97-02-28

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

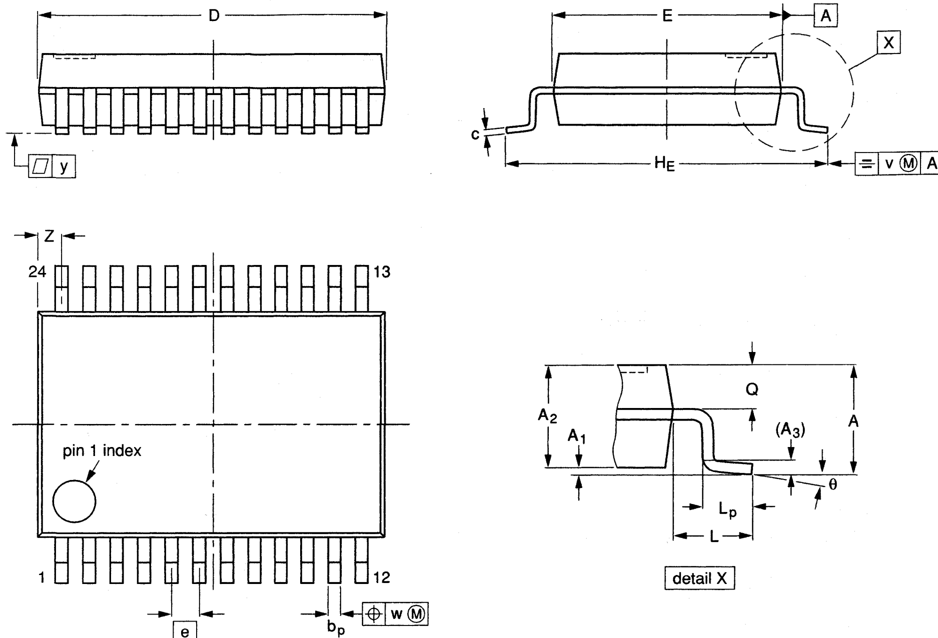
Note

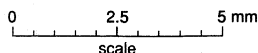
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				~~94-01-14~~ 95-02-04

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1





DIMENSIONS (mm are the original dimensions)

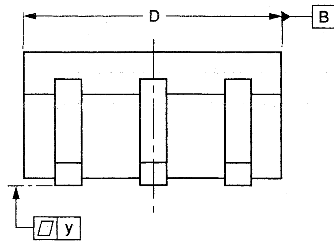
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

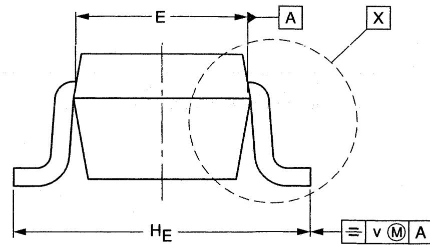
Note

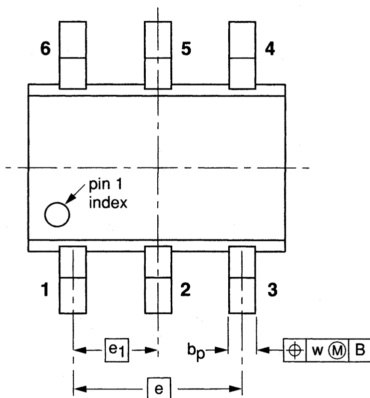
1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

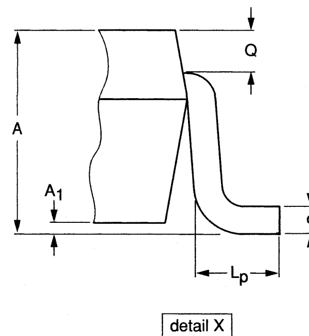
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				~~93-09-08~~ 95-02-04

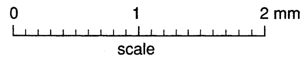
Plastic surface mounted package; 6 leads **SOT363**











DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT363			SC-88			97-02-28

MOUNTING AND SOLDERING

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INTRODUCTION

There are two basic forms of electronic component construction, those with leads for through-hole mounting and (micro)miniature types for surface mounting. Through-hole mounting gives a very rugged construction and uses well established soldering methods. Surface mounting has the advantages of high packing density plus high-speed automated assembly.

LEADED DEVICES

The following general rules are for the save handling and soldering of leaded devices. Special rules for particular types may apply and, for these, instructions are given in the individual data sheets. With all components, excessive forces or heat can cause serious damage and should always be avoided.

Handling

- Avoid perpendicular forces on the body of the device
- Avoid sudden forces on the leads or body. These forces are often much greater than allowed
- Avoid high acceleration as a result of any shock, e.g. dropping the device on a hard surface
- During bending, support the leads between body or stud and the bending point
- During the bending process, axial forces on the body must not exceed 20 N
- Bending the leads through 90° is allowed at any distance from the body when it is possible to support the leads during bending without contacting the body or weldings
- Bending close to the body or stud without supporting the leads is only allowed if the bend radius is greater than 0.5 mm
- Twisting the leads is allowed at any distance from the body or stud only if the lead is properly clamped between body or stud and the twisting point
- Without clamping, twisting the leads is allowed only at a distance of greater than 3 mm from the body; the torque angle must not exceed 30°
- Straightening bent leads is allowed only if the applied pulling force in the axial direction does not exceed 20 N and the total pull duration is not longer than 5 s.

Soldering

- Avoid any force on the body or leads during or immediately after soldering
- Do not correct the position of an already soldered device by pushing, pulling or twisting the body
- Avoid fast cooling after soldering.

The maximum allowable soldering time is determined by:

- Package type
- Mounting environment
- Soldering method
- Soldering temperature
- Distance between the point of soldering and the seal of the device's body.

SURFACE-MOUNT DEVICES

Since the introduction of Surface Mount Devices (SMDs), component design and manufacturing techniques have changed almost beyond recognition. Smaller pitch, minimum footprint area and reduced component volume all contribute to a more compact circuit assembly. As a consequence, when designing printed circuit boards (PCBs), the dimensions of the footprints are perhaps more crucial than ever before.

One of the first steps in this design process is to consider which soldering method, either wave or reflow, will be used during production. This determines not only the solder footprint dimensions, but also the minimum spacing between components, the available area underneath the component where tracks may be laid, and possibly the required component orientation during soldering.

Although reflow soldering is recommended for SMDs, many manufacturers use, and will continue to use for some time to come, a mixture of surface-mount and through-hole components on one substrate (a mixed print).

The mix of components affects the soldering methods that can be applied. A substrate having SMDs mounted on one or both sides but no through-hole components is likely to be suitable for reflow or wave soldering. A double sided mixed print that has through-hole components and some SMDs on one side and densely packed SMDs on the other normally undergoes a sequential combination of reflow and wave soldering. When the mixed print has only through-hole components on one side and all SMDs on the other, wave soldering is usually applied.

To help with your circuit board design, this guideline gives an overview of both reflow and wave soldering methods, and is followed by some useful hints on hand soldering for repair purposes, and the recommended footprints for our SMD discrete semiconductor packages.

Reflow soldering process

There are three basic process steps for single-sided PCB reflow soldering, these are:

1. Applying solder paste to the PCB
2. Component placement
3. Reflow soldering.

APPLYING SOLDER PASTE TO THE PCB

Solder paste can be applied to the PCBs solder lands by one of either three methods: dispensing, screen or stencil printing.

Dispensing is flexible but is slow, and only suitable for pitches of 0.65 mm and above.

With screen printing, a fine-mesh screen is placed over the PCB and the solder paste is forced through the mesh onto the solder lands of the PCB. However, because of mesh aperture limitations (emulsion resolution), this method is only suitable for solder paste deposits of 300 μm and wider.

Stencil printing is similar to screen printing, except that a metal stencil is used instead of a fine-mesh screen. The stencil is usually made of stainless steel or bronze and should be 150 to 200 μm thick. A squeegee is passed across the stencil to force solder paste through the apertures in the stencil and onto the solder lands on the PCB (see Fig.1). It does not suffer from the same limitations as the other two printing methods and so is the preferred method currently available.

It is recommended that for solder paste printing, the equipment is located in a controlled environment maintained at a temperature of 23 ±2 °C, and a relative humidity between 45% and 75%.

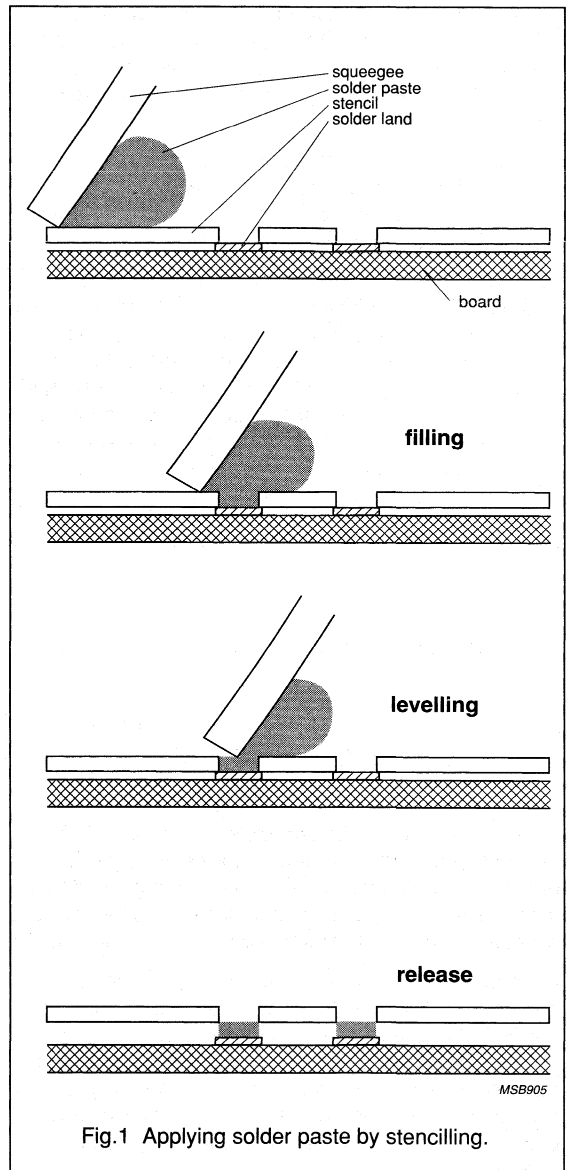


Fig.1 Applying solder paste by stencilling.

Stencil printing

The printing process must be able to apply the solder paste deposits to the PCB:

- In the correct amounts
- At the correct position on the lands
- With an acceptable height and shape.

The amount of solder paste used must be sufficient to give reliable soldered joints. This amount is controlled by the stencil thickness, aperture dimensions, process settings, and the volume of paste pressed through the apertures by the squeegee.

The downward force of the squeegee is counteracted by the hydrodynamic pressure of the paste, and so the machine should be set to ensure that the stencil is just 'cleaned' by the squeegee.

Suitable aperture dimensions depend on the stencil thickness. The solder paste deposits must have a flat part on the top (Fig.2, examples 4 and 5), which can be achieved by correct process settings. The footprints given in this book were designed for these correct deposit types. Stencil apertures that are too small result in irregular dots on the lands (Fig.2, examples 1 to 3). If the apertures are too large, solder paste can be scooped out, particularly if a rubber squeegee is used (Fig.2, example 6).

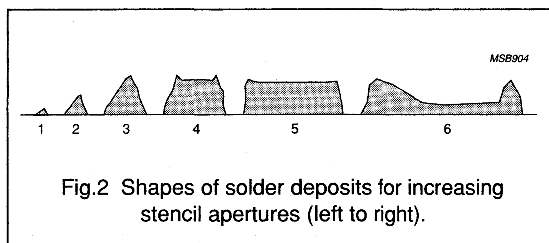


Fig.2 Shapes of solder deposits for increasing stencil apertures (left to right).

Ideally, the deposited solder paste should sit entirely on the solder land. The tolerated misplacement of solder paste with respect to the solder land is determined by the most critical component. The solder paste deposit must be deposited within 100 μm with respect to the solder land.

Furthermore, the tackiness (tack strength) of the solder paste must be sufficient to hold surface-mount devices on the PCB during assembly and during transport to the reflow oven. Tack strength depends on factors such as paste composition, drying conditions, placement pressure, dwell time and contact area. As a general rule, component placement should be within four hours after the paste printing process.

Squeegee

The squeegee can be either metal or rubber. A metal squeegee gives better overall results and so is recommended, however with step stencils, a rubber squeegee has to be used. The footprints given in this chapter were designed for application by both types of squeegee.

Stencil apertures

Stencil apertures can be made by either:

- Etching
- Laser cutting
- Electroforming.

Of the three methods, etching is less accurate as the deviation in aperture dimensions with respect to the target is relatively large (target is +50 μm at squeegee side and 0 μm at PCB side).

Laser-cut and electroformed stencils have smaller deviations in dimensions and are therefore more suitable for small and fine-pitch components (see Fig.3).

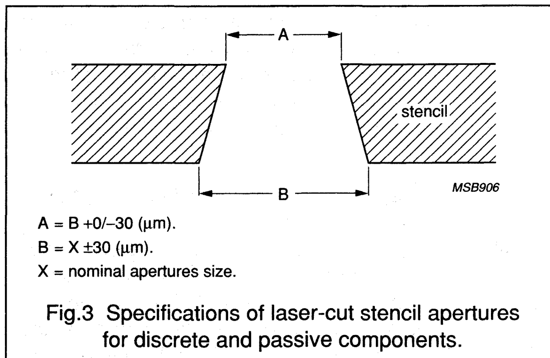


Fig.3 Specifications of laser-cut stencil apertures for discrete and passive components.

A useful method of controlling the stencil printing process during production is by monitoring the weight of solder paste on the board which may vary between 80% and 110% of the theoretical amount according to the target (designed) apertures. Smearing and clogging of a small aperture cannot be detected with this method.

Solder paste

Reflow soldering uses a paste consisting of small nodules of solder and a flux with binder, solvents and additives to control rheological properties. The flux in the solder paste can be rosin mildly activated or rosin activated.

The requirements of the solder paste are:

- Good rolling behaviour
- No slump during heat-up
- Low viscosity during printing
- High viscosity after printing
- Sufficient tackiness to hold the components
- Removal of oxides during reflow soldering.

Suitable solder paste types have the following compositions:

- Sn62Pb36Ag2
- Sn63Pb37
- Sn60Pb40.

COMPONENT PLACEMENT

The position of the component with respect to the solder lands is an important factor in the final result of the assembly process. A misaligned component can lead to unreliable joints, open circuits and/or bridges between leads.

The placement accuracy is defined as the maximum permissible deviation of the component outline or component leads, with respect to the actual position of the solder land pattern belonging to that component or component leads on the circuit board (see Fig.4).

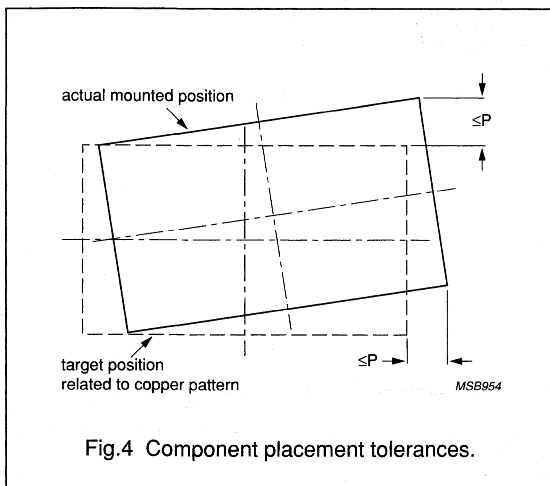


Fig.4 Component placement tolerances.

A maximum placement deviation (P) of 0.25 mm is used in these guidelines, which relates to the accuracy of a low-end placement machine. A higher placement accuracy is required for components with a fine pitch. This is given in the footprint description for the components concerned.

Besides the position in x- and y-directions, the z-position with respect to the solder paste, which is determined by the placement force, is also important. If the placement force is too high, solder paste will be squeezed out and solder balls or bridges will be formed. If the force is too low, physical contact will be insufficient, leads will not be soldered properly and the component may shift.

REFLOW SOLDERING

There are several methods available to provide the heat to reflow the solder paste, such as convection, hot belt, hot gas, vapour phase and resistance soldering. The preferred method is, however, convection reflow.

Convection reflow

With this method, the PCBs passes through an oven where it is preheated, reflow soldered and cooled (see Fig.5). If the heating rate of the board and components are similar, however, preheating is not necessary.

During the reflow soldering process, all parts of the board must be subjected to an accurate temperature/ time profile. Figure 5 shows a suitable profile framework for single-sided reflow soldering and the first side of double-sided print boards. It's important to note that this profile is for discrete semiconductor packages. The actual framework for the entire PCB could be smaller than the one shown, as other components on the board may have different process requirements.

Reflow soldering can be done in either air or a nitrogen atmosphere. If soldering in air, the temperature (T_p) must not exceed 240 °C on the first side of a double-sided print board with organic coated solder lands. This is because peak temperatures greater than 240 °C reduce the solderability of the lands on the second side to be soldered. This peak temperature can rise to 280 °C when soldering the second side with organic coated solder lands in air.

If soldering in a nitrogen atmosphere, a peak temperature of 280 °C is allowed for double-sided print boards or single-sided reflow soldering. Soldering in a nitrogen atmosphere results in smoother joint meniscus, smaller contact angles, and better wetting of the copper solder lands.

The profile can be achieved by correct combinations of conveyor speed and heater temperature. To check whether the profile is within specification, the coldest and hottest spots on the board have to be located.

To do this, you should dispense solder paste deposits regularly over the surface of a test board and on the component leads. Set the oven to a moderate temperature with maximum conveyor velocity and pass the test board through. If too many solder paste dots melt, lower the oven's temperature. Continue passing test boards through the oven, while lowering the speed of the belt in small steps.

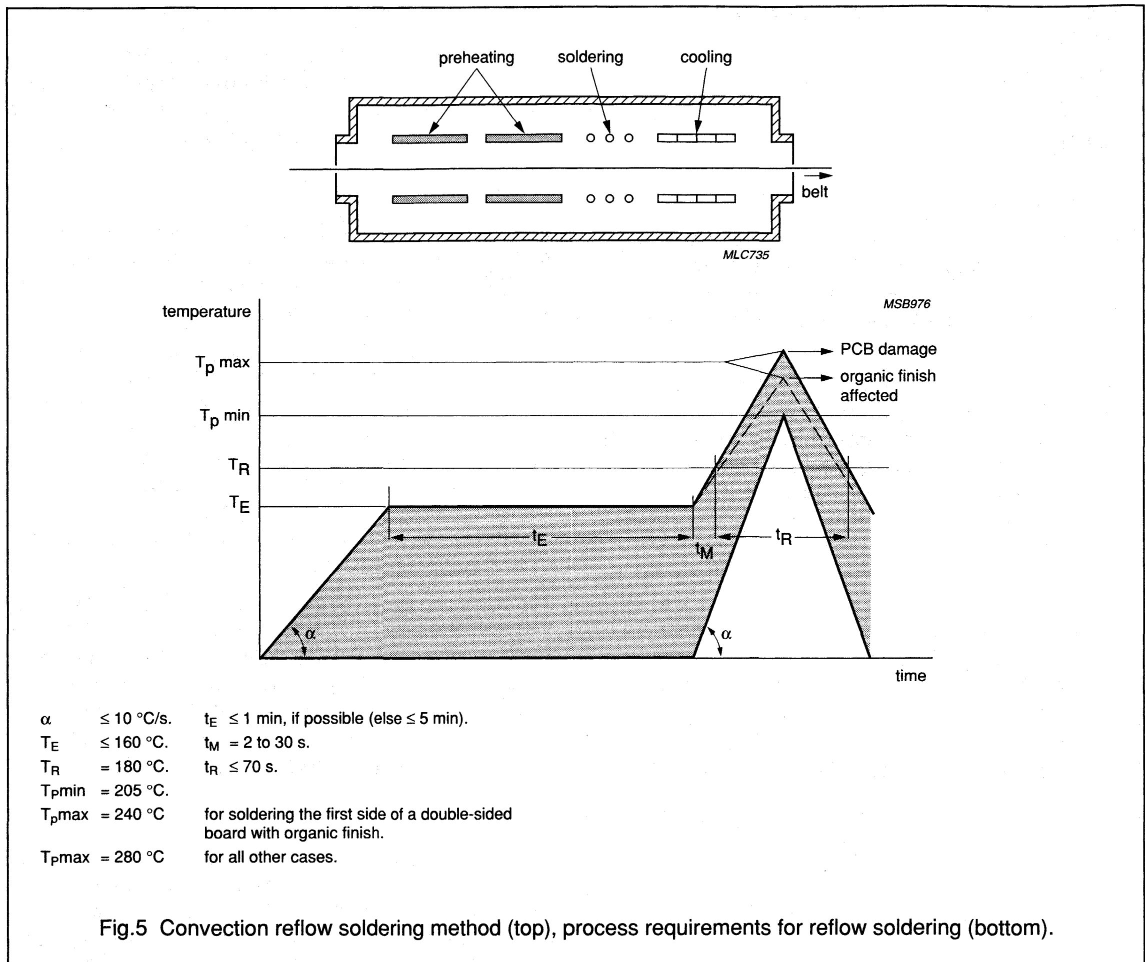


Fig.5 Convection reflow soldering method (top), process requirements for reflow soldering (bottom).

The deposit that melts first indicates the warmest location, the one that melts last indicates the coldest location. Paste dots not reflowed after two runs must be replaced by fresh dots. Thermocouples have to be mounted at the coldest and warmest location and temperature profiles measured.

Double-wave soldering process

There are four basic process steps for double-wave soldering, these are:

1. Applying adhesive
2. Component placement
3. Curing adhesive
4. Wave soldering process.

APPLYING ADHESIVE

To hold SMDs on the board during wave soldering, it is necessary to bond the component to the PCB with one or more adhesive dots. This is done either by dispensing, stencilling or pin transfer. Dispensing is currently the most popular technique. It is flexible and allows a controlled amount of adhesive to be applied at each position. Stencil printing and pin transfer are less flexible and are mainly used for mass production. The component-specific requirements for an adhesive dot are:

- Shape (volume) of the adhesive dot
- Number of dots per component
- Position of the dots.

Volume of adhesive

There must be enough adhesive to keep components in their correct positions while being transported to the curing oven. This means that the deposited adhesive must be higher than the gap between the component and the board surface. Nevertheless, there should not be too much deposit as it may smear onto the solder lands, where it can affect their solderability. The gap between a component and printed board depends on the geometry of the board and component (see Fig.6).

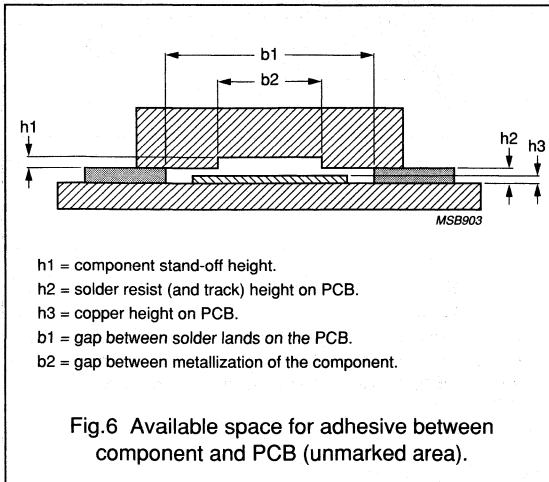


Fig.6 Available space for adhesive between component and PCB (unmarked area).

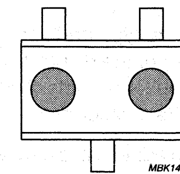
Table 1 gives guidelines for volumes of adhesive dots per package. The spreading in volumes should be within ±15%.

Table 1 Guidelines for volumes of adhesive dots

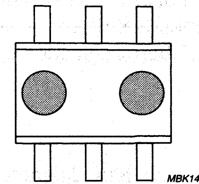
COMPONENT	NUMBER OF DOTS	VOLUME PER DOT (mm^3)
SC-70 (SOT323)	2	0.045
SC-88 (SOT363)	2	0.045
SOT23	2	0.06
SOT89	2	0.3
SOT223	2	0.70

Number, position and volume of dots per component

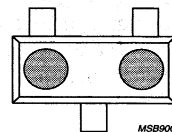
Figure 7 shows the recommended positions and numbers of adhesive dots for a variety of packages. SOT89 and SOT223 packages require much larger adhesive dots compared with those for other components.



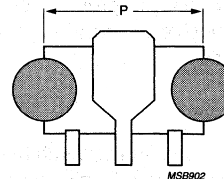
a. SC-70 (SOT323).



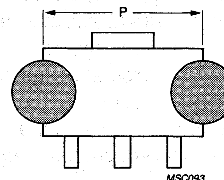
b. SC-88 (SOT363).



c. SOT23.



d. SOT89 (P = 4.4 mm).



e. SOT223 (P = 6.0 mm).

For optimum power dissipation, the SOT89 requires a good thermal contact (i.e. good solder joint) between the package and the solder land. During wave-soldering, however, flux may not always reach the total soldering area beneath the component body, which in turn can lead to an incomplete solder joint. If the SOT89 is double-wave soldered, therefore, power derating must be applied.

Fig.7 Position of adhesive dots. Pitch between two small dots is 1.0 mm.

Nozzle outlet diameter

Depending on adhesive type and component size, the nozzle outlet diameter of the dispenser can vary between 0.6 and 0.7 mm for the larger dots, and between 0.3 and 0.5 mm for the smaller dots.

As the rheology of the adhesive is temperature dependent, the temperature in the nozzle must be carefully controlled before dispensing. The required temperature depends on the adhesive type, but is usually between 26 °C and 32 °C to maintain the adhesive's rheology within specification during dispensing. Thermally curing epoxy adhesives are normally used.

Adhesives

Beside the nozzle diameters, different adhesive types are also used for different component sizes.
Small components can be secured during assembly and wave soldering with a thin (low green strength) adhesive, which can be dispensed at high speeds. For larger components (such as QFP and SO packages), a higher green strength adhesive is required.

COMPONENT PLACEMENT

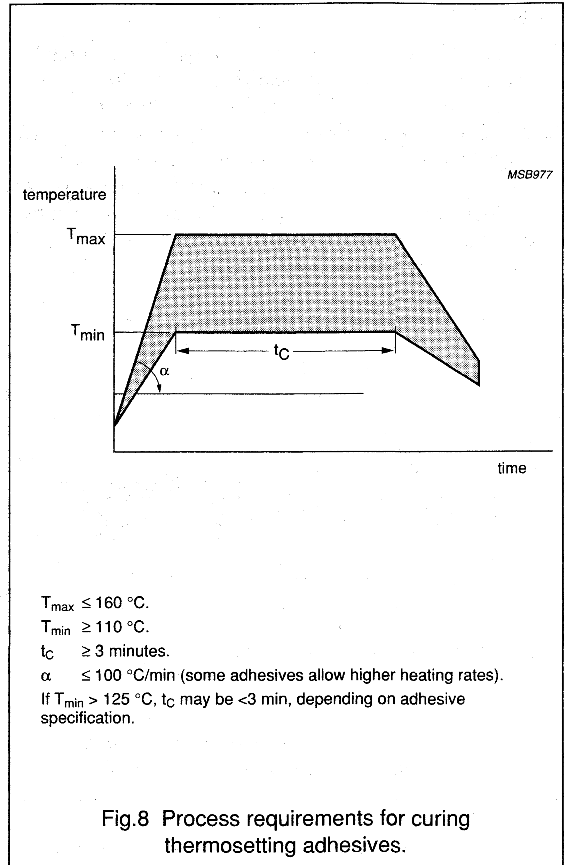
Positioning components on the PCB is similar in practice to that of reflow soldering. To prevent component shift and smearing of the adhesive, board support is important while placing components.

CURING THE ADHESIVE

To provide sufficient bonding strength between component and board, the adhesive must be properly cured. Figure 8 gives general process requirements for curing most thermosetting epoxy adhesives with latent hardeners. The temperature profile of all adhesive dots on the PCB must be within this framework. It's important to note that this profile is for discrete semiconductor packages. The actual framework for the entire PCB could be smaller than the one shown, as other components on the board may have different process requirements.

To check whether the profile is within specification, the temperature of coldest and hottest spots must be measured. The coldest spot is usually under the largest package: the hottest spot is usually under the smallest package.

The adhesive can be cured either by infrared or hot-air convection.



T_{max} ≤ 160 °C.
T_{min} ≥ 110 °C.
t_C ≥ 3 minutes.
α ≤ 100 °C/min (some adhesives allow higher heating rates).
If T_{min} > 125 °C, t_C may be <3 min, depending on adhesive specification.

Fig.8 Process requirements for curing thermosetting adhesives.

Bonding strength

The bonding strength of glued components on the board can be checked by measuring the torque force. For small components the requirements are given in Table 2.
No values are specified for larger packages.

Table 2 Bonding strength requirements

COMPONENT	MINIMUM BONDING STRENGTH (cNcm)	TARGET BONDING STRENGTH (cNcm)
SC-70 (SOT323) SC-88 (SOT363)	110	250
SOT23	150	250

WAVE SOLDERING PROCESS

After applying adhesive, placing the component on the PCB and curing, the PCB can be wave soldered. The wave soldering process is basically built up from three sub-processes. These are:

1. Fluxing
2. Preheating
3. (Double) wave soldering.

Although listed here as sub-process they are in practice combined in one machine. All are served by one transport mechanism, which guides the PCBs at an incline through the soldering machine. It's important to note that the PCB must be loaded into the machine so that the SMDs on the board come into direct contact with the solder wave (see Fig.9).

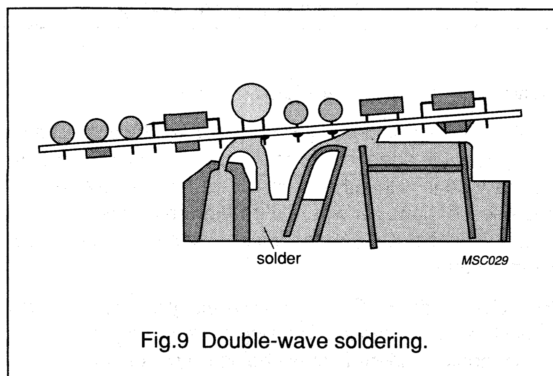


Fig.9 Double-wave soldering.

In principle, two different systems of PCB transports are available for wave soldering:

- Carrier transport

  PCBs are mounted on a soldering carrier, which moves through the soldering machine, taking it from one sub-process to the next. The advantage of carrier mounting is that the board is fixed and warpage during soldering is reduced.

- Carrierless transport

  PCBs are guided through the soldering machine by a chain with grips. This method is more convenient for mass production.

Fluxing

Fluxing is necessary to promote wetting both of the PCB and the mounted components. This ensures a good and even solder joint.

During the fluxing process, the solder side of the PCB (including the components) are covered with a thin layer of solder flux, which can be applied to the PCB either by spraying or as a foam. Although several types of solder flux are available for this purpose, they can be categorized into three main groups:

- Non-activated flux (e.g. rosin-based fluxes)
- Mildly activated flux (e.g. rosin-based or synthetic fluxes)
- Highly activated flux (e.g. water-soluble fluxes).

The choice for a particular flux type depends mainly on the products to be soldered.

Although there is always some flux residue left on the PCB after soldering, it's not always necessary to wash the boards to remove it. Whether to clean the board can depend on:

- The type of flux used (highly activated fluxes are corrosive and so should always be removed).
- The required appearance of the board after soldering.
- Customer requirements.

Preheating

After the flux is applied, the PCB needs to be preheated. This serves several purposes: it evaporates the flux solvents, it accelerates the activity of the flux and it heats the PCB and components to reduce thermal shock.

The required pre-heat temperature depends on the type of flux used. For example, the more common low-residue fluxes require a pre-heat temperature of 120 °C (measured on the wave solder side of the PCB).

(Double) wave soldering

The PCB first passes over a highly intensive (jet) solder wave with a carefully controlled constant height. This ensures good contact with the PCB, the edges of SMDs and the leads of components near to high non-wetted bodies. The greater the board's immersion depth into this first wave, the fewer joints will be missed.

If the PCB is carrier mounted, the first wave's height, and thus the board's immersion depth, can be greater. Carrierless soldering is more convenient for mass production, but the height of the wave must be lower to avoid solder overflowing to the top side of the board. The height of the jet wave is given in Table 3 along with an indication of soldering process window. This information is based on a 1.6 mm thick PCB.

Table 3 Process ranges for carrierless and carrier double wave soldering

	CARRIERLESS	CARRIER
Preheat temperature of board at wave solder side (°C)	120 ±10	
Heating rate preheating (°C/s)	$\Delta T/\Delta t \leq 3$	
First (jet) wave: wave height with respect to bottom side of board (mm)	1.6 +0.5/−0	3.0 +0.5/−0
Second (laminar) wave (double sided overflow): height with respect to underside of the board (mm) relative stream velocity with respect to the board	 0.8 +0.5/−0 0	
Solder temperature (°C)	250 ±3	
Contact times (s): first (jet) wave second (laminar) wave	 0.5 +0.5/−0 2.0 ±0.2 (plain holes); 2.5 ±0.2 (plated holes)	
PCB transport angle (°)	7 ±0.5	
Solder alloys	Sn60Pb40; Sn60Pb38Bi2	

The second, smoother laminar solder wave completes formation of the solder fillet, giving an optimal soldered connection between component and PCB. It also reduces the possibility of solder bridging by taking up excessive solder.

To reduce lead/tin oxides and possibly other solder imperfection forming during soldering, the complete wave configuration can be encapsulated by an inert atmosphere such as nitrogen.

Hand soldering microminiature components

It is possible to solder microminiature components with a light-weight hand-held soldering iron, but this method has obvious drawbacks and should be restricted to laboratory use and/or incidental repairs on production circuits:

- Hand-soldering is time-consuming and therefore expensive
- The component cannot be positioned accurately and the connecting tags may come into contact with the substrate and damage it
- There is a risk of breaking the substrate and internal connections in the component could be damaged
- The component package could be damaged by the iron.

Assessment of soldered joint quality

The quality of a soldered joint is assessed by inspecting the shape and appearance of the joint. This inspection is normally done with either a low-powered magnifier or microscope, however where ultra-high reliability is required, video, X-ray or laser inspection equipment may be considered.

Both sides of the PCB should be carefully examined: there should be no misaligned, missing or damaged components, soldered joints should be clean and have a similar appearance, there should be no solder bridging or residue, and the PCB should be assessed for general cleanliness.

Unlike leaded component joints where the lead also provides added mechanical strength, the SMD relies on the quality of the soldering for both electrical and mechanical integrity. It is therefore necessary that the inspector is trained to make a visual assessment with regard to long-term reliability.

Criteria used to assess the quality of an SMD solder joint include:

- Correct position of the component on the solder lands
- Good wetting of the surfaces
- Correct amount of solder
- A sound, smooth joint surface.

POSITIONING

If a lead projects over the solder land too far an unreliable joint is obtained. Figures 10 to 12 show the maximum shift allowed for various components. The dimensions of these solder lands guarantee that, in the statistically extreme situation, a reliable soldered joint can be made.

GOOD WETTING

This produces an even flow of solder over the surface land and component lead, and thinning towards the edges of the joint. The metallic interaction that takes place during soldering should give a smooth, unbroken, adherent layer of solder on the joint.

CORRECT AMOUNT OF SOLDER

A good soldered joint should have neither too much nor too little solder: there should be enough solder to ensure electrical and mechanical integrity, but not so much that it causes solder bridging.

SOUND, SMOOTH JOINT SURFACE

The surface of the solder should be smooth and continuous. Small irregularities on the solder surface are acceptable, but cracks are unacceptable.

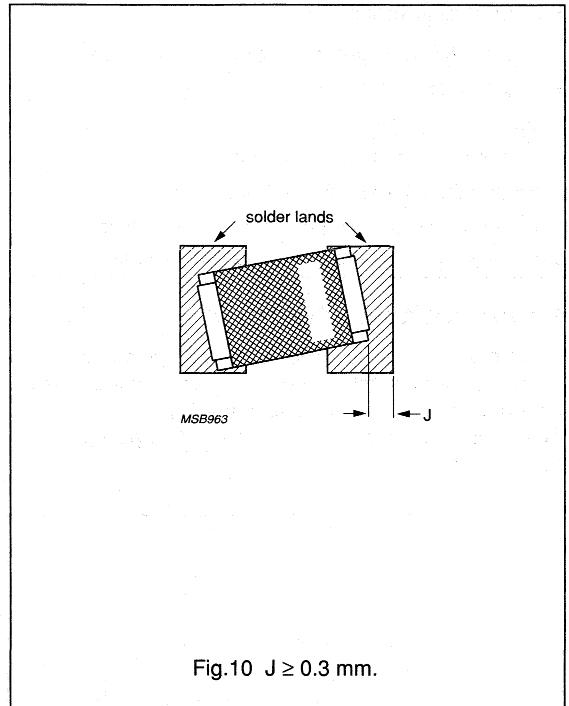


Fig.10 J ≥ 0.3 mm.

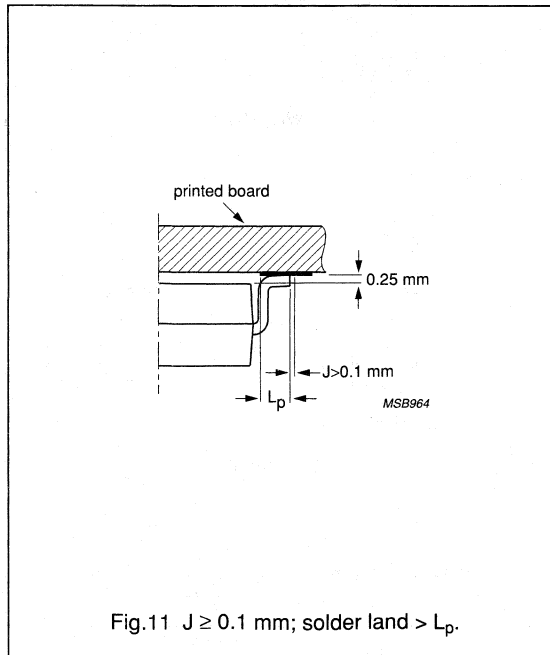


Fig.11 J ≥ 0.1 mm; solder land > L_p.

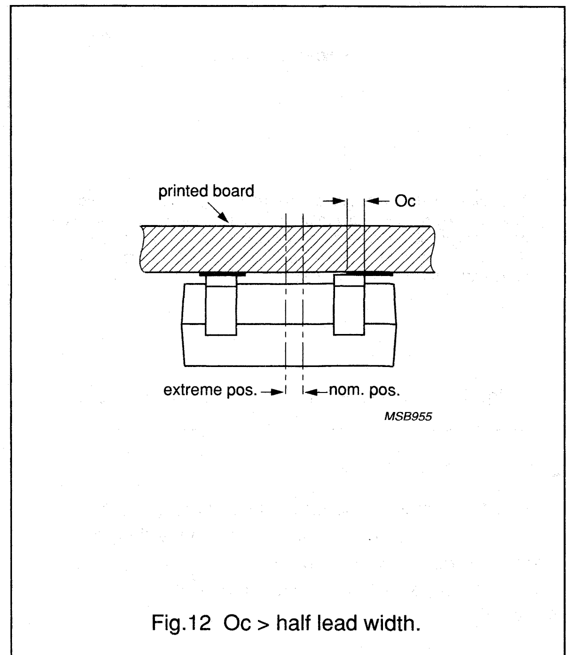


Fig.12 Oc > half lead width.

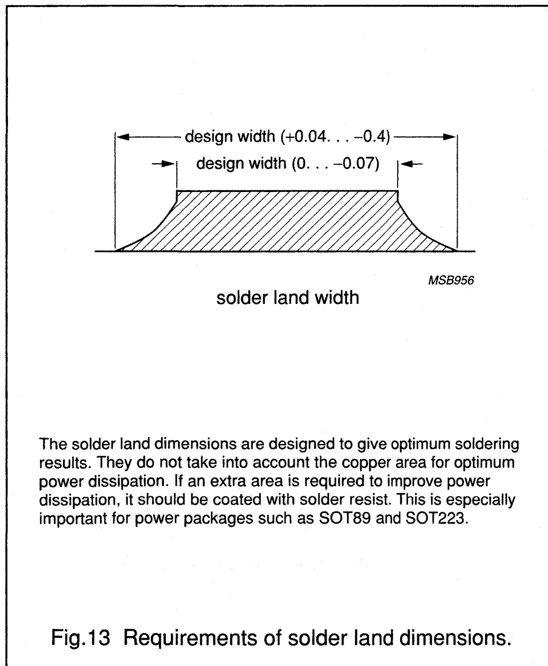
Footprint definitions

A typical SMD footprint, is composed of:

- Solder lands (conductive pattern)
- Solder resist pattern
- Occupied area of the component
- Solder paste pattern (for reflow soldering only)
- Area underneath the SMD available for tracks
- Component orientation during wave soldering.

SOLDER LANDS (CONDUCTIVE PATTERN)

The dimensions of the solder lands given in these guidelines are the actual dimensions of the conductive pattern on the printed board (see Fig.13).
These dimensions are more crucial for fine-pitch components.



The solder land dimensions are designed to give optimum soldering results. They do not take into account the copper area for optimum power dissipation. If an extra area is required to improve power dissipation, it should be coated with solder resist. This is especially important for power packages such as SOT89 and SOT223.

Fig.13 Requirements of solder land dimensions.

SOLDER RESIST PATTERN

The solder resist on the circuit board prevents short circuits during soldering, increases the insulation resistance between adjacent circuit details and stops solder flowing away from solder lands during reflow soldering.

In contrast to the tracks, which must be entirely covered, solder lands must be free of solder resist. Because of this, the cut-outs in the solder resist pattern should be at least 0.15 mm or 0.3 mm larger than the relevant solder lands (for a photo-defined and screen printed solder resist pattern respectively). The solder resist cut-outs given with the footprints in these guidelines are sketched and their dimensions can be calculated by using the above rule. Consult your printed board supplier for agreement with these solder resist cut-outs.

OCCUPIED AREA OF THE COMPONENT

A minimum spacing between components is necessary to avoid component placement problems, short circuits during wave or reflow soldering and dry solder joints during wave soldering caused by non-wettable component bodies. These problems can be avoided by placing the components so the occupied areas do not overlap (see Fig.14).

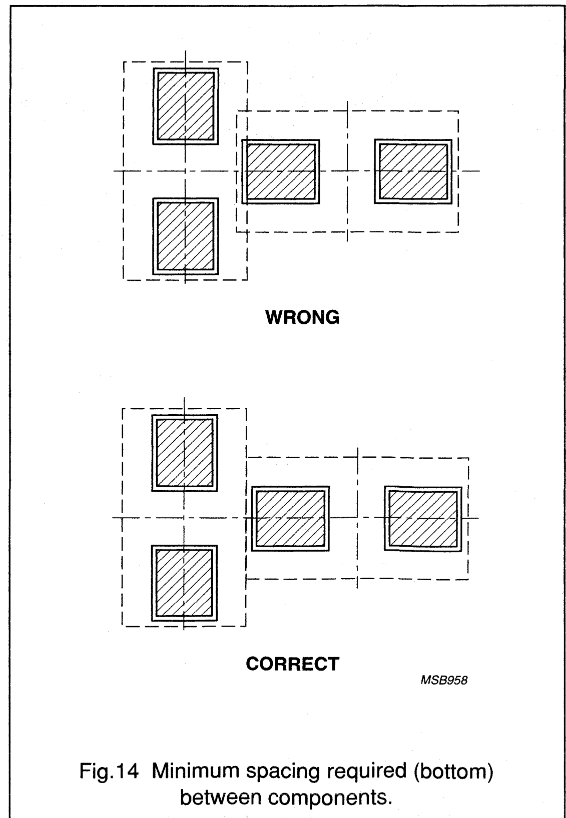


Fig.14 Minimum spacing required (bottom) between components.

SOLDER PASTE PATTERN

It is important to use a solder paste printer which is optical aligned with the PCBs copper pattern for the reflow footprints presented here. This is because, for these footprints, the solder paste deposit must be within a 0.1 mm tolerance with respect to the copper pattern.

To ensure the right amount of solder for each solder joint, the stencil apertures must be equal to the solder paste areas given by the footprints.

AREA AVAILABLE FOR TRACKS (CONDUCTIVE PATTERN)

Tracks underneath leadless SMDs must be covered with solder resist. However, as solder resist can sometimes be thin or have pin holes at the edges of tracks (especially when applied by screen printing), an additional clearance for tracks with respect to the actual metallization position of the mounted component should be taken into account (see Fig.15).

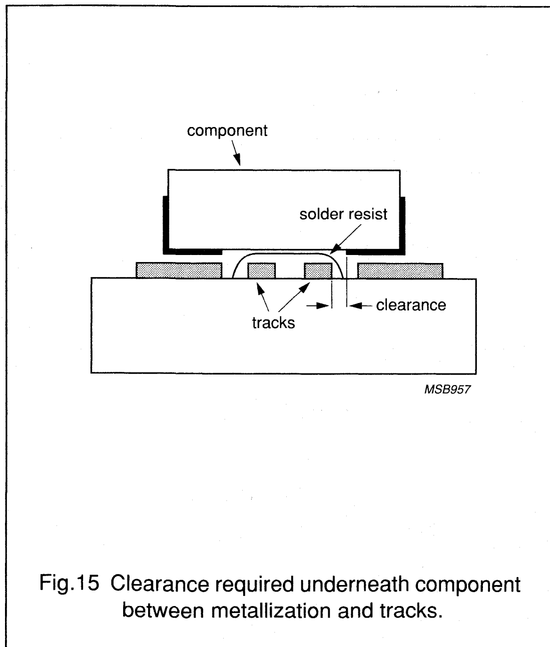


Fig.15 Clearance required underneath component between metallization and tracks.

For components that need the additional clearance, the footprints on the following pages give the maximum space for tracks not connected to the solder lands (clearance ≥ 0.1 mm), for low-voltage applications.
The number of tracks in this space is determined by the specified line resolution of the printed board.

COMPONENT ORIENTATION DURING WAVE SOLDERING

Where applicable, footprints for wave soldering are given with the transport direction of the PCB. This is given as either a 'preferred transport direction during soldering' or 'transport direction during soldering'.

Components with small terminals and non-wettable bodies, have a smaller risk of dry joints, especially when using carrierless soldering as the components are placed according to the 'preferred orientation'.

Components have no orientation preference for reflow soldering.

Recommended footprints

The recommended footprints for our discrete semiconductor packages are given on the following pages. For their dimensional outline drawings, see the 'Package outlines' section in this book.

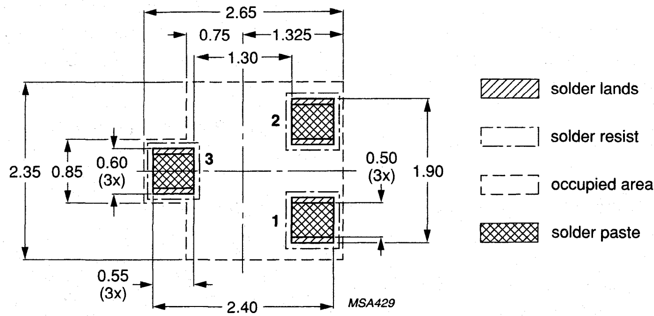


Fig.16 Reflow soldering footprint for SC-70 (SOT323).

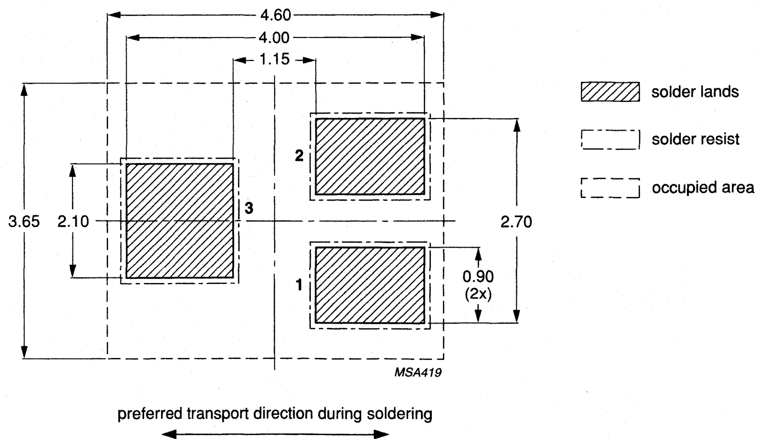


Fig.17 Wave soldering footprint for SC-70 (SOT323).

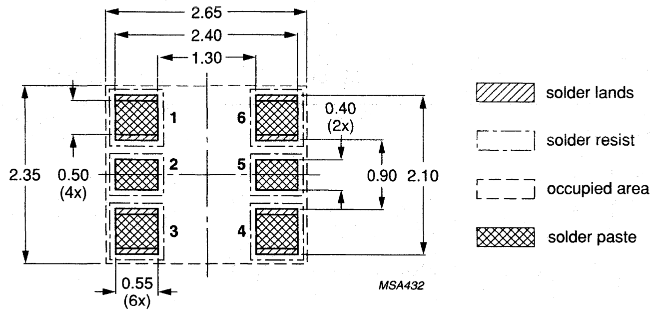


Fig.18 Reflow soldering footprint for SC-88 (SOT363).

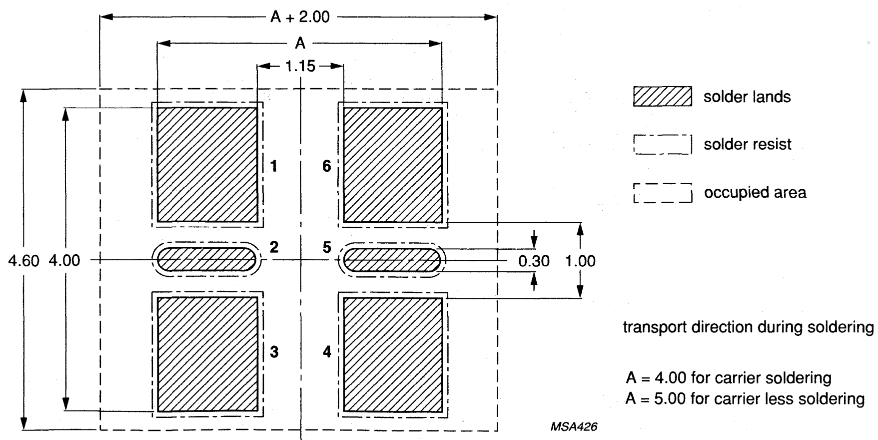


Fig.19 Wave soldering footprint for SC-88 (SOT363).

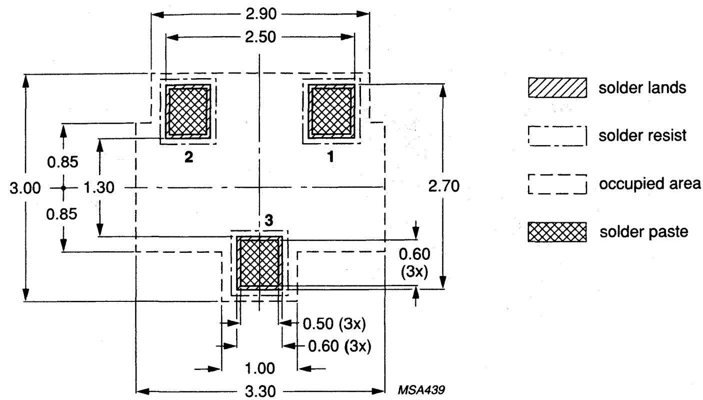


Fig.20 Reflow soldering footprint for SOT23.

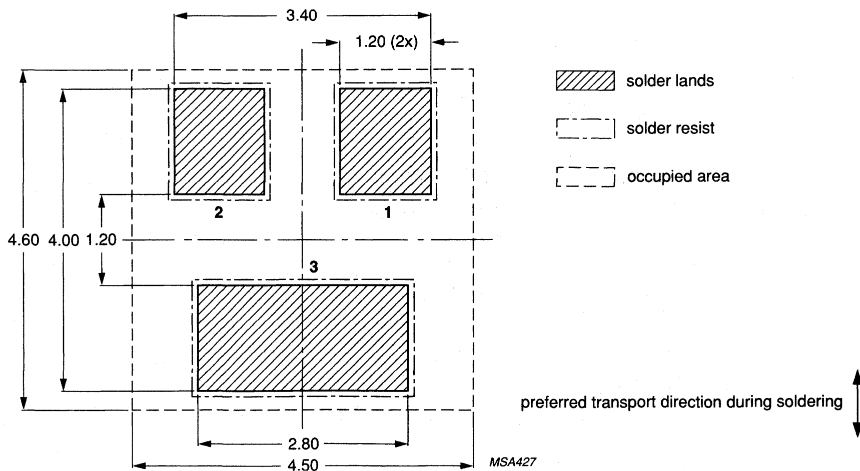


Fig.21 Wave soldering footprint for SOT23.

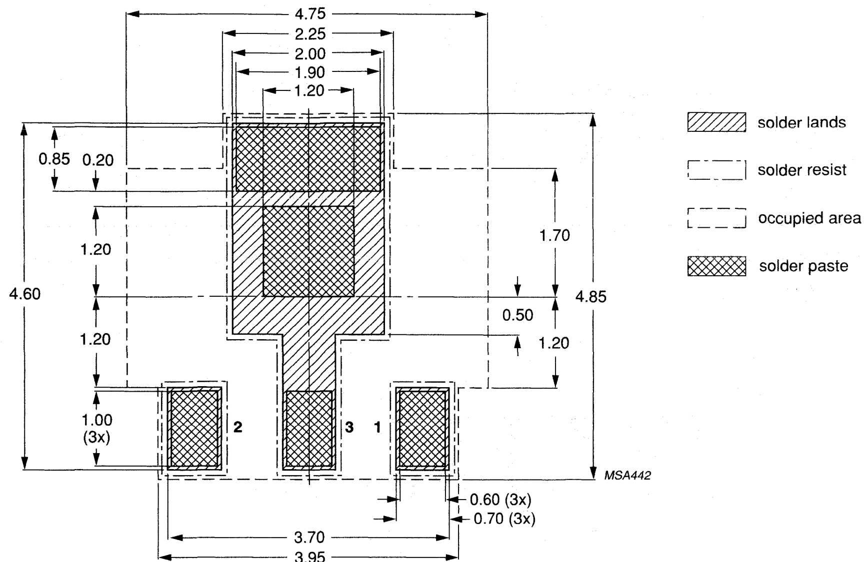
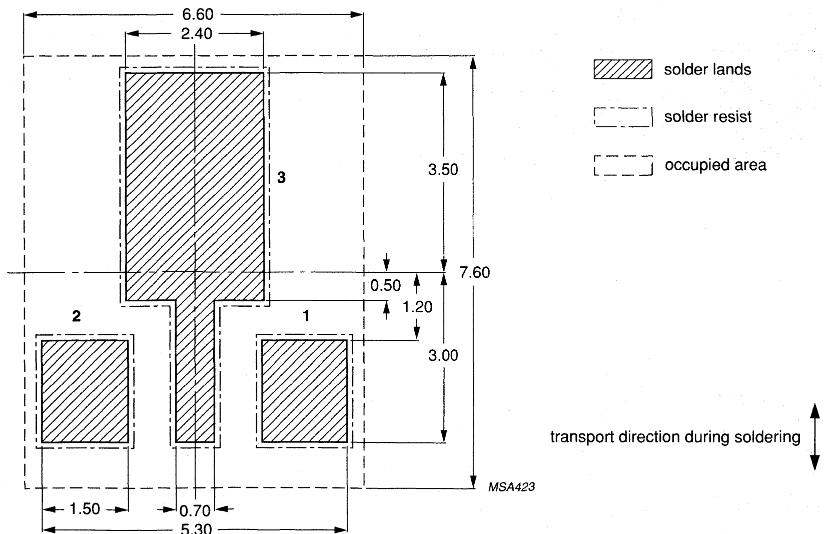


Fig.22 Reflow soldering footprint for SOT89.



Not recommended for wave soldering (see Fig.7).

Fig.23 Wave soldering footprint for SOT89.

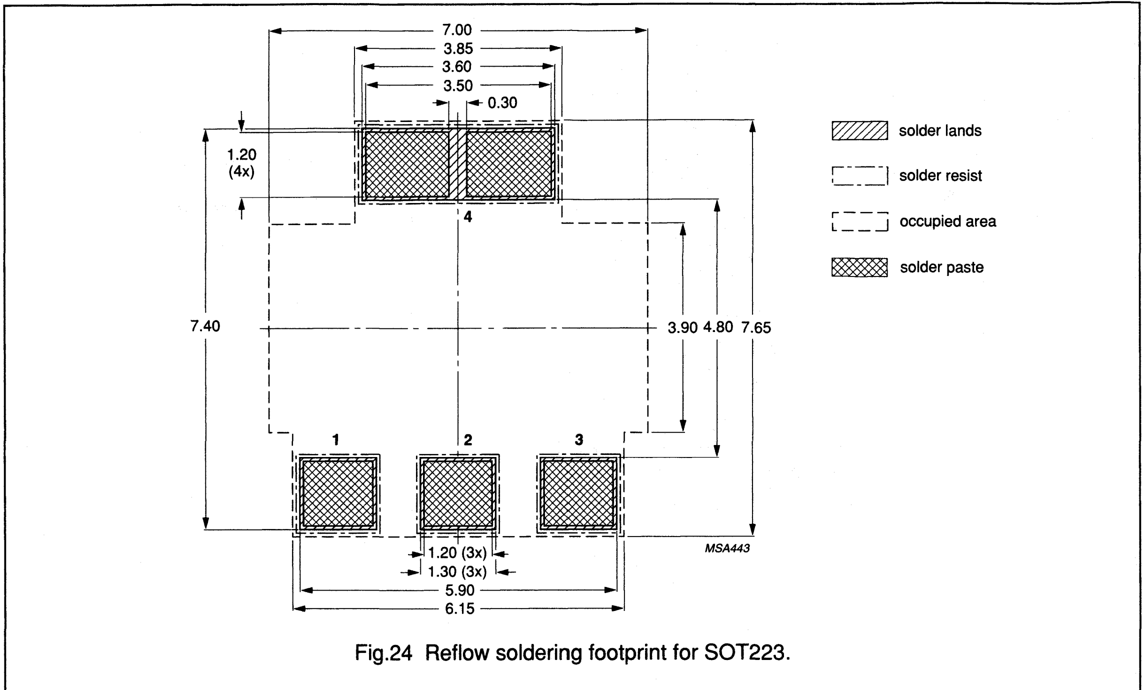


Fig.24 Reflow soldering footprint for SOT223.

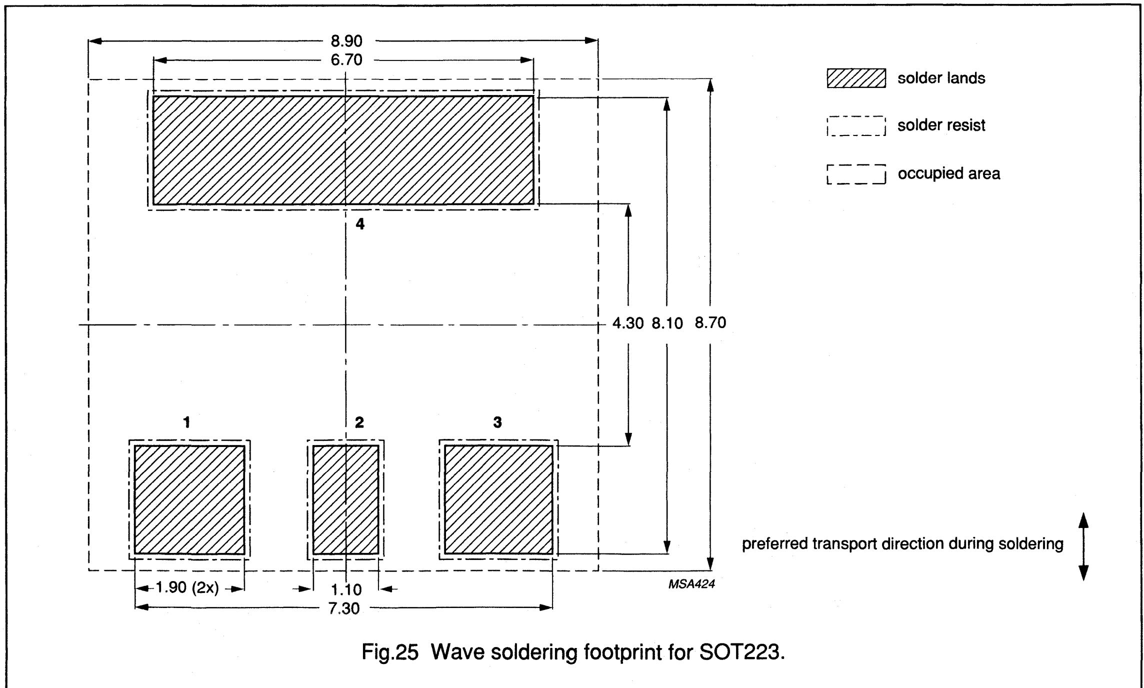
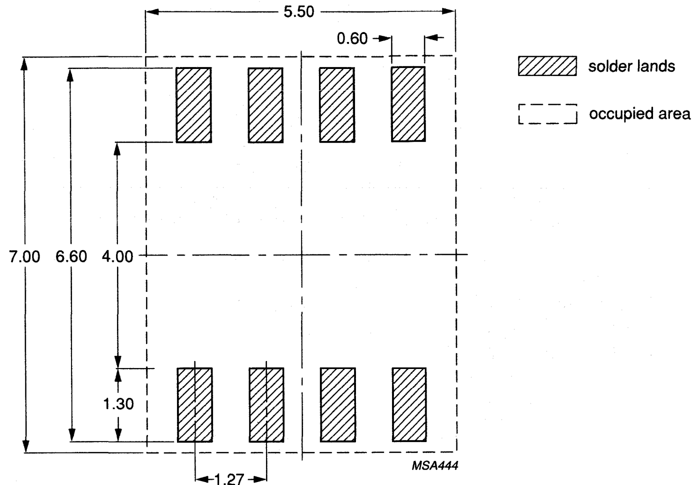
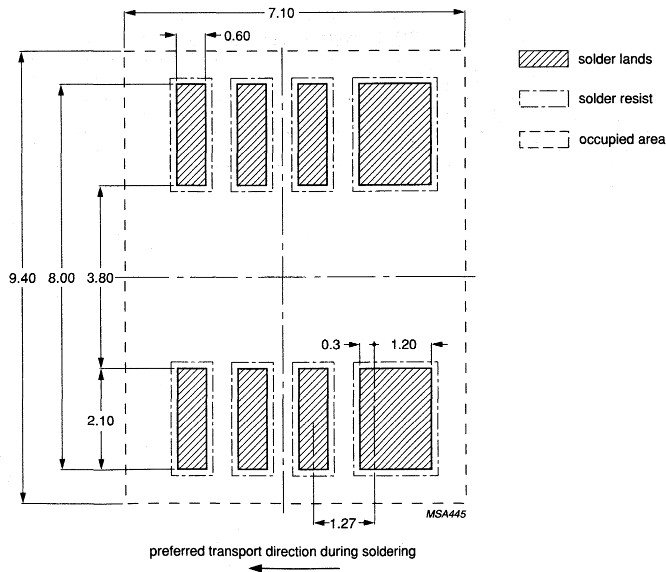


Fig.25 Wave soldering footprint for SOT223.



Placement accuracy: ±0.25 mm.

Fig.26 Reflow soldering footprint for SO8 (SOT96-1)



Placement accuracy: ±0.25 mm.

Fig.27 Wave soldering footprint for SO8 (SOT96-1)

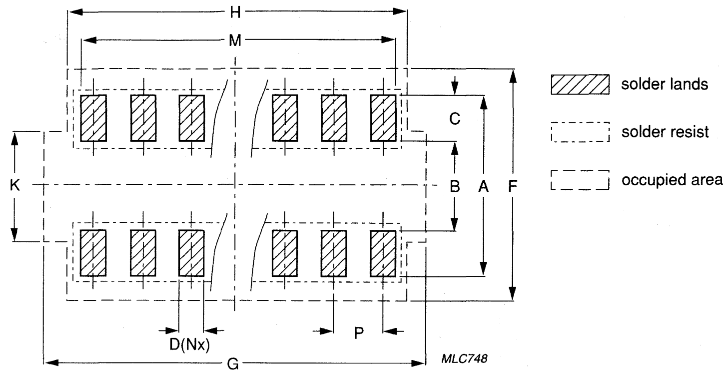


Fig.28 Reflow soldering footprint for SSOP16 (SOT338-1) and SSOP24 (SOT340-1).

Footprint dimensions for reflow soldering

PACKAGE NAME	PHILIPS CODE	N	FOOTPRINT DIMENSIONS IN mm										PLACEMENT ACCURACY
			P	A	B	C	D	F	G	H	K	M	
SSOP16	SOT338-1	16	0.65	8.10	5.70	1.20	0.40	8.35	6.50	5.20	5.55	4.95	±0.15
SSOP24	SOT340-1	24	0.65	8.10	5.90	1.10	0.40	8.35	8.50	7.80	5.55	7.55	±0.15

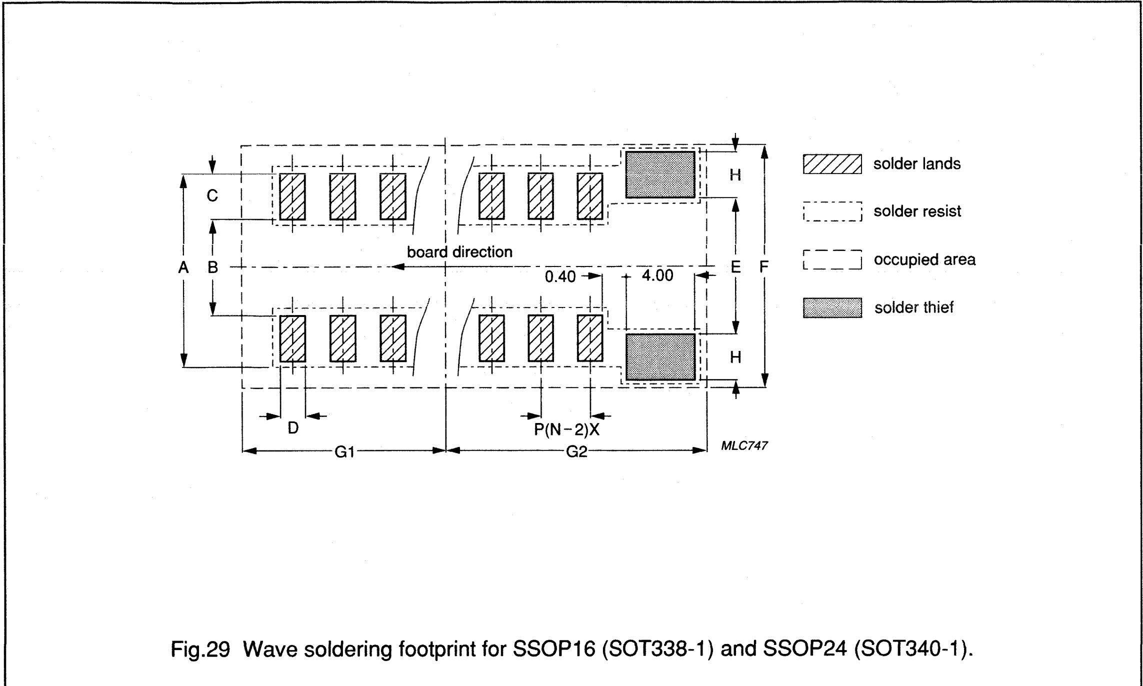


Fig.29 Wave soldering footprint for SSOP16 (SOT338-1) and SSOP24 (SOT340-1).

Footprint dimensions for wave soldering

PACKAGE NAME	PHILIPS CODE	N	FOOTPRINT DIMENSIONS IN mm										PLACEMENT ACCURACY
			P	A	B	C	D	E	F	G1	G2	H	
SSOP16	SOT338-1	16	0.65	9.15	5.35	1.90	0.30	6.15	10.65	4.25	7.075	2.00	±0.10
SSOP24	SOT340-1	24	0.65	9.15	5.55	1.80	0.30	6.30	10.80	5.25	8.375	2.00	±0.10

PACKING AND PACKING QUANTITIES

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SCOPE

This chapter covers packing and packing quantity details for surface-mount and leaded devices in the following packages:

Table 1 Survey of packages

PACKAGE	
SURFACE-MOUNT	**THROUGH-HOLE**
SC -70 (SOT323)	TO-92 (SOT54)
SC-88 (SOT363)	TO-92 var. (SOT54 var.)
SOT23	
SOT89	
SOT223	
SO8 (SOT96-1)	
SSOP16 (SOT338-1)	
SSOP24 (SOT340-1)	

SURFACE-MOUNT DEVICES

Tape and reel packing for surface-mount devices meets the feed requirements for automatic pick and place equipment (packing conforms to IEC publication 286-3). Tape is an ideal shipping container making handling easy and providing secure blister cavities in which the devices are sealed with peel-off cover tape.

Tape specification

Tape dimensions are specified in Tables 3 and 4 and in Figures 1 through 4 for 8, 12 and 16 mm tape.

Table 2 Carrier tape widths

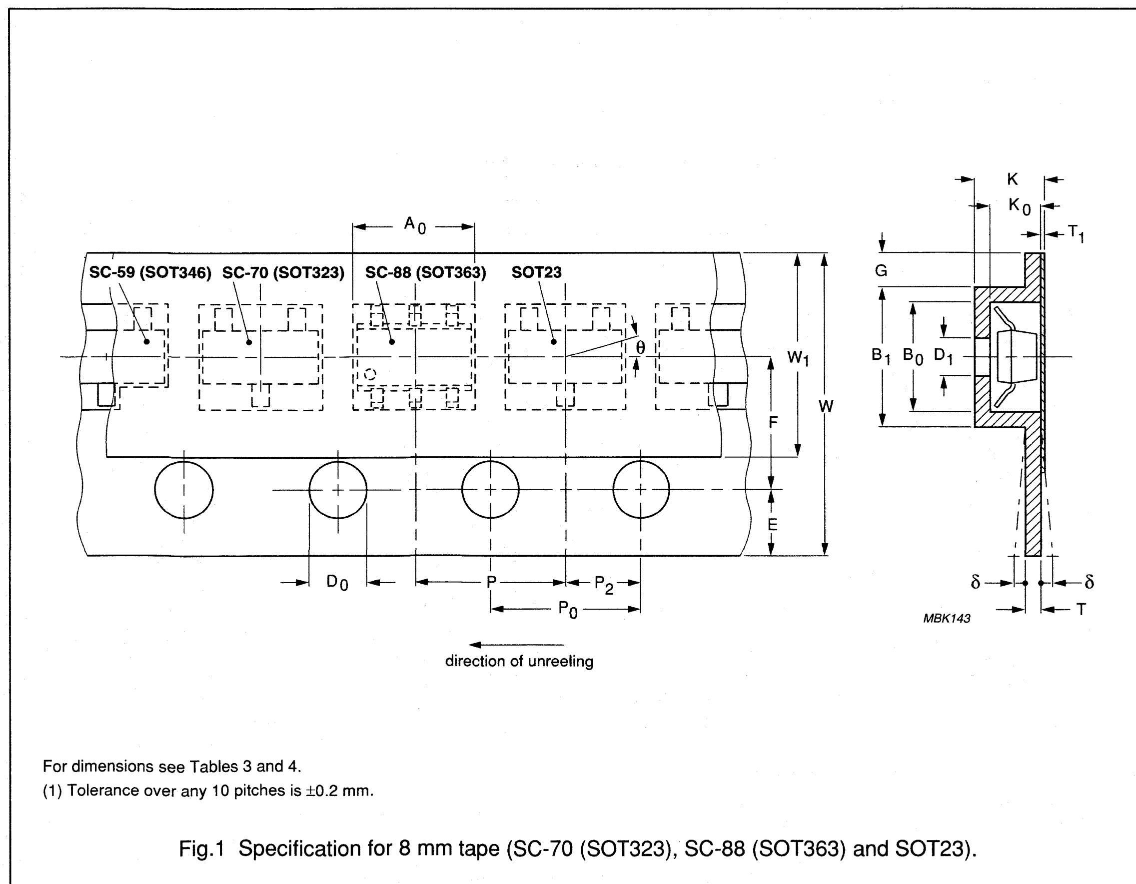
8 mm	12 mm	16 mm
SC-70 (SOT323)	SOT89	SSOP16 (SOT338-1)
SC-88 (SOT363)	SOT223	SSOP24 (SOT340-1)
SOT23	SO8 (SOT96-1)	

Table 3 Variable tape dimensions

PACKAGE	SYMBOL						
	W (mm)	**F (mm)**	**P (mm)**	**D_1 (mm)**	**A_0 (mm)**	**B_0 (mm)**	**K_0 (mm)**
SC-70 (SOT323)	8.0	3.5	4.0	1.0	2.4	2.4	1.2
SC-88 (SOT363)	8.0	3.5	4.0	1.0	2.4	2.4	1.2
SOT23	8.0	3.5	4.0	1.0	3.1	2.6	1.3
SOT89	12.0	5.5	8.0	1.5	4.3	4.6	1.6
SOT223	12.0	5.5	8.0	1.5	7.0	7.4	1.9
SO8 (SOT96-1)	12.0	5.5	8.0	1.5	6.7	5.4	1.8
Tolerance	±0.2	±0.05	±0.1	min.	±0.1	±0.1	±0.1
SSOP16 (SOT338-1)	16.0	7.5	12.0	1.5	8.2	6.6	2.5
SSOP24 (SOT340-1)	16.0	7.5	12.0	1.5	8.2	8.8	2.5
Tolerance	±0.3	±0.1	±0.1	min.	±0.1	±0.1	±0.1

Table 4 Fixed tape dimensions

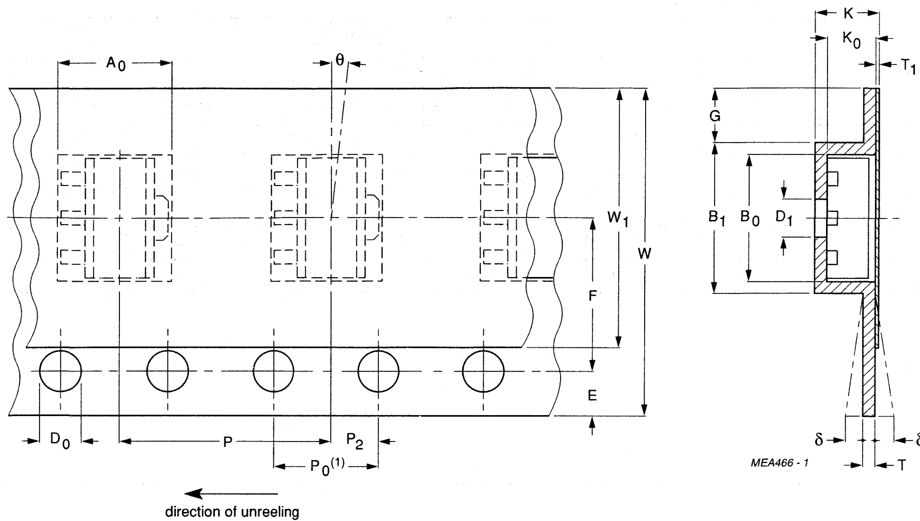
PACKAGE	SYMBOL							
	E (mm)	D_0 (mm)	P_0 (mm)	P_2 (mm)	G (mm)	T (mm)	δ (mm)	θ (deg)
8 and 12 mm tape	1.75	1.5	4.0	2.0	0.75	0.4	0.3	15
Tolerance	±0.1	−0/+0.1	±0.1	±0.05	min.	max.	max.	max.
16 mm tape	1.75	1.5	4.0	2.0	0.75	0.4	0.3	10
Tolerance	±0.1	−0/+0.1	±0.1	±0.1	min.	max.	max.	max.



For dimensions see Tables 3 and 4.

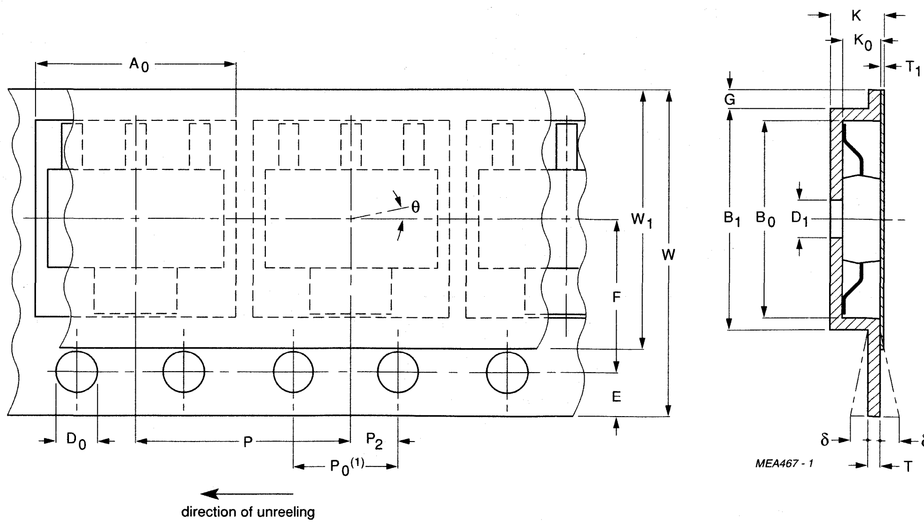
(1) Tolerance over any 10 pitches is ±0.2 mm.

Fig.1 Specification for 8 mm tape (SC-70 (SOT323), SC-88 (SOT363) and SOT23).



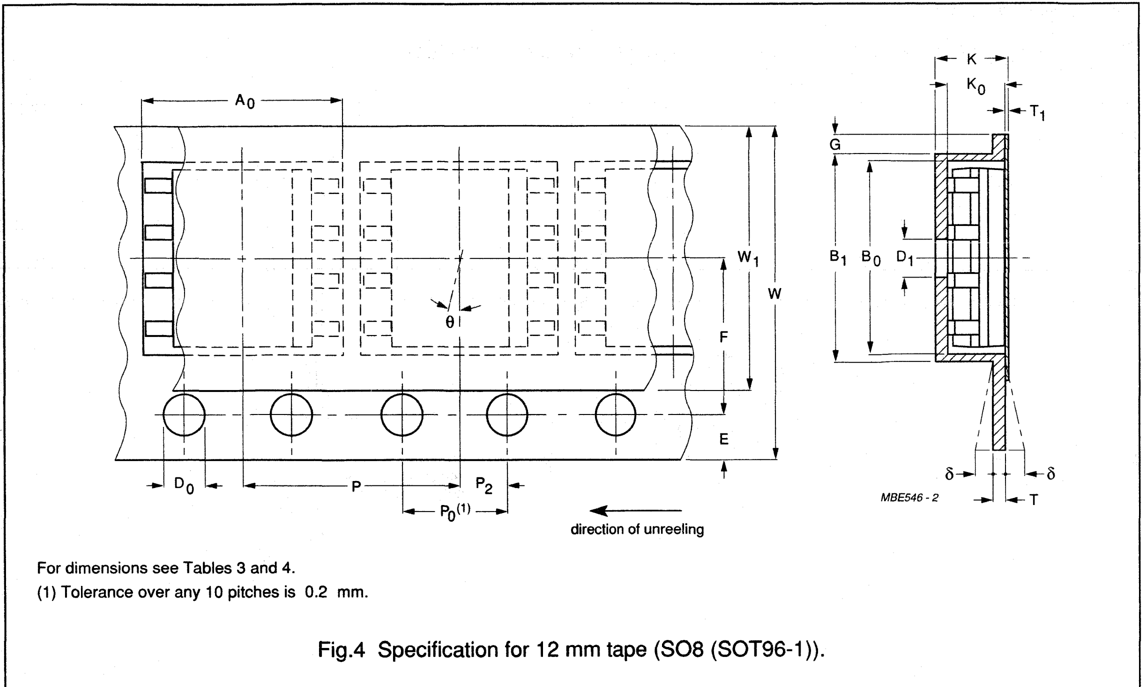
For dimensions see Tables 3 and 4.
(1) Tolerance over any 10 pitches is 0.2 mm.

Fig.2 Specification for 12 mm tape (SOT89).



For dimensions see Tables 3 and 4.
(1) Tolerance over any 10 pitches is 0.2 mm.

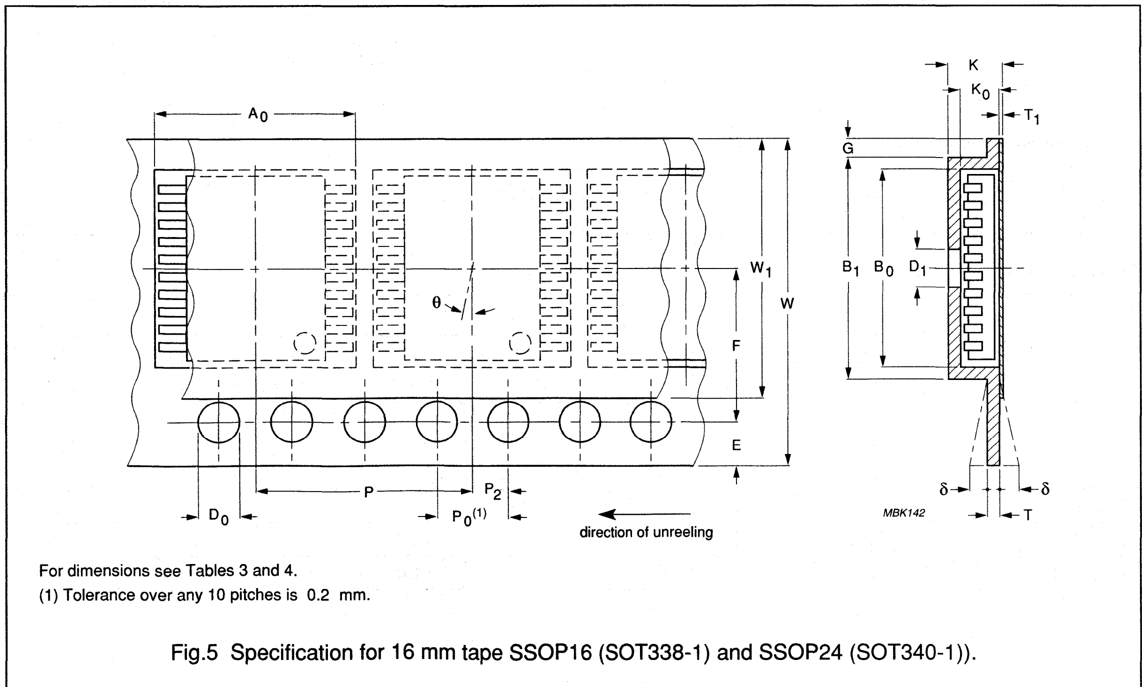
Fig.3 Specification for 12 mm tape (SOT223).



For dimensions see Tables 3 and 4.

(1) Tolerance over any 10 pitches is 0.2 mm.

Fig.4 Specification for 12 mm tape (SO8 (SOT96-1)).



For dimensions see Tables 3 and 4.

(1) Tolerance over any 10 pitches is 0.2 mm.

Fig.5 Specification for 16 mm tape SSOP16 (SOT338-1) and SSOP24 (SOT340-1)).

Reel specification

Reel dimensions are specified in Fig.6 and Table 5 for 8, 12 and 16 mm tape.

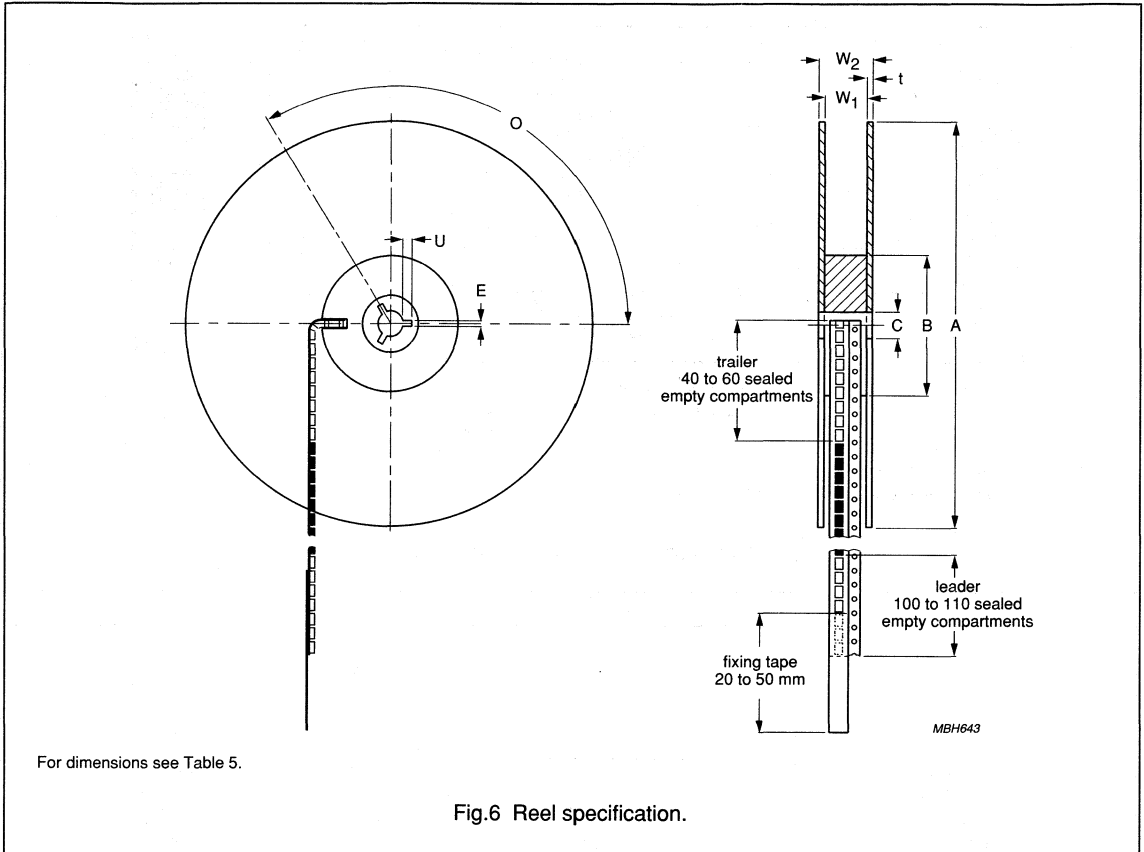


Fig.6 Reel specification.

Table 5 Reel dimensions

TAPE WIDTH	SYMBOL							
	A (mm)	**B (mm)**	**C (mm)**	**W_1 (mm)**	**W_2 (mm)**	**E (mm)**	**U (mm)**	**O (deg)**
8 mm	180/286 or 180/330	62	12.75	8.4	14.4	1.5	3.6	120
12 mm	180/330	62	12.75	12.4	18.4	1.5	3.6	120
16 mm	330	62	12.75	16.4	22.4	1.5	3.6	120
Tolerance	±0.5	±1.5	−0/+0.15	−0/+1.5	max.	min.	min.	−

Tube specification

Devices in SO8 packages are also available in tubes. The tube dimensions are specified in Fig.7.

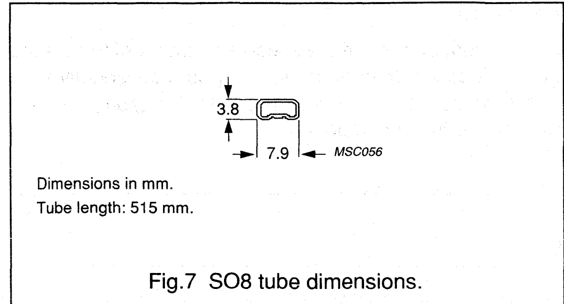


Fig.7 SO8 tube dimensions.

Packing quantities

Table 6 shows the packing quantities for a single box for each package style, and Table 7 shows the smallest packing quantity (SPQ) for a single tube and the packing quantity (PQ) for a single box for SO and SSOP packages.

Table 6 Packing quantities by package with relevant ordering code

PACKAGE	PACKING QUANTITY	ORDERING CODE ENDING	KIND OF PACKING	REEL DIAMETER (mm/inch)
SC-70 (SOT323)	3000 10000	115 135	8 mm tape and reel 8 mm tape and reel	180/7 286/11¼
SC-88 (SOT363)	3000 10000	115 135	8 mm tape and reel 8 mm tape and reel	180/7 286/11¼
SOT23	3000 10000	215 235	8 mm tape and reel 8 mm tape and reel	180/7 286/11¼
SOT89	1000 4000	115 135	12 mm tape and reel 12 mm tape and reel	180/7 330/13
SOT223	1000 4000	115 135	12 mm tape and reel 12 mm tape and reel	180/7 330/13
SO8 (SOT96-1)	2500	118	8 mm tape and reel	330/13
SSOP16 (SOT338-1)	2000	118	16 mm tape and reel	330/13
SSOP24 (SOT340-1)	1000	118	16 mm tape and reel	330/13

Table 7 Packing quantities by package in tubes

PACKAGE	PACKING QUANTITY	ORDERING CODE ENDING	KIND OF PACKING
SO8 (SOT96-1)	100 2000	– 112	515 mm tube (turn-lock) 20 tubes in a box

LEADED DEVICES

Tape and reel packing of TO-92 devices

Tape and reel packing meets the feed requirements of automatic pick and place equipment (packing conforms to IEC publication 286-2 and 286-3). Additionally, the tape is an ideal shipping container.

The transistors are supplied on tape in boxes (ammopack) or on reels. The number per reel and per ammopack is 2000. The ammopack has 80 layers of 25 transistors each. Each layer contains 25 transistors, plus one empty position in order to fold the layer correctly.The ammopack is accessible from both sides, enabling the user to choose between 'normal' (see Fig.8) and 'reverse' tape. 'Normal' is indicated by a plus sign (+) on the ammopack and 'reverse' by a minus sign (–). In the European version, the leading pin is the source.

DROPOUTS

A maximum of 0.5% of the specified number of transistors in each packing may be missing. Up to 3 consecutive components may be missing provided the gap is followed by 6 consecutive components.

TAPE SPLICING

Splice the carrier tape on the back and/or front so that the feed hole pitch (P_0) is maintained (see Figs 9 and 10).

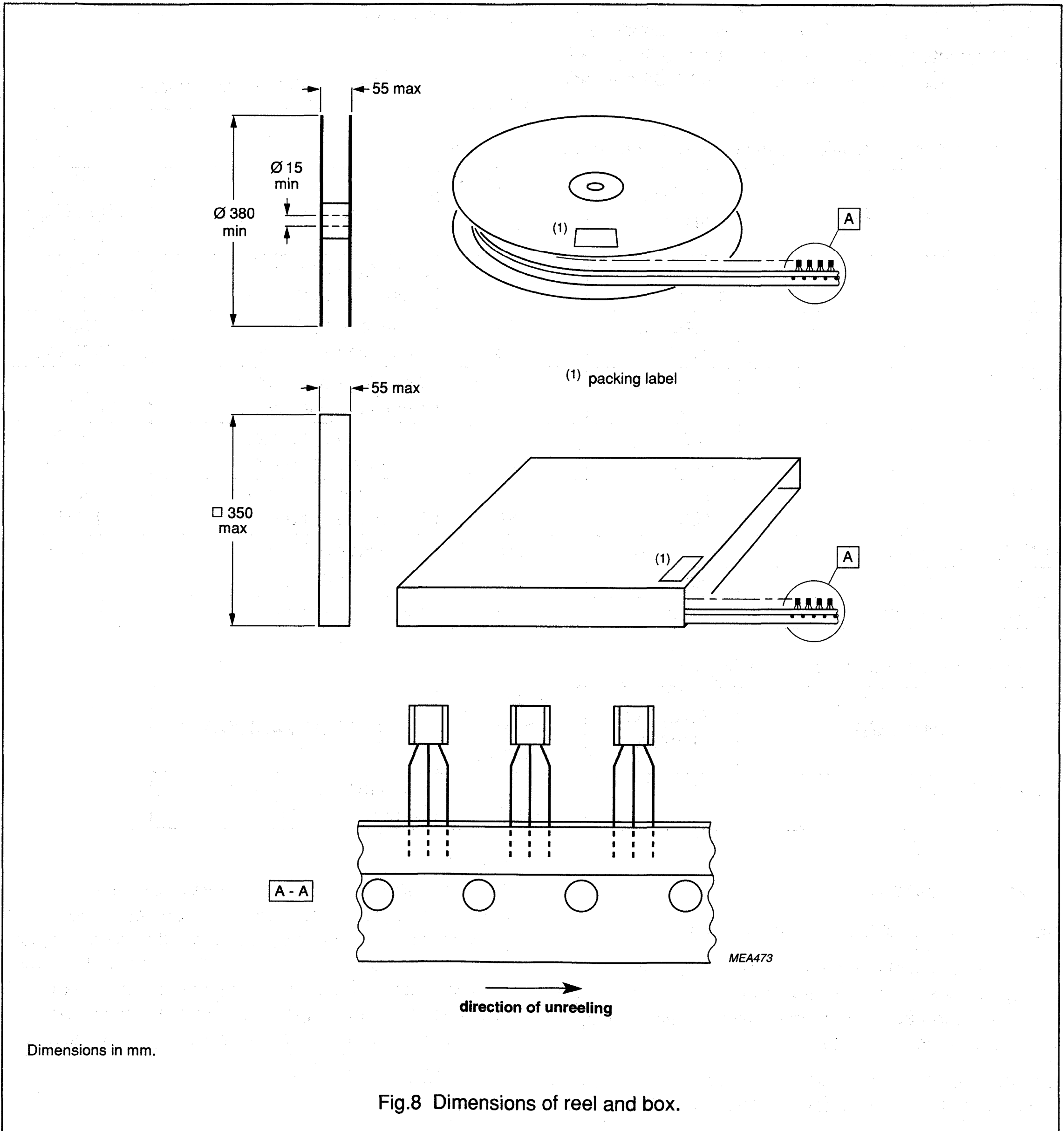


Fig.8 Dimensions of reel and box.

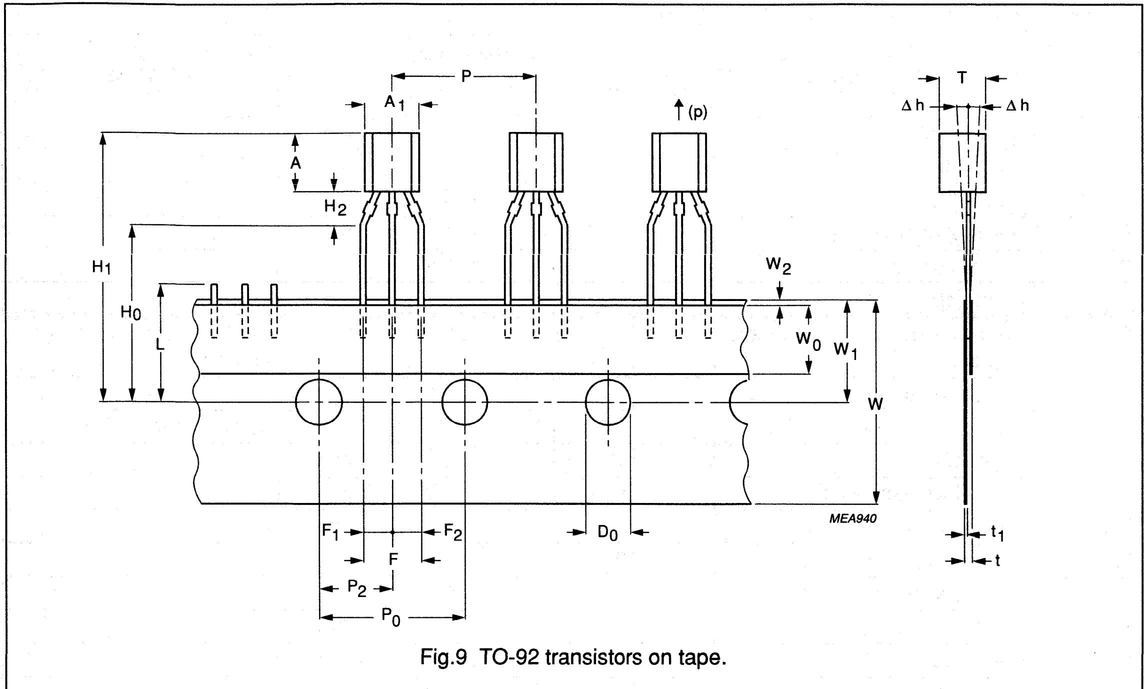


Fig.9 TO-92 transistors on tape.

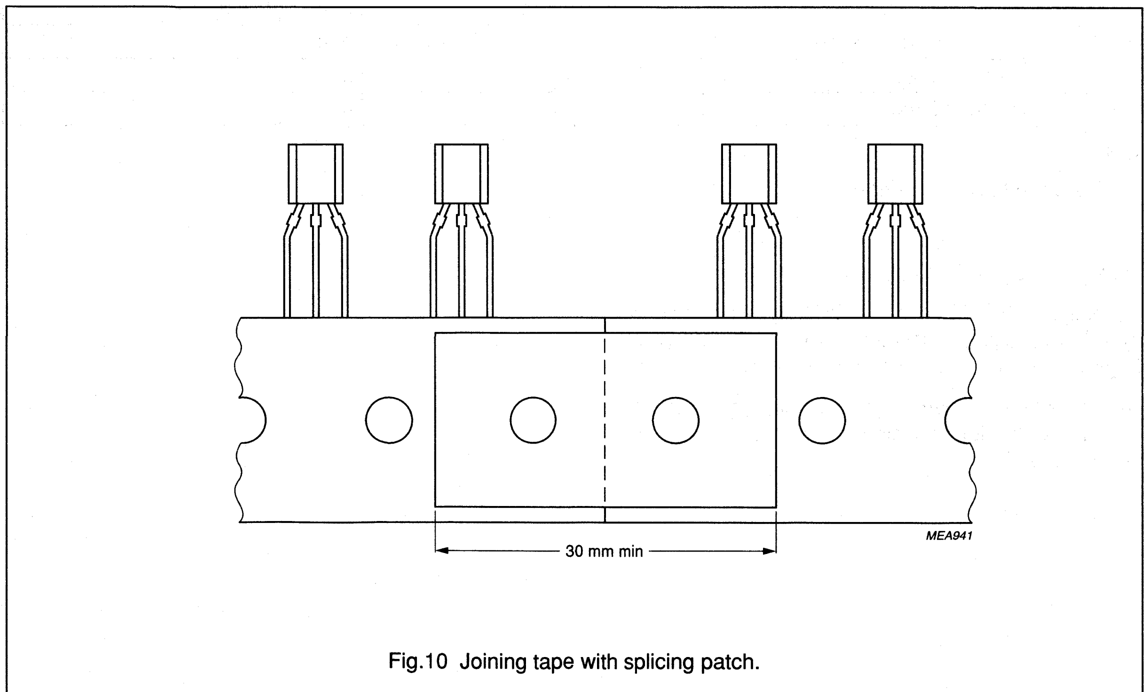


Fig.10 Joining tape with splicing patch.

Table 8 Tape specification (TO-92 leaded types)

SYMBOL	DIMENSION	SPECIFICATIONS					REMARKS
		MIN.	NOM.	MAX.	TOL.	UNIT	
A_1	body width	4	–	4.8	–	mm	
A	body height	4.8	–	5.2	–	mm	
T	body thickness	3.5	–	3.9	–	mm	
P	pitch of component	–	12.7	–	±1	mm	
P_0	feed hole pitch	–	12.7	–	±0.3	mm	
	cumulative pitch error	–	–	–	±0.1		note 1
P_2	feed hole centre to component centre	–	6.35	–	±0.4	mm	to be measured at bottom of clinch
F	distance between outer leads	–	5.08	–	+0.6/–0.2	mm	
Δh	component alignment	–	0	1	–	mm	at top of body
W	tape width	–	18	–	±0.5	mm	
W_0	hold-down tape width	–	6	–	±0.2	mm	
W_1	hole position	–	9	–	+0.7/–0.5	mm	
W_2	hold-down tape position	–	0.5	–	±0.2	mm	
H_0	lead wire clinch height	–	16.5	–	±0.5	mm	
H_1	component height	–	–	23.25	–	mm	
L	length of snipped leads	–	–	11	–	mm	
D_0	feed hole diameter	–	4	–	±0.2	mm	
t	total tape thickness	–	–	1.2	–	mm	t_1 = 0.3 to 0.6
F_1, F_2	lead-to-lead distance	–	–	–	+0.4/–0.2	mm	
H_2	clinch height	–	–	–	–	mm	
(p)	pull-out force	6	–	–	–	N	

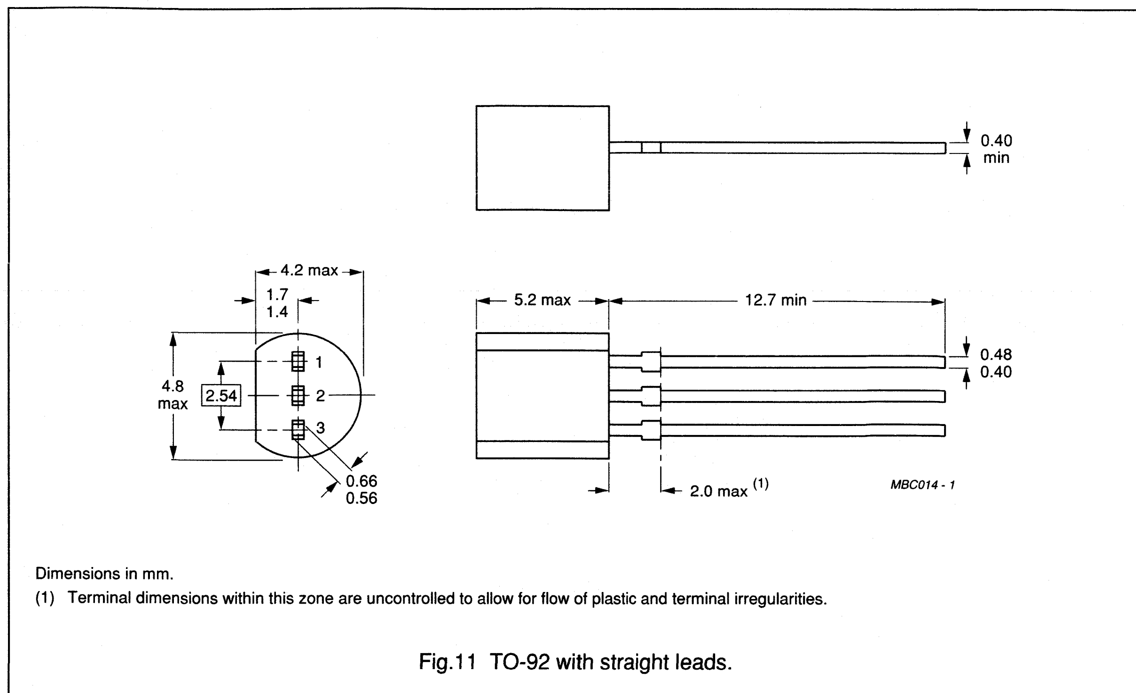
Note

1. Measured over 20 devices.

Bulk packing of TO-92 devices

In addition to TO-92 on tape, TO-92 can also be delivered in bulk. Products are packed in boxes in foil and plastic bags with 1 000 pieces to a bag and 5 bags to a box.

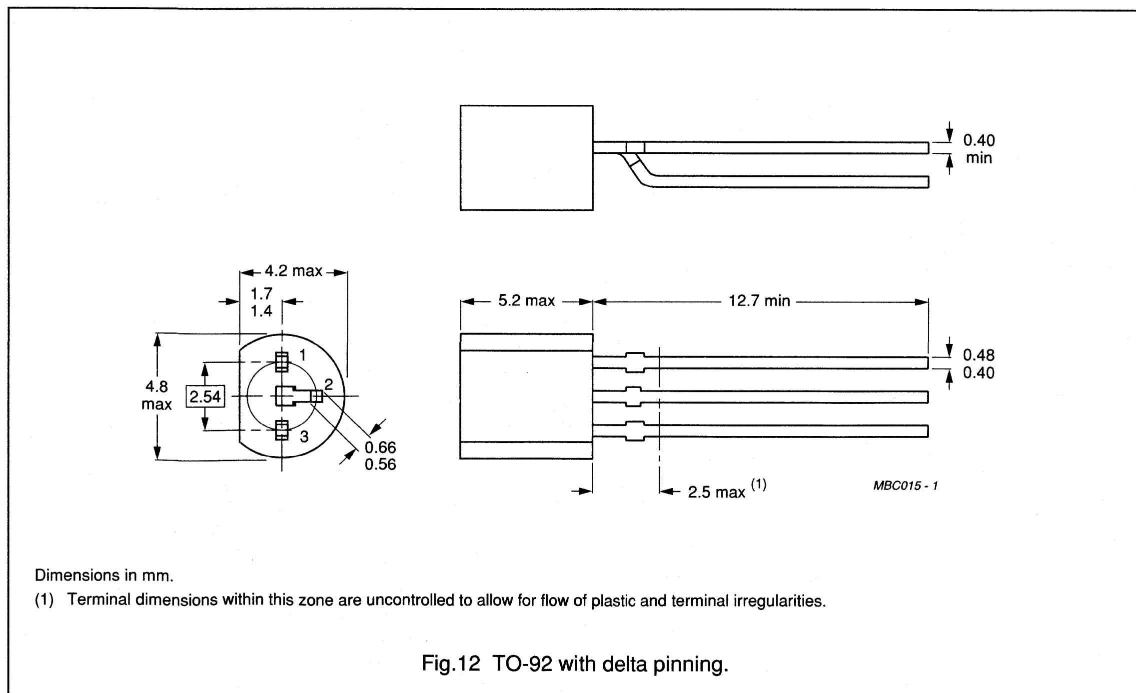
As well as the standard TO-92 with straight leads (see Fig.11), leads with delta pinning are available in bulk on request (see Fig.12).



Dimensions in mm.

(1) Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

Fig.11 TO-92 with straight leads.



Dimensions in mm.

(1) Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

Fig.12 TO-92 with delta pinning.

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Data handbook system

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